



### INTEL DEBUTS ASIC ALTERNATIVE

*By Tom R. Halfhill {12/13/10-01}*

Intel has introduced an interesting alternative to custom chips: an Atom CPU packaged with an Altera FPGA in a multichip module. The new Atom E600C series (previously known as Stellarion) is suitable for some low-volume embedded applications that need to wrap an x86 processor in application-specific logic.

The E600C bonds two die side by side in a 1,466-pin 37.5mm flip-chip BGA (FCBGA). One die is an Atom E600-series single-core processor (“Tunnel Creek”). It integrates a 512KB L2 cache, an Intel GMA600 graphics engine, an Intel HD Audio engine, a low-voltage differential signaling (LVDS) display interface, a 32-bit DDR2-800 memory controller, four lanes of PCI Express (PCIe Gen1), and miscellaneous I/O. This die is identical to those in conventionally packaged Atom E600-series processors.

The FPGA die is an Altera Arria II GX. Arria is the company’s midrange family—larger than Cyclone but smaller than Stratix. This Arria chip has 60,214 programmable logic elements, 312 DSP blocks (18-bit by 18-bit multipliers), 5.2Mb of embedded memory, one PCIe hardware block, and eight 3.125Gbps transceivers. The FPGA accounts for 364 I/O pins on the multichip package.

Not all of these resources are available to developers, however. The Atom CPU communicates with the FPGA over two PCIe lanes, leaving only two lanes free for system I/O. On the FPGA side, the CPU link commandeers the PCIe 1×1 hardware block and two of the eight high-speed transceivers. For additional bandwidth, developers can implement another PCIe 1×1 interface as soft intellectual property (IP) in about 5,000 programmable gates.

Intel pitches the E600C as a “configurable Atom-based processor,” but the CPU isn’t configurable. Rather, the whole multichip device is a configurable SoC, to the extent that developers can implement their custom IP in the programmable fabric. In concept, the E600C is similar to some Altera and Xilinx FPGAs that embed CPU hard cores. The crucial difference is that those CPUs are tightly coupled to the fabric, whereas the Atom CPU is loosely coupled to the FPGA over PCIe. Offloading cryptography to the FPGA is practical, for example, but adding low-latency custom instructions to the CPU is not.

Production shipments begin in January. Intel’s 1,000-unit prices range from \$61 to \$106, depending on the CPU frequency (600MHz to 1.3GHz) and temperature rating (commercial or industrial). Thermal design power (TDP) ranges from 2.7W to 3.6W. Power can exceed those specifications, however, if custom logic strenuously exercises the FPGA.

Atom E600-series processors without FPGAs cost only \$19 to \$64 in the same speed range, but the \$42 price premium for the multichip product looks much better when compared with Altera’s single-unit prices for an equivalent Arria II device: \$500 to \$800. Altera doesn’t quote volume pricing. (FPGA prices start in the exosphere but plummet like a meteorite in volume.)

Some developers will, no doubt, find applications for the Atom E600C. Replacing two chips with one will save board space and allow a single board to serve multiple products. As an ASIC alternative, the E600C cuts engineering costs, is faster to market, and enables field upgrades. And it’s one more way of bundling a CPU with an FPGA (see [MPR 10/25/10-01](#), “Altera Adds CPUs for FPGAs”). But it’s no substitute for a CPU licensing model like ARM’s, which gives chip developers far more design flexibility and reduces costs for large production runs.

There is hope, however. Intel has formed the Atom and SoC Development Group, suggesting that designs proven first in the E600C may lead to an ASIC or ASSP. Also, Intel has a history of converting multichip packages into conventional single-chip products, as seen most recently with Arrandale and Sandy Bridge. A monolithic Atom SoC with programmable logic is foreseeable, especially in light of Intel’s recent agreement to manufacture Achronix FPGAs in next-generation 22nm technology (see [MPR 11/15/10-02](#), “Intel Eyes Foundry Market”). ♦

