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MICROPROCESSOR REPORT

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CAVIUM COMPLETES OCTEON II LINE

Four New Series Fill Out Family of Networking Processors

By Tom R. Halfhill {11/15/10-01}

Chips are breeding faster than rabbits at Cavium, the rapidly growing supplier of networking and security processors. Today, Cavium announced four new series in the 64-bit Octeon II family, populating a product line that now spans an unprecedented range from 1 to 32 CPU cores per processor chip.

The new Octeon II series are the CN60xx, CN61xx, CN62xx, and CN66xx. They join the CN63xx, CN67xx, and CN68xx series announced earlier this year. (See *MPR 5/31/10-02*, "Cavium Pushes Octeon to 32 CPUs.") The new brood fills the low-end to midrange Octeon II line, leaving no significant gaps. Family members differ in their number of CPUs, clock speeds, L2 caches, memory controllers, networking accelerators, packet interfaces, and other I/O. Despite these broad differences, Cavium preserves pin compatibility among similar chips, as Figure 1 shows.

All Octeon II processors use Cavium's cnMIPS-II CPU core—an original implementation of the MIPS64-R2 architecture licensed from MIPS Technologies. Target clock frequencies are 400MHz to 1.5GHz, and typical power consumption ranges from 2.5W for the smallest chips to 60W for the 32-core giant. Unlike previous Octeon chips, which were manufactured by TSMC, the new chips will be manufactured in Samsung's 65nm G process and are scheduled for production next year. Cavium says it began sampling the CN62xx and CN63xx series to customers in June, and the other chips are scheduled to begin sampling in 1Q11 and 2Q11. So far, Cavium claims more than 30 design wins for Octeon II.

Cavium designed Octeon II for network-infrastructure, data-storage, and data-center equipment. At the low end, these chips target small-business routers, switches, gateways, printers, and network-attached storage (NAS) subsystems. The midrange to high-end chips are intended for larger versions of those systems, plus network security, enterprise WLAN controllers, storage controllers, and other communications equipment. They are suitable for both control-plane and data-plane applications, although the larger multicore designs are intended mainly for the data plane.

Octeon II succeeds Octeon Plus and the original Octeon family, which inaugurated Cavium's strategy to become more than a supplier of security coprocessors. (See *MPR 10/5/04-01*, "Cavium Branches Out.") Now fully populated, the Octeon II family gives Cavium a formidable product line that will strengthen its competitive position against Freescale's QorIQ processors and NetLogic's XLP.

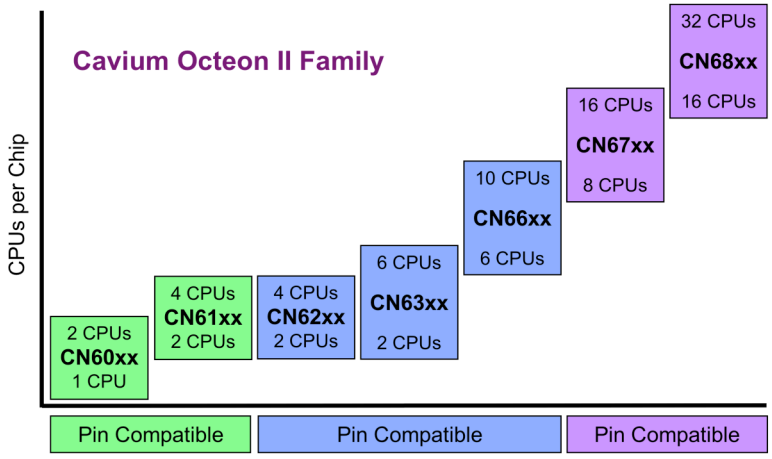

Figure 1. Cavium's Octeon II family. Newly announced series are the CN60xx, CN61xx, CN62xx, and CN66xx. The other series were announced earlier this year.

	CN60xx	CN61xx	CN62xx	CN63xx	CN66xx	CN67xx	CN68xx
CPU Type	Cavium cnMIPS-II (MIPS64-R2 compatible)						
CPU Cores	1–2 CPUs	2–4 CPUs	2–4 CPUs	2–6 CPUs	6–10 CPUs	8–16 CPUs	16–32 CPUs
CPU Frequency	400–900MHz	400M–1.2GHz	800M–1.0GHz	800M–1.5GHz	800M–1.5GHz	Up to 1.5GHz	Up to 1.5GHz
L1 Cache	37KB I-cache, 32KB D-cache						
L2 Cache	512KB	1MB	1MB	2MB	2MB	4MB	4MB
Memory Cntlrs (w/ ECC)	1x 32-bit DDR3-1066	1x 64-bit DDR3-1066	1x 64-bit DDR3-1600	1x 64-bit DDR3-1600	1x 64-bit DDR3-1600	2x 64-bit DDR3-1600	4x 64-bit DDR3-1600
Ethernet Controllers	6x GbE, 2x FE	1x 10GbE or 2x GbE, 2x FE	1x 10GbE or 4x GbE	1x 10GbE or 4x GbE	2x 10GbE or 4x GbE	5x 10GbE or 12x GbE	5x 10GbE or 12x GbE
Interlaken	—	—	—	—	—	Up to 4x	Up to 8x
PCI Express, Serial RapidIO	3x PCIe	4x PCIe	4x PCIe or 4x sRIO	8x PCIe or 8x sRIO	8x PCIe or 1x sRIO, 4x PCIe	16x PCIe	16x PCIe
TCP/IP Perf	5Gbps	5Gbps	8Gbps	10Gbps	15Gbps	20Gbps	40Gbps
Crypto Accel*	5Gbps	5Gbps	8Gbps	10Gbps	15Gbps	20Gbps	40Gbps
Reg-Ex Engine	1Gbps	1Gbps	4Gbps	7Gbps	7Gbps	20Gbps	20Gbps
Comp/Decomp	—	—	5Gbps	5Gbps	10Gbps	20Gbps	20Gbps
RAID5/6	1Gbps	1Gbps	5Gbps	4Gbps	4Gbps	5Gbps	5Gbps
De-Dupe	1Gbps	1Gbps	5Gbps	4Gbps	6Gbps	20Gbps	20Gbps
Classification	5Gbps	5Gbps	5Gbps	10Gbps	15Gbps	20Gbps	40Gbps
Package	31mm TEBGA, pin compatible		31mm FCBGA, pin compatible			45mm FCBGA, pin compatible	
Power (max)	2.5–5W	4–10W	8–12W	10–25W	12–28W	16–50W	20–60W
Samples	2Q11 (est)	2Q11 (est)	2Q10	2Q10	2Q11 (est)	1Q11 (est)	1Q11 (est)
Production	4Q11 (est)	4Q11 (est)	1Q11 (est)	1Q11 (est)	4Q11 (est)	3Q11 (est)	3Q11 (est)
List Price	$19–$32	$40–$80	$60–$115	$60–$200	$100–$280	$280–$580	$500–$999†

Table 1. Key parameters for Cavium's Octeon II family. FE=Fast Ethernet. *Estimated performance with the IPSec security protocol and Snow 3G stream cipher. (Source: Cavium, except †The Linley Group estimate)

Familiar Formula: CPUs + Coprocessors

Adherence to the MIPS64 instruction-set architecture has maintained a high degree of software compatibility across three Octeon generations. Octeon II's cnMIPS-II core adds a few instructions and improves performance over Cavium's first-generation cnMIPS64 CPU while maintaining backward compatibility. Octeon II adds more acceleration engines and I/O controllers, requiring minor changes to high-level C/C++ control code to call the modified application programming interfaces (APIs).

The cnMIPS-II is an integer-only CPU with two-way superscalar execution but no instruction reordering or CPU-level multithreading—Cavium prefers a multicore approach to threading. Compared with most competing designs, Cavium's CPU is relatively simple, deterministic, and compact. These attributes help Cavium integrate up to 32 CPUs per chip in the Octeon II CN68xx, whereas Freescale and NetLogic can fit no more than eight CPUs despite being a full process generation ahead of Cavium's 65nm technology. Cavium has already demonstrated the new CPU running at 1.5GHz in CN63xx samples.

Although Cavium's strength is data-plane processing, Octeon II chips are well suited for mixed-mode processing. To supplement its relatively simple core, Cavium surrounds the CPU with custom coprocessors that accelerate common networking tasks. Usually, an API call to a coprocessor kicks off a multicycle process that runs in parallel with the CPU's control code. Some specialized tasks—such as compression, cryptography, packet classification, and deep packet inspection—run orders of magnitude faster on these engines.

Cavium's first foray into networking was with Nitrox security processors, which remain in the company's product catalog. Octeon II chips integrate the same basic cryptography engine, which has its own parallel pipeline. In addition to varying the number of CPUs and the clock speeds, Cavium equips different chips with different accelerators, memory controllers, and I/O interfaces, according to their target markets. For packet I/O, all Octeon II chips except the CN60xx have XAUI interfaces for 10G Ethernet ports; all have SGMII interfaces for Gigabit Ethernet (GbE). All have PCI Express (PCIe), but only the CN62xx, CN63xx, and CN66xx also have Serial RapidIO (sRIO), which is useful in cellular base stations.

The high-end CN67xx and CN68xx have Interlaken and Interlaken-LA chip-to-chip networking interfaces. Interlaken allows developers to build Octeon II systems with even more than 32 CPUs. (Octeon II doesn't support coherent memory across multiple chips, so the chips are typically arranged in a pipeline fashion.) Interlaken-LA connects to an optional ternary context-addressable memory (TCAM) chip. Table 1 summarizes the key features and performance of Octeon II processors.

As noted in the table, Octeon II preserves pin compatibility among related series of Octeon II chips, except when using additional I/O capabilities. For example, the CN66xx's second XAUI interface doubles the number of possible 10G Ethernet ports compared with the CN63xx and CN62xx. The extra XAUI interface will be useful in fault-tolerant designs with failover capabilities. (Omitting a second XAUI interface on the CN63xx was a rare oversight; for its own CN63xx-based Ethernet adapter, Cavium had to attach an

external 10GbE controller chip to a PCIe interface.) Even so, the CN66xx chips remain footprint compatible with the CN63xx and CN62xx, so they fit the same sockets on the same boards and run the same software.

Sleeping Cipher Silicon

Cavium is touting five new Octeon II features, each having a trademarked whiz-bang name: DormantCrypto, Authentik, EMVisor, Hyper Finite Automata, and PowerOptimizer. The first two features are security remedies for an insecure world, the third is a virtualization extension, the fourth is a different approach to deep packet inspection, and the fifth is a new twist on clock gating.

DormantCrypto allows Cavium and its OEM customers to reduce production, stocking, and shipping costs while still obeying U.S. export regulations that restrict some security-related products. The problem is that Cavium's cryptography engines can encrypt and decrypt data much faster than mainline code running on general-purpose CPUs—performance that's too good for countries on the government's blacklist (the T-5: Cuba, Iran, North Korea, Sudan, and Syria). Manufacturing two versions of the same processor or system—one with the accelerators and one without—inflates costs for both Cavium and its customers, and it complicates inventory stocking.

The usual solution is to isolate the crypto logic with on-chip fuses, then blow the fuses during manufacture to permanently disable the logic. This technique still requires system makers to stock two different versions of the chip.

Cavium has patented a solution that leaves the cryptography logic dormant until it's unlocked with an encrypted software key that's unique to each chip. These keys are considered too long to crack or forge, and they are entrusted to the equipment suppliers that build systems using Cavium's processors. Suppliers can ship the same systems to all markets and provide the keys only to customers in approved countries. This solution doesn't permanently alter the chip, as blown fuses do, so crippling the cryptography logic is reversible. Cavium says the National Security Administration (NSA) has approved DormantCrypto for export.

The Authentik feature takes DormantCrypto to the next level by locking the whole chip. It's designed to protect equipment suppliers that outsource manufacturing to contract factories. To unlock the processor, end users must have a software key that's unique to the hardware of each system. Again, the equipment suppliers hold and distribute the keys. Among other things, Authentik prevents contract manufacturers from secretly making extra units and selling them through unauthorized channels. Without keys, the processors (and therefore the bogus systems) won't function.

Faster Bare-Metal Hypervisors

Octeon II's EMVisor is a virtualization extension that provides hardware acceleration for hypervisors. Virtualization became popular on servers but is also spreading to embedded systems, especially in networking and communications. EMVisor virtualizes all of the chip's high-speed I/O interfaces and acceleration engines. Each virtual machine can use one or more CPUs as well as the memory controllers, Ethernet ports, and PCIe interfaces. A central controller virtualizes interrupts, and a virtual switch allows multiple virtual machines to exchange network packets with each other. In addition, EMVisor allows developers to dynamically upgrade the virtual machines and deploy remote firmware upgrades.

Cavium's Hyper Finite Automata (HFA) is a new approach to deep packet inspection. Hardware acceleration for deep inspection is common in networking processors, and two traditional approaches are deterministic finite automata (DFA) and non-deterministic finite automata (NFA): two different methods that a regular-expression (reg-ex) engine can use when applying inspection rules to packets.

Earlier Octeon and Octeon Plus chips use DFA, which is good at handling relatively large numbers of simple rules. But as rules become more complex, the processor must retain more and more state information, requiring more memory. DFA performance remains deterministic, however. The other common inspection method, NFA, can handle even the most complex Perl-compatible regular expressions, which may contain numerous wildcards. Cavium says HFA combines the best of both methods, but it remains unproven.

Throttling Logic to Save Power

Octeon II's PowerOptimizer is an improvement over the clock gating in Octeon Plus, increasing the number of gated blocks in each CPU from around a dozen to more than 100. The chip can briefly turn off the clock for very small logic blocks—as small as individual pipeline stages—for time increments as brief as one clock cycle. All modern CPUs use clock gating to some degree. Like other CPUs, Octeon II can determine when a logic block isn't needed for a particular operation and turn off its clock until the block is needed.

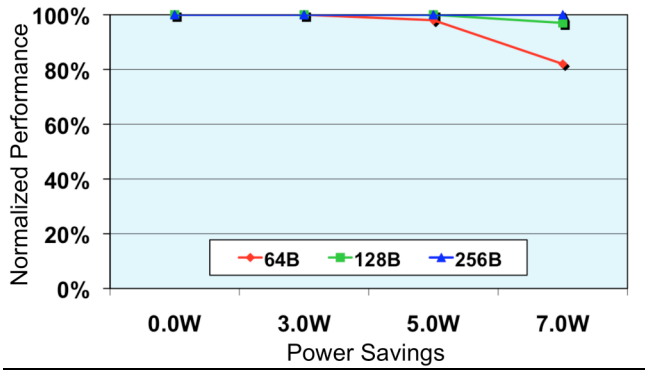

Figure 2. Power savings using Octeon II's PowerOptimizer. Cavium's dynamic power monitor and feedback mechanism uses fine-grained clock gating to hold power consumption below a preset limit. (Source: Cavium)

In addition, Octeon II chips have a programmable feedback mechanism that monitors the software workload, estimates power consumption, and automatically keeps power from rising above a predetermined limit. If power threatens to exceed the programmed limit, the chip begins shutting off circuits by gating their clocks. The limit can be set individually for each CPU. This approach can smooth power spikes caused by bursty traffic, preventing the chip from exceeding its thermal limit without hampering throughput.

With proper tuning, Cavium's approach can also reduce power in situations where the processor's performance is bottlenecked in one area (for example, memory bandwidth or crypto performance). In these situations, PowerOptimizer can throttle back the other components in the processor, saving power without sacrificing performance. Cavium says PowerOptimizer cuts power consumption by 15% to 20% for more than 95% of applications.

Figure 2 shows results of PowerOptimizer at work. For this test, Cavium ran an Internet Protocol forwarding program on a 1.3GHz Octeon II CN6335 processor with six CPUs. Packet sizes ranged from 64 bytes to 256 bytes. The chart shows little or no performance loss while saving up to about 5W of power, which could be the programmed power threshold if the software must maintain a certain performance level. Attempting to save more than 5W, however, noticeably degrades performance for smaller packets.

This approach departs from the most popular method of reducing power consumption: dynamically varying the core voltage and clock frequency in response to the software workload. Power varies linearly with frequency and quadratically with voltage, because voltage is a squared term in the equation. Power savings can be dramatic when a lighter workload allows a processor to dial down its voltage and clock speed.

This method must be used carefully, however, because the on-board voltage regulator and PLL must stabilize the voltage and clock speed after switching gears. This delay is on the order of milliseconds, making frequent changes impractical. Also, creating and isolating individual voltage and frequency domains for numerous CPUs becomes too complex in large designs—a particular concern for Cavium, whose largest Octeon II has 32 CPUs. Yet the ability to vary power consumption per CPU is vital when workloads are unevenly distributed. Competing processors typically group CPUs into multiple voltage domains.

Octeon II chips always run at their rated voltage and clock speed, eliminating the stabilization delays of voltage/frequency scaling. In effect, Octeon II can "emulate" lower clock frequencies on a 16-level scale of programmable power thresholds. Each CPU can run at a different emulated frequency while actually running at the same frequency.

PowerOptimizer appears to make sense only when the CPU isn't the performance bottleneck. Emulating a lower clock frequency by idling clock-gated circuits won't be effective if a task absolutely needs those idle circuits for useful work. In other words, the performance threshold must be under the power threshold. Cavium's approach provides more flexibility, but voltage scaling can provide a bigger gain. The proof will come when Cavium can demonstrate that Octeon II delivers superior performance per watt compared with its competition.

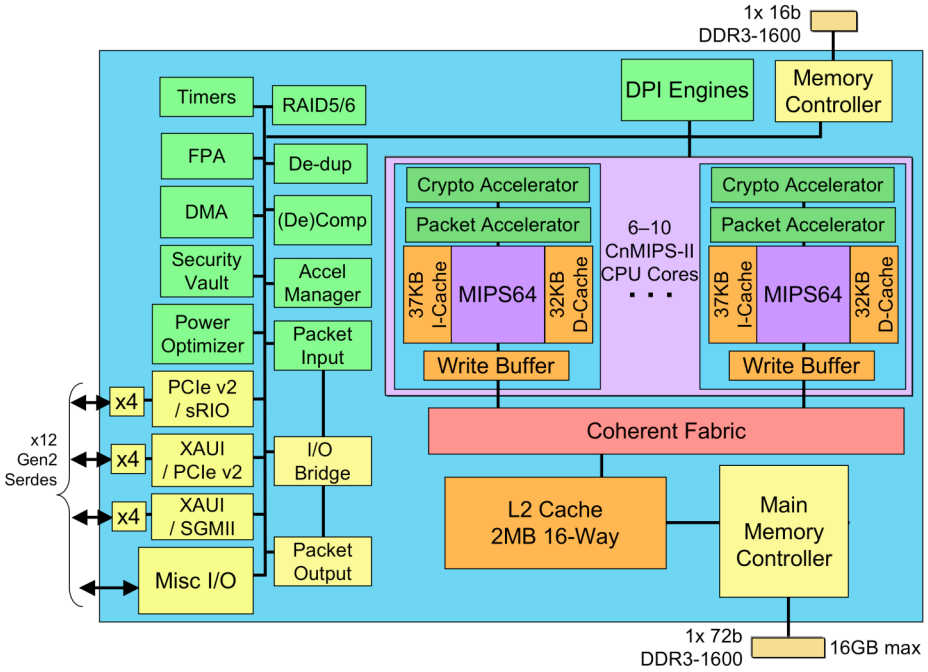

Figure 3. Cavium Octeon II CN66xx block diagram. CN66xx-series chips will have 6 to 10 CPU cores; other features are common throughout the series. (Source: Cavium)

Freescale, NetLogic Compete

The closest Octeon II competitors are Freescale's QorIQ processors and NetLogic's new XLP family. *Microprocessor Report* has covered recent announcements by both companies in depth: see *MPR 9/6/10-01*, "Freescale Upgrades QorIQ"; *MPR 7/5/10-01*, "Freescale's P5 Raises QorIQ's I.Q."; and *MPR 7/26/10-01*, "NetLogic Broadens XLP Family." Only a few Octeon II chips are sampling now. NetLogic recently began sampling the XLP, and Freescale already has some QorIQ chips in production.

Two of the new Octeon II series invite comparisons: the CN66xx and the CN61xx. The former has the highest performance among the newly announced products and is mostly pin compatible with the smaller CN63xx and CN62xx. (We covered the larger CN67xx and CN68xx series in our previously cited article, "Cavium Pushes Octeon to 32

CPUs.") The CN61xx is the higher-performance series in the Octeon II family's lower end, and it's pin compatible with the smaller CN60xx.

The CN66xx chips are designed for midrange networking and communications equipment. They will have 6 to 10 CPUs running at clock speeds of 800MHz to 1.5GHz. These CPUs will share 2MB of L2 cache and one 64-bit DDR3-1600 memory interface. The CN66xx chips support up to two 10G Ethernet ports, up to four GbE ports, and up to eight PCIe interfaces. For cellular base-station designs, developers can configure the ×4 serdes to support one or two sRIO interfaces. Figure 3 shows a block diagram of the CN66xx.

Competitors include Freescale's QorIQ P4 series and NetLogic's XLP3xx series. Freescale's P4 chips have four (P4040) or eight (P4080) CPUs. Both use Freescale's Power Architecture e500mc core—a single-threaded two-way superscalar machine, like Cavium's cnMIPS-II core. In these QorIQ chips, the Power e500mc runs at 1.5GHz—the same top speed as the CN66xx CPUs. The Power e500mc can execute instructions out of order, giving it a slight advantage over the in-order cnMIPS-II, but Cavium's CPUs are 64-bit cores, and the CN6645 will have more CPUs (10).

XLP CPU Core Is More Powerful

NetLogic's XLP3xx series has three members: the single-core XLP304, the dual-core XLP308, and the quad-core XLP316. None has as many CPUs as Cavium's smallest CN66xx, but one NetLogic EC4400 CPU core will deliver far more performance than a cnMIPS-II core. The EC4400 is an original MIPS64-compatible design with four-way superscalar execution, instruction reordering, and four threads per CPU. It's a huge improvement over the single-issue, in-order CPUs in NetLogic's older XLR and XLS processors, and it's more sophisticated (and complex) than the two-way superscalar, single-threaded CPUs found in Cavium's Octeon II and Freescale's QorIQ P4.

Furthermore, NetLogic will manufacture XLP processors in TSMC's 40nm G process—a full generation ahead of Octeon II. Using this process advantage, NetLogic is currently sampling XLP chips at 2.0GHz—33% faster than Octeon II's top speed. With its combination of superior microarchitecture and higher frequency, one EC4400 CPU should match the performance of two cnMIPS-II CPUs when running control-plane code. In data-plane applications, the EC4400's ability to run four threads per CPU will further increase throughput to match three or, in some cases, four cnMIPS-II CPUs.

Table 2 compares Cavium's Octeon II with Freescale's QorIQ P4 series and NetLogic's XLP 3xx series. A 6-core CN66xx chip looks like the closest competitor for the P4040 and XLP308, whereas the 10-core CN66xx matches up against the P4080 and the XLP316.

CN66xx Offers More Accelerators

Freescale's QorIQ P4040 has four CPUs; the P4080 has eight. Both have more cache and memory bandwidth (20.8GB/s versus 12.8GB/s) than the CN66xx chips, so they stand a better chance of sustaining their peak performance on memory-intensive applications. The P4 chips have more Gigabit Ethernet interfaces, but they offer only three PCIe interfaces, as opposed to eight in the CN66xx. If a design needs fewer than eight PCIe interfaces and only one 10G Ethernet port, Cavium offers the CN62xx series, which is similar to the CN66xx and fits the same sockets. In addition, the CN66xx has RAID6, deduplication, and decompression engines that the QorIQ chips lack, making Octeon II better suited to certain types of storage and antivirus designs.

Even giving Freescale a slight edge in per-CPU performance, the 6-CPU CN66xx will clearly outperform the

	Cavium Octeon II CN66xx Series	Freescale QorIQ P4 Series	NetLogic XLP 3xx Series
CPU Type (ISA)	cnMIPS-II (MIPS64-R2)	Power e500mc (32-bit Power)	EC4400 (MIPS64-R2)
CPU Cores	6–10 CPUs	4 or 8 CPUs	1, 2, or 4 CPUs
Instruction Pipeline	9 stages, 2-way issue	7 stages, 2-way issue	12 stages, 4-way issue
Threads	1 per CPU	1 per CPU	4 per CPU
CPU Freq (max)	800MHz–1.5GHz	1.5GHz	2.0GHz
L1 Cache (I / D)	37KB / 32KB per CPU	32KB / 32KB per CPU	64KB / 32KB per CPU
L2 Cache	2MB	128KB per CPU	512KB per CPU
L3 Cache	None	2MB	1MB per CPU
Memory Cntlrs (w/ ECC)	1x 64-bit DDR3-1600	2x 64-bit DDR3-1300	2x 64-bit DDR3-1600
Ethernet Controllers	2x 10GbE or 4x GbE	2x 10GbE, 8x GbE	2x 10GbE or 8x GbE
PCI Express	8x PCIe	3x PCIe	8x PCIe
Serial RapidIO	1x sRIO	2x sRIO	4x sRIO
Crypto Accel?	Yes	Yes	Yes
Reg-Ex Engine?	Yes	Yes	Yes
RAID Engine	RAID5/6	RAID5	RAID5/6
Other Accelerators	De-dupe, comp/decomp	None	None
IC Process	Samsung 65nm G	Freescale 45nm SOI	TSMC 40nm G
Package	31mm FCBGA	FC-PBGA, 1,295 pins	BGA, ~1,000 pins
Power	12–28W (max)	19–27W (typ), 24–33W* (max)	20–30W (max)
Sampling	2Q11 (est)	3Q09, 4Q09	4Q10 (est)
Production	4Q11 (est)	2H10	3Q11 (est)
List Price	$100–$280	$250–$400*	$150–$300*

Table 2. Comparison of midrange networking processors. With six CPUs, the CN6660 will outperform the four-CPU P4040 and match up well against the two-CPU XLP308. (Source: vendors, except *The Linley Group estimate)

P4040, and the 10-CPU CN6645 should slightly edge the P4080 on typical application code. Although P4 chips are built in a 45nm silicon-on-insulator (SOI) process, they still appear to use more power than the corresponding Octeon II products. The CN66xx thus outperforms the QorIQ chips in all regards, unless its inferior memory bandwidth creates a bottleneck. The P4040 and P4080 began production last year, however, whereas the CN66xx is at least six months from sampling.

The dual-core 2.0GHz XLP308 will compete strongly with Cavium's 6-core 1.5GHz CN66xx on data-plane applications, and the quad-core XLP316 will crush the 10-core CN6645. The XLP308 and XLP316 have significantly more cache than the CN66xx chips and twice as much memory bandwidth (25.6GB/s versus 12.8GB/s)—features that are generally useful in data-plane applications. They also have twice as many GbE ports and four times as many sRIO interfaces.

Despite NetLogic's lead in process technology, the quad-core XLP316 uses about the same power as the 10-core CN6645: a price must be paid for larger caches, an additional memory controller, richer I/O, and a more complex CPU that runs 33% faster. If 30W is too hot to handle, NetLogic's dual-core XLP208 uses only 15W (maximum) and is a good match for a six-core CN66xx. Alternatively, dialing down the XLP316's clock frequency to match Cavium's 1.5GHz clock rate should save at least 7W—or more, if the voltage also falls—dropping the XLP316 below the 10-core CN6645.

Greater Integration Helps Cavium

Toward the low end of the performance spectrum, Cavium's Octeon II CN60xx and CN61xx series will compete with Freescale's QorIQ P1 and P2 series, as well as NetLogic's XLP1xx and XLP2xx series. In this crowded corner of the market, numerous chips with one, two, or four CPUs are slugging it out. Table 3 compares the CN61xx with two examples: Freescale's dual-core P1022 and NetLogic's single-core XLP104.

All the chips in this group have similar performance, power, and features. The CN61xx is unique in providing a 10GbE port, but this high-speed interface is rarely used in low-end applications. The NetLogic processor can extrude more GbE ports. Like the CN66xx, however, the CN61xx has more acceleration logic.

	Cavium Octeon II CN61xx Series	Freescale QorIQ P1022	NetLogic XLP XLP104
CPU Type (ISA)	cnMIPS-II (MIPS64-R2)	Power e500v2 (32-bit Power)	EC4400 (MIPS64-R2)
CPU Cores	2–4 CPUs	2 CPUs	1 CPU
Instruction Pipeline	9 stages, 2-way issue	7 stages, 2-way issue	12 stages, 4-way issue
Threads	1 per CPU	1 per CPU	4 per CPU
CPU Freq (max)	400MHz–1.2GHz	1.055GHz	500MHz–2.0GHz
L1 Cache (I / D)	37KB / 32KB per CPU	32KB / 32KB per CPU	64KB / 32KB per CPU
L2 Cache	1MB	256KB	512KB
L3 Cache	None	None	512KB
Memory Cntlrs (w/ ECC)	1x 64-bit, DDR3-1066	1x 64-bit DDR3-800	1x 64-bit DDR3-1333
Ethernet Controllers	1x 10GbE or 2x GbE, 2x FE	2x GbE	5x GbE
PCI Express	4x PCIe	3x PCIe	4x PCIe
Other I/O	2x USB 2.0 + PHYs	2x USB 2.0, 2x SATA	2x USB 2.0 + PHYs, 2x SATA
Crypto Accel?	Yes	Yes	Yes
Reg-Ex Engine?	Yes	No	Yes
RAID Engine	RAID5/6	RAID5	RAID5/6
Other Accelerators	De-dupe, comp/decomp	None	None
IC Process	Samsung 65nm G	Freescale 45nm SOI	TSMC 40nm G
Power	4–10W (max)	3.0W (typical), 5.5W* (max)	2.5–10W (max)
Sampling	2Q11 (est)	1Q10	4Q10 (est)
Production	4Q11 (est)	4Q10	3Q11 (est)
List Price	$40–$80	$42	$40–$50*

Table 3. Comparison of low-end networking processors. Cavium's CN61xx offers a wider range of Ethernet speeds and more acceleration engines than competing processors. FE=Fast Ethernet. (Source: vendors, except *The Linley Group estimate)

NetLogic's XLP chips are fabricated in a 40nm G process, which should confer a power advantage similar to Freescale's, but NetLogic specifies as much total power for the single-core XLP104 as Cavium claims for the quad-core CN6140. This is largely because the XLP104 runs up to 67% faster and has a more powerful CPU. It will outperform a dual-core CN6120 but not the CN6140, except on pure data-plane applications.

One of NetLogic's strengths is that its quad-threaded CPUs excel in data-plane processing. Small systems built with one-, two-, or four-CPU chips often assign control- and data-plane duties to the same processor. NetLogic expects to begin production in 3Q11; developers must wait a little longer for Cavium's chips, but Freescale's P1022 is available now.

Next year, not long after the new Octeon II chips sample, we expect Freescale to begin sampling chips in next-generation process technology (32nm or 28nm) while pushing its new 64-bit CPU core (Power e5500) deeper into the QorIQ product line. These developments would pose a greater threat to Octeon II. Cavium hasn't disclosed its chosen process technology for the next-generation Octeon III, but we won't be surprised if those future processors skip 40nm and jump directly to 32nm or 28nm as well. Therefore, we expect competition to intensify among chips with two to eight CPUs. Nevertheless, Cavium's ability to integrate more CPUs (up to 32 per chip) will help the company defend its high ground.

From Infrared to Ultraviolet

Cavium's latest announcements strengthen the Octeon II family with highly integrated processors spanning the widest performance spectrum in the industry. Whether a project calls for a chip with 1 CPU, 32 CPUs, or anything in between, the Octeon II family has a likely candidate. Even formidable competitors like Freescale and NetLogic currently offer no more than eight CPUs per chip.

But Cavium's strengths go beyond CPUs. From the start, Octeon processors have led the industry with copious amounts of acceleration logic. Dedicated engines offload packet classification, pattern matching, compression, decompression, deduplication, and other chores that would bog down the general-purpose CPUs. Cavium's extra muscle is harder to quantify but makes Octeon processors more powerful than they appear for applications that require RAID6, deduplication, or decompression.

Despite its lagging process technology, Octeon II is very competitive with Freescale's QorIQ and NetLogic's XLP families—a testament to Cavium's engineering talent and market savvy. Octeon II performance scales higher than QorIQ's but is similar to the XLP's, although the QorIQ P5 and XLP are better for high-end control-plane applications. Cavium has a few extra accelerators and I/Os that will be useful in some niche applications, but many of the new chips are 6 to 12 months behind the XLP and QorIQ in reaching the market, providing a window of opportunity for these competitors. With its broad Octeon II family, however, Cavium can lay claim to designs across the entire high-speed embedded market. ♦

Price & Availability

Cavium's new Octeon II CN62xx series is sampling now. The new CN60xx, CN61xx, and CN66xx series are scheduled to begin sampling in 2Q11. Volume production is scheduled for 1Q11 (CN62xx) or 4Q11 (CN60xx, CN61xx, and CN66xx). Pricing is $19–$32 (CN60xx), $40–$80 (CN61xx), $60–$115 (CN62xx), and $100–$280 (CN66xx). For more information, visit *www.caviumnetworks.com/OCTEON-II_CN68XX.html.*