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ALTERA ADDS CPUS FOR FPGAS

New Options: Cortex-A9 and MIPS32, Plus Intel's Stellarton

By Tom R. Halfhill {10/25/10-01}

Embedding a CPU core and peripherals in an FPGA is the fastest way to rush an SoC to market, but the disadvantages have kept most developers loyal to conventional fixed logic. Now, Altera is again using embedded CPUs as bait to lure the industry toward reconfigurable logic. This time, the world's second-largest FPGA company is pitching three different CPU architectures—ARM, MIPS, and Nios—plus a fourth option of the x86 in a multichip module from Intel.

These choices span a broader range of implementation options than ever before. Developers will be able to choose a hard core (the foundry builds the CPU in fixed logic on the same die as the programmable fabric), soft cores (developers compile a synthesizable CPU for the fabric at design time), and the Intel multichip module (which pairs an Atom processor with an Altera FPGA). Although Altera and other FPGA vendors have offered both hard and soft CPUs for years, Altera's new "Embedded Initiative" is the most comprehensive CPU-FPGA strategy to date.

Last June, Altera's archrival Xilinx—the leading FPGA vendor—announced an initiative that will embed a dual-CPU configuration of ARM's Cortex-A9 MPCore in future devices. Developers will surround those hard cores with application-specific accelerators and peripherals implemented in the programmable-logic fabric. Altera is adopting the Cortex-A9 hard core for its future devices, too. Both companies are promoting a faster path to SoCs that eliminates the long foundry turnaround and risk of multiple spins to fix hardware bugs. As Figure 1 shows, Altera is also promoting a unified development flow for all four CPU architectures it supports.

Going a step further than Xilinx, Altera has also designed a new MIPS32-compatible synthesizable CPU under license from MIPS Technologies. Two additional options for embedded CPUs—ARM's Cortex-M1 and Altera's own 32-bit Nios II—aren't really new. Altera designed the proprietary Nios architecture in 2000, followed by Nios II in 2004 (see *MPR 6/28/04-02*, "Altera's New CPU for FPGAs"). In 2007, ARM introduced Cortex-M1 specifically for FPGA integration (see *MPR 3/19/07-01*, "ARM Blesses FPGAs"). For small projects, low-cost Cortex-M1 development kits are available from industry distributors like Arrow without a special license from ARM.

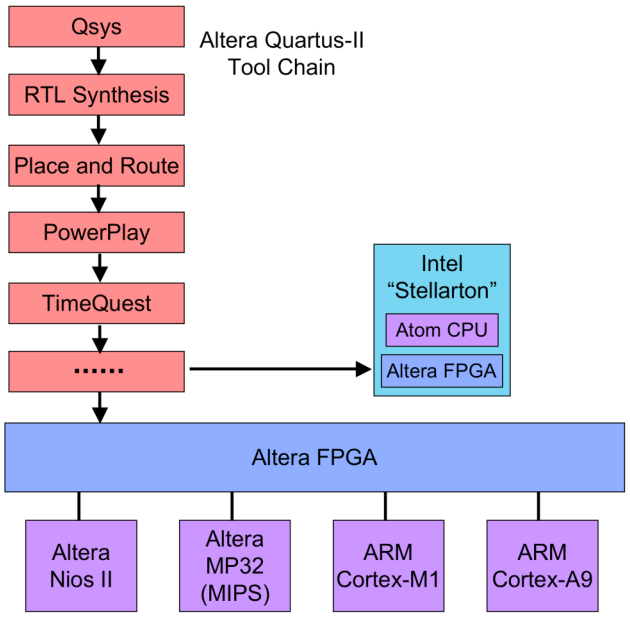

Figure 1. Altera's options for implementing SoCs in FPGAs. A single FPGA tool chain and design flow can target four CPU architectures (ARM, MIPS, Nios II, and x86) and three CPU implementation options: hard cores, soft cores, and Intel's CPU-FPGA multichip module. (Source: Altera)

Programmable logic remains slower, more power hungry, and usually more expensive than implementing the same functions in fixed logic. But with four available CPU architectures, three implementation options, and declining FPGA prices, it's time for SoC developers to take another look at this solution.

Chip Announcements Next Year

Both Altera and Xilinx have announced their intentions but no actual chips. Product introductions are coming in 2011 and will likely span their extensive FPGA product lines. Hard CPUs can be embedded in any FPGA. The ARM, MIPS, and Nios II soft CPUs are small enough to fit into midrange and even many low-end FPGAs, such as those in Altera's Cyclone family.

Intel's multichip module, code-named Stellarton, is an altogether different beast. It will be sold by Intel, not Altera, although Intel has also withheld details of actual products. These multichip packages will integrate an Atom E600-series CPU chip (formerly "Tunnel Creek") with an FPGA large enough to implement the acceleration logic and soft peripherals that Intel deems appropriate for its target markets. Intel briefly revealed Stellarton at the Intel Developers Forum (IDF) in September and plans to introduce products in 1H11. (See *MPR 9/20/10-01*, "Intel Unveils Atom E6xx, Westmere-EX.")

Altera designed its new MIPS-compatible CPU, dubbed the MP32, after obtaining a MIPS32 architecture license last year. Unlike the licensable CPU cores from MIPS, the MP32 is optimized for synthesis in programmable logic. Altera will release more details later, but the MP32 will offer approximately the same performance as Nios II, which can exceed 300MHz in high-end Stratix-class devices. The MP32 will probably be a little larger and costlier than Nios II, however. (Altera uses Nios II to sell FPGAs, so a royalty-free license costs only $495.)

The MP32's biggest advantage over Nios II is an industry-standard CPU architecture that can run operating systems that haven't been ported to Altera's proprietary architecture, including Android, VxWorks, and Windows CE. Thanks to a memory-management unit (MMU), the MP32 can run sophisticated operating systems that manage virtual memory, such as Linux. In addition, the MP32 provides an easier conversion path to FPGAs for developers already using MIPS processors in their ASICs and ASSPs. Altera was able to quickly design the new CPU core because Nios II resembles the original Stanford University MIPS architecture that spawned MIPS Technologies in the 1980s.

Altera plans to extend its HardCopy ASIC program to the new embedded CPUs. HardCopy lets developers convert an FPGA-based design into a structured ASIC with little or no additional design effort. Developers like this option because it offers a path to lower unit costs if a design becomes popular—FPGAs are still far more expensive than equivalent fixed-logic chips, even when purchased in large quantities. Although relatively few developers actually exercise the HardCopy option, it helps sell customers on the concept of implementing an SoC in an FPGA. (See *MPR 12/17/07-02*, "Altera Aims For ASICs.")

Another Sword in the Stone

This isn't the first time Altera has pitched 32-bit ARM and MIPS processors for FPGAs. Ten years ago, Altera introduced its Excalibur product line, which integrated hard-core implementations of the ARM922T. Altera also announced, but never delivered, Excalibur chips with MIPS32 4Kc hard CPUs. Xilinx followed by embedding PowerPC 405 hard cores into some Virtex-II Pro and Virtex-4 FPGAs and later offered PowerPC 440 hard cores in Virtex-5 FXT chips. In addition, Xilinx designed its own soft CPU, the 32-bit MicroBlaze, to compete with Nios. (See *MPR 11/5/01-03*, "FPGAs Catch Fire at MPF.")

Despite considerable fanfare over these announcements, sales of FPGAs with hard CPUs were disappointing. A few of these chips remain available, but they are minimally marketed. Altera says the main reason for their failure to meet expectations was a gap in process technology that favored fixed-logic chips. In 2000, Altera was using 180nm technology for Excalibur at a time when cutting-edge developers needed 130nm performance. (See *MPR 10/16/2000-01*, "Embedded Processor World War.")

Today, the process-technology gap has closed. Both Altera and Xilinx plan to sample next-generation FPGAs manufactured in TSMC's 28nm high-*k* metal-gate (HKMG) technology early next year. Altera is using the high-performance (HP) version of that process for its top-line Stratix-V FPGAs but hasn't announced which version will be used to manufacture its future Arria and Cyclone chips. Xilinx will introduce its future Virtex-7, Artix-7, and Kintex-7 FPGAs in a lower-power derivative of that 28nm process called HPL. (Xilinx has also named Samsung as a second source for 28nm.)

Some cutting-edge ASIC and ASSP projects are also targeting 28nm technology. Those early design starts will begin reaching the market in late 2011 and 2012, around the same time as the next-generation FPGAs. But most new ASICs and ASSPs won't use 28nm for years (if ever), because nonrecurring engineering (NRE) costs have ballooned since 2000. By aggressively adopting 28nm, the two leading FPGA vendors are allowing SoC developers to use programmable logic without dooming their projects to trailing-edge process technology.

FPGAs Become More Capable

Another factor in favor of a renewed CPU-FPGA strategy is that ARM has become the dominant embedded-processor vendor. Ten years ago, the market was more fragmented—CPU architectures like the AMD 29K, Intel i960, Hitachi SuperH, and Motorola 68K still reigned. Since then, the SoC revolution has tilted the market toward licensable CPU

architectures like ARM and MIPS. By offering both a higher-performance hard core (Cortex-A9) and a lower-performance soft core (Cortex-M1), Altera and Xilinx can attract ARM developers who might otherwise start a conventional chip project—assuming that an FPGA is a viable option for other reasons. The new MP32 gives Altera another industry-standard CPU architecture.

A third factor is that FPGAs have advanced significantly since 2000. They have much larger programmable fabrics, giving developers more room to wrap embedded CPUs with application-specific accelerators and peripherals. Today's programmable-logic cells are much faster and more area efficient than they were 10 years ago, and their interconnects are particularly improved. Of course, fixed logic has also greatly advanced since 2000, but SoC projects that were simply impossible for the FPGAs of 10 years ago are now feasible.

In addition, FPGAs are sprouting features rarely or never seen in 2000: hard-wired Ethernet controllers, high-speed serdes transceivers, PCI Express interfaces, analog components, thousands of DSP slices, and megabytes of embedded memory. In particular, the growing capacity for on-chip memory is making FPGA-based SoCs more practical, because some earlier designs were I/O bound. DSP slices have dramatically improved signal-processing performance, winning numerous designs for FPGAs in communications equipment. (Of course, their flexibility for field upgrades is also important, but that hasn't changed much.)

All together, these factors are making FPGA-based designs more competitive with fixed logic at higher volumes than ever before. This is not, however, an ironclad argument for embedding hard CPUs in FPGAs. For FPGA vendors, hard cores remain a risky endeavor. So far, neither Altera nor Xilinx has made the case that a hard Cortex-A9 will significantly change the equation in favor of programmable logic. Soft CPUs are much more popular—Altera says 30% of customer shipments now include one.

Tools Are Changing, Too

Another nagging doubt is the FPGA tool chain and design flow, which has repelled many developers. Functions normally executed in software can run much faster in programmable logic, but programming the fabric usually requires RTL and extensive system modeling to determine which functions to port. ASICs, ASSPs, and general-purpose CPUs are more easily programmed in C and C++. High-level tools are available for FPGAs, but they usually generate less-efficient layouts. Therefore, FPGA projects require different engineering skills and tools.

Both Altera and Xilinx claim their new CPU strategies include better tools and design flows, but the tradeoffs are essentially the same. Altera is retiring SOPC Builder, the 10-year-old system-level integration tool in its Quartus-II FPGA tool chain. Its replacement, called Qsys, lets developers integrate various intellectual property (IP) blocks, whether the IP is licensed from Altera, licensed from a third party, or developed in house. The tool chain can target ARM, MIPS, Nios II, and x86.

Qsys implements a new on-chip switch fabric that Altera says is up to twice as fast as the one in SOPC Builder. Also, Qsys generates the switch fabric in open RTL code that developers can inspect and modify. SOPC Builder synthesized the switch fabric without this degree of transparency.

Another new Qsys feature is compatibility with ARM's latest Amba-4 AXI interconnect standard. Other CPU architectures and IP blocks can also use Amba, but Altera says Amba won't be required to use industry-standard IP. By contrast, SOPC Builder uses Altera's proprietary Avalon interconnect, which is similar to Amba-3 AXI. Amba-4 adds new capabilities for system-wide coherence that will be especially valuable for multicore SoCs. Xilinx is also adopting Amba-4 for its Cortex-A9 FPGAs.

Price & Availability

Altera plans to announce specific FPGAs and embedded-CPU options next year. Devices manufactured in TSMC's next-generation 28nm high-*k* metal-gate process are also scheduled to sample next year. Browse to *www.altera.com/corporate/news_room/releases/2010/products/nr-edward.html*.

Don't Expect Radical Changes

Further analysis must wait until Altera and Xilinx announce their new products next year. Nevertheless, these products don't appear to radically alter the basic tradeoffs between programmable logic and fixed logic. Over time, rising NRE costs keep shifting the unit-volume threshold toward FPGAs, but only gradually. For chip developers near the cusp of that threshold, the competitive positions of FPGA vendors come into play.

IP availability is an important competitive factor, so it's advantageous for an FPGA vendor to offer more CPU-architecture choices and implementation options. For example, MIPS-minded customers will probably favor Altera over Xilinx, thanks to the new MP32 core. If a customer prefers an ARM hard core, either Altera or Xilinx may do if their Cortex-A9 offerings prove similar. Prospective customers who crave an x86 should look closely at Intel's Stellarton. If CPU architecture is irrelevant, both Altera and Xilinx offer their own proprietary CPUs at very low cost.

In the fiercely fought battle between these companies, CPU integration is bound to become an important differentiator. Any performance differences will rest on the companies' preferred flavor of 28nm technology and their respective engineering talents, integrated peripherals, tool chains, and embedded CPUs. In any event, developers will soon see faster FPGAs, new CPU options, and more alternatives to fixed logic for their SoC designs. ♦