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MIPS BOOSTS MULTIPROCESSING

New MIPS32 1074K Challenges ARM Cortex-A9 and Cortex-A15

By Tom R. Halfhill {10/11/10-01}

MIPS Technologies is fighting to defend its strong market positions in home consumer electronics and networking while trying to win new ground in mobile electronics. To accomplish these objectives, the company needs increasingly powerful processors that reduce power consumption—the same conflicting design goals that bedevil almost all of today's CPU vendors.

At the recent Linley Tech Processor Conference in San Jose, MIPS introduced its most powerful embedded-processor core to date: the MIPS32 1074K. Designed primarily for multicore SoCs with two to four CPUs, the 32-bit 1074K combines the strong single-thread performance of the MIPS32 74K with the cache-coherent multiprocessing of the MIPS32 1004K. The licensable 1074K is a fully synthesizable core, is portable to any foundry, and is available now. As Figure 1 shows, the 1074K neatly rounds out the MIPS32 product line, giving MIPS more variety in high-performance embedded CPU cores than any other vendor.

Like most other MIPS32 processors, the 1074K's comfort zone is AC-powered systems—especially home consumer electronics, whose demand for processing power keeps increasing. HDTVs, digital video recorders (DVRs), set-top boxes, and DVD players are gaining better user interfaces and Internet connections. Home networking equipment is moving to faster communication standards, such as fiber, VDSL, and 802.11n Wi-Fi. Network-attached storage (NAS) and voice over IP (VoIP) are moving from the enterprise to consumer markets. Often, these functions are merging into one system: for example, set-top boxes that can stream TV programming from the Internet and record the digital video for later viewing.

Consumers are also demanding mobility. They want access to music, video, and Internet services anytime, anywhere. Video decoding, transcoding, and digital-rights management (DRM) devour nearly as many clock cycles in battery-powered systems as they do in mains-powered systems. To meet these performance demands, SoC developers need faster CPUs and more CPUs, but without busting their power budgets.

In a cache-coherent symmetric-multiprocessing (SMP) configuration, two MIPS 1074K CPUs consume only about 850mW at 1.2GHz, so this processor is suitable for both the tethered and mobile domains. In addition, MIPS was an early adopter of Android and has spent more than a year optimizing its software-development tools and middleware for Google's fast-rising operating system, which straddles the same domains.

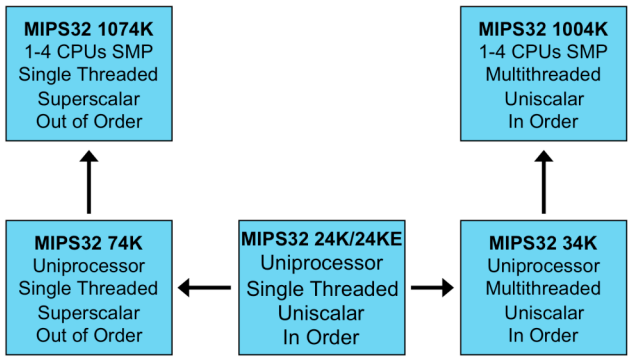

Figure 1. High-performance MIPS32 licensable CPU cores. With the addition of the MIPS32 1074K, MIPS Technologies now offers cache-coherent multiprocessing in both single-threaded and multithreaded flavors and with a choice of in-order single-issue execution or out-of-order superscalar execution. The 1074K also has the most clock-frequency headroom of any MIPS processor—up to 2.5GHz in 28nm CMOS. (Source: MIPS)

For lower-power applications, the MIPS32 family also includes the M14K and M14Kc processors with their compressed 16/32-bit instruction set. (See *MPR 11/16/09-01*, "MicroMIPS Crams Code.") These CPUs compete with ARM's lower-end Cortex processors, whereas the 1074K and its high-performance MIPS32 brethren compete more directly with ARM's Cortex-A8, Cortex-A9 MPCore, and new Cortex-A15.

MIPS32 74K + SMP = 1074K

The MIPS32 1074K comes to the battle with a deep 15-stage pipeline, two- or four-issue superscalar execution, instruction reordering, and optimized logic for implementing a cache-coherent SMP system. One performance-enhancement feature missing from the 1074K is multithreading. Instead, the 1074K emphasizes single-thread performance, as does its direct ancestor, the MIPS32 74K.

For applications that can benefit from multithreading, MIPS already offers the MIPS32 34K—the first licensable multithreaded CPU core. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.") And if a customer wants multithreading *and* multiprocessing, MIPS already offers the MIPS32 1004K—the first licensable CPU with both of those features. (See *MPR 4/28/08-01*, "Multicore Multithreading With MIPS.")

This unique lineup of CPUs offers distinct tradeoffs. Whereas the 1074K is a deeply pipelined single-threaded CPU with superscalar issue and instruction reordering, the 1004K is a shorter-pipelined multithreaded CPU with single-issue in-order execution. The former processor wins hands down when a single thread dominates the application; the latter processor is the better choice for applications rich in data- or task-level parallelism. The 1004K uses only about half as much power, but it will finish a single-threaded task more slowly, so its power efficiency depends on the nature of the application.

The 1074K base core is almost identical to the MIPS32 74K, which *Microprocessor Report* covered in 2007. (See *MPR 5/29/07-01*, "MIPS 74K Goes Superscalar," which includes a block diagram, and *MPR 6/4/07-01*, "MIPS 74K Performance Update.") The most significant change is the instruction pipelines. Since introducing the 74K three years ago, MIPS has trimmed the pipelines to improve efficiency and has carried that improvement forward to the 1074K. The original 74K pipeline had 16 stages for ALU instructions and 17 stages for load/store and branch instructions. As Figure 2 shows, the 1074K and the latest revision of the 74K both have 14 stages for ALU instructions and 15 stages for load/store and branch instructions.

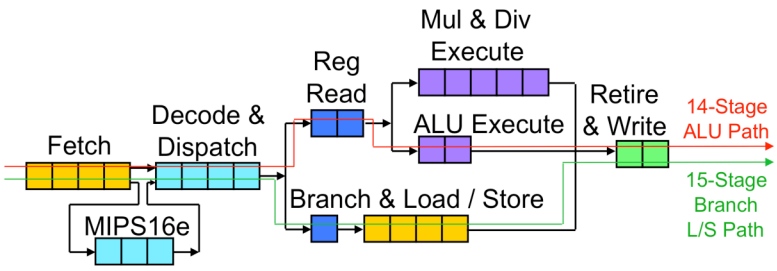

Figure 2. MIPS32 1074K pipeline diagram. MIPS trimmed two stages from the ALU and branch-load/store pipelines in the original MIPS32 74K processor of 2007. The 1074K pipelines are identical. MIPS says the slightly shorter pipelines are more efficient and have a negligible effect on clock frequency. (Source: MIPS)

As a synthesizable core, the 1074K has several features that developers can add, remove, or configure at design time. For example, adding a double-precision FPU transforms the 1074K into the 1074Kf, the floating-point variant of the processor. Developers can choose between a full-blown memory-management unit (MMU) or a simpler fixed-map translator (FMT). The optional CorExtend interface lets developers create application-specific instructions that augment the standard MIPS32 instruction set. (See *MPR 3/3/03-01*, "MIPS Embraces Configurable Technology.")

Superscalar issue varies with the CPU configuration. The 1074K can fetch up to four instructions per clock cycle but executes only two integer instructions per cycle. Those two instructions can be any ALU instruction and an integer branch or load/store instruction. In its 1074Kf configuration, the processor can additionally execute two floating-point instructions per cycle, so it becomes a four-issue superscalar machine. The two floating-point instructions must be an arithmetic instruction and a move instruction (to or from the integer registers). The 1074K can also execute instructions out of order for maximum efficiency, juggling up to 32 instructions at a time. With all these features, the 1074K is among the most powerful licensable CPU cores available, even in a uniprocessor configuration.

Off-the-Shelf Multiprocessing

The 1074K's signature option is cache-coherent SMP. Like the 1004K, its multithreaded cousin, the 1074K supports SMP designs having two to four CPUs. Both the 1004K and 1074K work with the MIPS Coherent Processing System (CPS), a block of licensable intellectual property (IP) that has all the essential logic for an SMP design. Of course, chip developers have always been able to link multiple CPUs incoherently with custom logic, but the CPS provides out-of-the-box support for shared-memory cache-coherent operating systems, like SMP Linux. (To build systems with more than four CPUs, developers can still use custom logic.)

Figure 3 shows a quad-core design with the CPS and another optional IP block, the MIPS "SOC-it" L2 cache controller. Each CPU has its own Open Core Protocol (OCP) port to a coherence fabric that weaves the cluster together. Most internal data paths are 256 bits wide. The CPU

cluster connects to the L2 controller and system over separate 256-bit-wide read and write interfaces. The cache coherence manager snoops the L1 caches in the background without disturbing a CPU's main pipeline until there's a cache hit. The coherence manager can hide the latency of snooping the L1 caches by issuing speculative reads to the L2 cache and main memory.

Additional elements of the CPS are a global interrupt controller, I/O coherence unit, cluster power controller, and debug logic. The interrupt controller routes external interrupts to the corresponding CPU and also allows CPUs to interrupt each other. The I/O unit is a hardware accelerator that keeps I/O traffic cache coherent: for example, when a peripheral DMA controller is moving data to and from the L2 cache or main memory.

The power controller supervises the CPU cluster's power gating, clocking, and system resets and is programmable via special registers. This controller can manage each CPU's sleep state individually, and it can wake up a sleeping CPU in response to external events or requests from another CPU in the same cluster. The CPS debug logic extends the MIPS PDtrace logic by allowing developers to trace the cluster's coherence-management functions.

Although using multiple CPU clusters in a chip design is possible, the CPS maintains coherence only among the two to four CPUs in each cluster. Given the superscalar, out-of-order 1074K's inherent horsepower, few (if any) consumer-system designs will need more than four of these CPUs. Carrier and enterprise networking designs might require larger numbers of 1074K CPUs, in which case developers would need to create a custom cache-coherent interconnect.

Another licensable alternative for larger multicore designs is IBM's PowerPC 476FP. It supports one or two clusters with up to eight coherent CPUs per cluster. With four-issue ALUs, dual-issue FPUs, and instruction reordering, it's even more powerful than the MIPS 1074K. The PowerPC 476FP's shorter nine-stage pipeline will hamper its maximum clock speed in a race with the 15-stage MIPS processor, but IBM offers the option of a prehardened core, which regains some ground on the fully synthesizable 1074K. (For our report on the PowerPC 476FP, see *MPR 2/16/10-01*, "The Rise of Licensable SMP.")

Preliminary Specs Look Good

This is not to say that the MIPS32 1074K is slow. On the contrary, MIPS touts it as the world's fastest fully synthesizable embedded-processor core—a claim somewhat dampened by ARM's recent announcement of Cortex-A15. Both companies predict, on the basis of simulations, that their newest CPUs will reach 2.5GHz (typical) in 28nm CMOS. But ARM's processor may require some structured IP to reach that clock frequency, whereas the MIPS32 1074K is fully synthesizable. SoC developers now starting projects with the 1074K will probably target 28nm unless they are cost conscious, in which case a 40nm process is a safer distance from the bleeding edge.

Table 1 shows the MIPS32 1074Kf's preliminary and estimated performance in TSMC's tried-and-true 40nm G process. Both implementations have two CPUs, an FPU, same-size L1 caches (32KB each), and the SMP logic described above. Both were synthesized with a vanilla TSMC 12-track cell library. The first implementation uses transistors with standard voltage thresholds (V_t); MIPS derived the performance numbers from preliminary RTL in a fully floor-planned model. The second pushes a little harder by mixing standard V_t transistors with some low-V_t transistors and TSMC's 10% voltage overdrive (VOD) option; MIPS estimated the resulting performance numbers. Both implementations assume realistic timing parameters.

The pushed implementation boosts the clock frequency by about 25%, although the standard implementation is certainly not a slowpoke at 1.2GHz. The benchmark scores scale linearly with clock speed. Total active power (which includes the L1 caches and SMP logic) jumps about 50% in the second implementation, as expected with a higher voltage and clock frequency. But the lower-threshold transistors aren't significantly larger, so the die areas of these two implementations are the same.

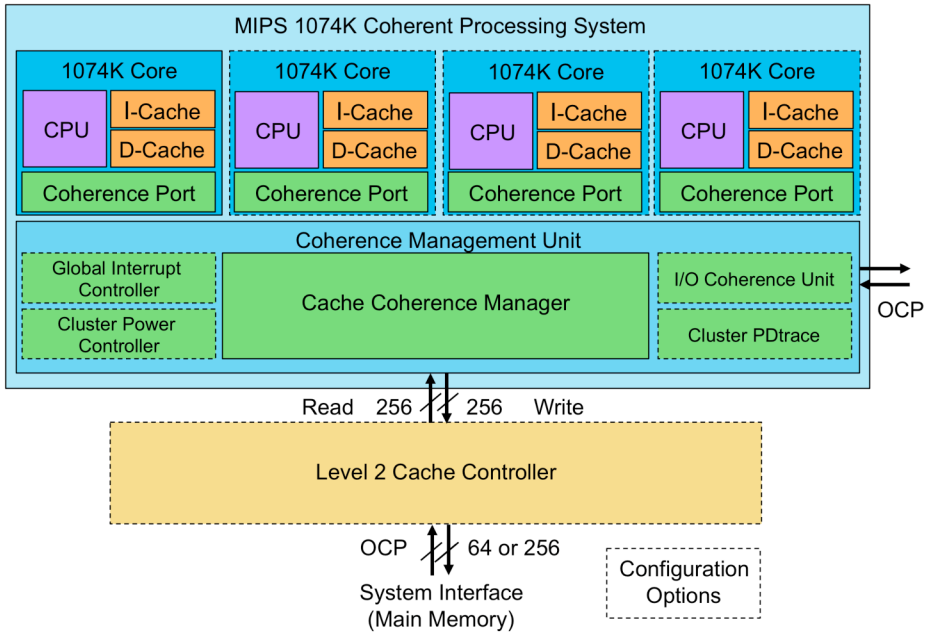

Figure 3. MIPS Coherent Processing System (CPS). This off-the-shelf IP supports cache-coherent SMP designs with two to four MIPS32 1074K or 1004K processor cores. The L2 cache controller is an optional IP block from MIPS. (Source: MIPS)

With some hand tuning, the 1074K should easily beat these performance estimates. Recently, MIPS announced that a MIPS32 74Kf processor—essentially, the uniprocessor version of the 1074Kf—exceeded 2.4GHz under typical conditions in TSMC's 40nm G process. MIPS's partner Open-Silicon optimized critical paths by using 159 new LV_t cells, 147 RV_t cells, and 147 HV_t cells. In addition, Open-Silicon optimized the floor planning, clock-tree synthesis, and circuit placement.

Even without these optimizations, it's impressive that a dual-core SMP configuration of the 1074Kf consumes only about 850mW (typical) at 1.2GHz. Qualcomm's dual-CPU Scorpion—a custom design that's compatible with ARM's Cortex-A8—consumes about 1.0W at 1.3GHz when fabricated in TSMC's 45nm LP process. That estimate, however, includes an L2 cache, which the MIPS configurations in Table 1 omit. Nevertheless, a single-CPU 1074K design should be suitable for a smartphone, and a dual-CPU design should be suitable for a tablet. Although MIPS's primary market is AC-powered consumer electronics, the 1074K may open a few doors into the mobile market, too.

1074K Closely Matches Cortex-A9

The MIPS 1074K competes directly with ARM's Cortex-A9 MPCore and forthcoming Cortex-A15 "Eagle." The two-year-old Cortex-A9 is the closest match because it, too, is designed for two- to four-way coherent SMP. Unfortunately, an apples-to-apples comparison is impossible because ARM commonly licenses Cortex-A9 as an optimized hard macro and hasn't published detailed specifications for a synthesizable soft core in current process technology.

	MIPS 1074Kf (Preliminary)	MIPS 1074Kf (Estimated)
IC Process	TSMC 40nm G	TSMC 40nm G
TSMC Cell Library	12-track standard V_t	12-track mixed V_t + 10% VOD
CPU Cores	2 CPUs	2 CPUs
CPU Freq (worst case)	1.2GHz	Up to 1.5GHz
CPU Power (active)	0.36mW/MHz per CPU	0.43mW/MHz per CPU
Total Active Power w/ CPS + L1 Caches	~850mW (typical)	~1.3W (typical)
Total Area	4.1mm^2	4.1mm^2
Dhrystone 2.1	4,800Dmips	6,000Dmips
CoreMark	6,100CM	7,650CM
JavaScript (SunSpider)	2.1 sec	1.7 sec

Table 1. MIPS32 1074Kf specifications in TSMC's 40nm G. Both of these dual-core implementations are identically configured with FPUs, L1 caches, and the MIPS Coherent Processing System (CPS). Although these preliminary and estimated results aren't yet carved in silicon, they show significant differences after minor implementation and process tweaks. For both implementations, performance realistically assumes worst-case slow/slow corner results with production margins of 10% on-chip variation and 25-picosecond clock jitter. (Source: MIPS)

Instead, ARM has published some data for a dual-CPU Cortex-A9 that's prehardened for TSMC's 40nm G process, the same process that the dual-CPU 1074Kf targets in Table 1. ARM cites two implementations: one optimized for clock speed and the other optimized for low power consumption. Both Cortex-A9 hard macros use ARM's SC12 cell library with high-performance extensions, whereas MIPS used a generic TSMC cell library to synthesize its portable soft macro. In other words, at the implementation level, this comparison is stacked heavily in ARM's favor.

In other respects, the ARM and MIPS implementations are closer. Both have 32KB L1 instruction and data caches and the coherence logic required for their dual-CPU configurations. Cortex-A9, however, includes ARM's powerful Neon extensions. The 1074Kf has Revision 2 of the MIPS DSP Application-Specific Extensions (DSP-ASE) and a respectable FPU, but they are inferior to Neon.

Even with the advantage of a hardened implementation, Cortex-A9 doesn't look faster than the 1074K. ARM says the hard macro will hit 2.0GHz (typical) in TSMC's 40nm G process, compared with 1.2–1.5GHz (worst case) for the MIPS soft CPU. Open-Silicon's tuned implementation of the nearly identical MIPS32 74Kf reached 2.4GHz (typical) in the same process—without overdrive. In a typical-typical comparison, therefore, a sprint between the 1074K soft core and Cortex-A9 hard core will be a close contest. MIPS estimates that a Cortex-A9 soft macro synthesized with TSMC's standard-cell library would run at about 950MHz. According to ARM, the power-optimized Cortex-A9 hard macro manages only 800MHz (worst case), so the MIPS estimate looks reasonable.

ARM claims 0.5W for the power-optimized Cortex-A9 and 1.9W for the speed-optimized implementation (total active power for dual CPUs with caches, coherence logic, and Neon). MIPS estimates 0.85W for the standard implementation in Table 1 and 1.3W for the speedy implementation (total active power for dual CPUs with caches, coherence logic, FPUs, and DSP-ASE). Overall, MIPS is estimating 0.70–0.86mW per megahertz versus ARM's 0.62–0.95mW per megahertz. That's quite good for MIPS, especially considering ARM's implementation advantages and reputation for making lower-power CPUs.

MIPS beats ARM in die area, too, which is unusual when comparing soft cores with hard cores. Both 1074Kf implementations in Table 1 are 4.1mm^2. The speed-optimized Cortex-A9 implementation is 6.7mm^2, and the power-optimized version is 4.6mm^2. ARM's area is no doubt inflated by its superior Neon extensions.

One Cortex-A9 advantage, at least in theory, is throughput—it can issue four instructions per cycle. Only

the FPU-equipped 1074Kf can do the same, and then only if the code frequently mixes integer and floating-point instructions. But actually, these two processors are more closely matched than they appear. Cortex-A9 can decode only two instructions per cycle, so it can't maintain its peak execution rate. Effectively, both CPUs are dual-issue machines when running integer code and will probably average 1.0 to 1.2 instructions per cycle.

On simple benchmarks such as Dhrystone and CoreMark, Cortex-A9 is up to 25% faster per megahertz than the 1074K. Comparing performance per watt doesn't reveal significant differences, however, because their power numbers are quite close, and we can't ascertain how rigorously each vendor measured power consumption. Cortex-A9 customers should be able to reach firmer conclusions, because that CPU is already in production, whereas the 1074K is just entering the chip-design process.

Cortex-A15 Ups the Ante

MIPS faces a tougher fight against ARM's newest CPU core, Cortex-A15 "Eagle." (See *MPR 9/13/10-01*, "ARM Launches Cortex-A15.") Although ARM disclosed more details about Cortex-A15 at the Linley Tech Processor Conference in September, a thorough comparison of that CPU with the MIPS 1074K must wait until ARM releases additional information, probably at its technical conference in November.

What's known is that Cortex-A15 is ARM's most powerful CPU to date. To begin with, it's a three-way superscalar machine with very wide execution bandwidth. Although it can fetch and decode only three instructions per clock cycle, it has enough function units to execute up to eight instructions per cycle. Two instructions can be simple ALU operations; two can be loads or stores; one can be a branch; two can be complex operations, such as SIMD or FPU instructions; and one can be a multiply-accumulate (MAC) instruction.

Having this wide array of function units and issue options, Cortex-A15 stands a better chance of sustaining its peak throughput rate of three instructions per cycle. ARM claims 3.5 Dhrystone mips (Dmips) per megahertz, which is 40% faster than Cortex-A9 and 75% faster than MIPS's estimate of 2.0 Dmips per megahertz for the 1074K.

Cortex-A15's pipeline is a departure for ARM, too. The first 12 stages fetch, decode, and dispatch instructions in order. Then, depending on the instruction type, the pipeline's back end has an additional 3 to 12 stages, and the CPU can freely reorder the instructions for optimal execution. As many as 60 instructions may be in flight. For simple ALU instructions, the pipeline is 15 stages deep, but some complex instructions will journey through 24 stages. This depth should give Cortex-A15 as much clock-frequency headroom as the MIPS 1074K. Indeed, ARM says the new CPU will reach the same target frequency of 2.5GHz in a 28nm CMOS process. MIPS, however, says the 1074K will reach that frequency when fully synthesized; at this time, it's unclear whether Cortex-A15 (like Cortex-A9) will need some prehardening to reach its target.

Cortex-A15 has more tricks up its sleeve. It's the first ARM CPU to support the Amba-4 interconnect, which can maintain system coherence among 32 or more CPUs on a chip. In fact, ARM says an SoC could integrate multiple clusters of Cortex-A15 cores while maintaining system-wide coherence. Backward compatibility with Amba-3 allows additional clusters of Cortex-A9 and Cortex-A5 CPUs. Within the Cortex-A15 clusters, ARM's SMP and power-management logic can dynamically repartition groups of CPUs to tackle different chores and can even power down some CPUs when they're not needed. New virtualization extensions—a first for licensable embedded processors—allow a hypervisor to run different operating systems on different groups of CPUs.

With its other new features, such as 40-bit physical-memory addressing and faster save and restore, Cortex-A15 will be stiff competition for MIPS when it debuts in December. Of course, such a muscular CPU will probably be larger and consume more power. ARM says that slower implementations will be suitable for mobile devices like smartphones, but the company hasn't released power-consumption data. *MPR* will analyze the tradeoffs when more technical information becomes available.

PowerPC Is Faster—at a Cost

As we noted in "The Rise of Licensable SMP," embedded-processor cores designed for cache-coherent multiprocessing are experiencing a growth spurt. Before 2008, the ARM11 MPCore was the only licensable example (excluding do-it-yourself projects). Then MIPS jumped in with the 1004K, followed by IBM with the PowerPC 476FP. Table 2 summarizes these processors but omits ARM's Cortex-A15 pending further information from the company. The table also omits the Cortex-A5 MPCore, which replaced the ARM11 MPCore and is intended for lower-performance, lower-power applications. (See *MPR 10/26/09-01*, "ARM's Midsize Multiprocessor.")

The PowerPC 476FP is a particularly powerful competitor. It supports coherence with up to eight CPUs per cluster—twice as many as MIPS. In addition, IBM's SMP logic supports two clusters with up to 16 CPUs, although coherence is limited to each cluster. Clock speeds reach 1.6GHz in IBM's 45nm silicon-on-insulator (SOI) process, making the 476FP the swiftest processor in this group.

Also, the 476FP is the widest superscalar machine in this group—each CPU can issue four ALU instructions per clock cycle. The 476FP can issue an additional two floating-point instructions per cycle, but the FPU shares the load/store pipelines with the ALUs, so the maximum throughput is four instructions per cycle. As noted, ARM's Cortex-A9 can issue four ALU instructions per cycle but decodes only two per cycle. The MIPS 1074Kf can issue

	MIPS 1074K / 1074Kf	MIPS 1004K / 1004Kf	IBM PowerPC 476FP	ARM Cortex-A9 MPCore
CPU Architecture	MIPS32 R2	MIPS32 R2	Power ISA v2.05	ARMv7 Cortex-A
Symmetric Multiprocessing	2–4 cores, all coherent	2–4 cores, all coherent	2–16 cores, 2–8 coherent	2–4 cores, all coherent
CPU Cluster System Bus	OCP-like, 256-bit read, 256-bit write	OCP-like, 256-bit read, 256-bit write	CoreConnect PLB6, 2x 128 bits	Amba-3 AXI, 2x 64-bit read, 2x 64-bit write
Intercore Coherence?	Yes	Yes	Yes	Yes
Coherent Cache Snoop	L1, optional L2	L1, optional L2	L1 and L2	L1, optional L2
Global Interrupt Control?	Yes	Yes	Yes	Yes
Coherent I/O Control?	Yes	Yes	Yes	Yes
Coherent Debug?	Yes	Yes	Yes	Yes
Multithreading	1 thread per CPU	1 or 2 threads per CPU	1 thread per CPU	1 thread per CPU
Integer Pipeline	15 stages	9 stages	9 stages	8 stages (9–11 clocks)
Superscalar Execution	2-issue int (1074K) + 2-issue FP (1074Kf)	Single issue	4-issue integer + 2-issue FP	2-issue integer
Instruction Ordering	Out of order	In order	Out of order	Out of order
L1 Cache (I + D)	0–64KB I-cache, 16–64KB D-cache	8–64KB each	32KB each	16–64KB each
L2 Cache	Optional, 128KB–1MB	Optional, 128KB–1MB	Configurable, 256KB–1MB	Optional, up to 2MB
Memory Management	MMU or FMT	MMU	MMU	MMU
FPU	Optional SP / DP (1074Kf)	Optional SP / DP (1004Kf)	SP / DP (Power ISA 2.05)	Optional SP / DP
16-Bit Instructions	MIPS16e	MIPS16e	None	Thumb-2
DSP / SIMD Extensions	Yes (MIPS DSP-ASE R2)	Yes (MIPS DSP-ASE)	Minimal (MACs)	Opt. (ARM SIMD, Neon)
Java Extensions	None	None	None	Jazelle RCT, optional Jazelle DBX
User-Defined Extensions	Optional (MIPS CorExtend)	Optional (MIPS CorExtend)	Not available	Not available
Execution Modes	User, supervisor, kernel	User, supervisor, kernel	User, supervisor	User, supervisor, system, TrustZone
Maximum Clock Frequency (worst-case)	1.5GHz*	1.3GHz*	1.6GHz†	800MHz‡–2.0GHz§
Dhrystone 2.1 per CPU	2.0Dmips/MHz	1.56Dmips/MHz	2.5Dmips/MHz	2.5Dmips/MHz
CoreMark 1.0 per CPU	2.55CM/MHz	2.92CM/MHz	Not available	2.88CM/MHz
CPU Core Area (w/ coherence)	2.1mm²* 32KB caches + FPU	1.0mm²* 32KB caches + FPU	3.6mm²† 32KB caches + FPU	2.3mm²‡–3.4mm²§ 32KB caches + Neon
CPU Power (typical)	0.43mW/MHz*	0.17mW/MHz*	1.0mW/MHz†	0.31mW/MHz‡ 0.48mW/MHz§
Production	September 2010	June 2008	December 2010	April 2008

Table 2. Key parameters for high-performance licensable 32-bit CPUs with cache-coherent SMP. To compare performance, this table shows implementations in similar fabrication processes to the extent possible, but some important differences are noteworthy. IBM's PowerPC 476FP is initially available only as a hard core for IBM's 45nm silicon-on-insulator (SOI) process; IBM plans to license a portable soft macro next year. *MPR* derived Cortex-A9 data from ARM's published specifications for two hard-macro implementations, as footnoted. *TSMC 40nm G speed-optimized soft macro; †IBM 45nm SOI hard macro; ‡TSMC 40nm G power-optimized hard macro; §TSMC 40nm G speed-optimized hard macro, typical conditions. (Source: vendors)

four instructions per cycle only if two are ALU operations and two are FPU operations.

Higher performance isn't free. Despite the PowerPC 476FP's implementation advantage—hard cores are almost always more efficient than soft cores—it's the largest CPU in this group and gobbles twice as much power as the MIPS32 1074K. The 1074K delivers better performance per watt. Another drawback of the 476FP is that the hard core is limited to manufacturing in IBM's fab. The future soft core, however, will be portable to other processes and foundries.

Another potential competitor, Intel's Atom, is an outlier. It's not licensed as a portable CPU core for SoC development and lacks a glueless solution for cache-coherent multiprocessing, except in the form of dual-core standard parts. Nevertheless, Intel's Atom-based SoCs will be off-the-shelf alternatives to building a multicore SoC around licensable processors from ARM, IBM, and MIPS. Until Intel further reduces the core area and power consumption, however, Atom isn't in the same league. Three MIPS 1074Kf CPUs with SMP logic are smaller and more power efficient than a single Atom core, and together they deliver more than twice the performance, according to CoreMark and Dhrystone.

1074K Broadens MIPS's Product Line

Developers of high-end networking gear and others seeking the highest possible performance must consider the PowerPC 476FP, which delivers more performance per CPU than the MIPS32 1074K and enables more CPUs per

cluster. But it's a moot point for networking vendors like Cavium and NetLogic, which license the MIPS architecture and design their own MIPS-compatible CPUs instead of using a ready-made core from MIPS Technologies. Cavium has SMP designs with up to 32 MIPS64-compatible CPUs per chip.

For most consumer products, one to four MIPS 1074K processors should be plenty, and the new CPU stacks up well against the competition. The 1074K definitely gives ARM's Cortex-A9 a run for the money, and it's clearly differentiated from its SMP-ready cousin, the simpler 1004K. Developers that are familiar with MIPS and have MIPS-based software can comfortably choose the 1074K over Cortex-A9.

Historically, ARM has dominated the market for low-power mobile processors while MIPS has dominated the higher-power consumer market. With their newest CPUs, both companies are now aiming for similar levels of performance and power consumption. But MIPS isn't reducing the performance and power of its product line to meet ARM. Instead, the mobile market's demand for higher performance is rising to meet MIPS.

The converging demand of these two markets is potentially beneficial for MIPS but is also hazardous. On the one hand, MIPS sees an opportunity to expand into the mobile market and has already signed a few lead customers, such as Mavrix. On the other hand, ARM is aggressively pursuing the consumer market with new high-performance CPU cores and with help from architectural ago with Cortex-A9 and is taking an even bigger one now with Cortex-A15. It may be easier for ARM to attract new customers in the consumer-electronics market than it is for MIPS to attract new customers in the mobile-electronics market. A typical DVR, for example, contains less software than does a smartphone, so there's less code to port from one CPU architecture to another.

With the addition of the 1074K, MIPS has a broad product line of licensable high-performance CPUs that is unmatched in the industry. Whether a target application needs single threading, multithreading, uniprocessing, multiprocessing, or a combination of these features, MIPS has a CPU that fits the bill. Their size, performance, and power consumption are competitive with those of other CPUs in their class. The 1074K will help MIPS defend its home turf in home consumer electronics against ARM's incursions and has the potential to win new business in mobile electronics as well. ♦

Price & Availability

MIPS Technologies began shipping production RTL for the MIPS32 1074K and 1074Kf embedded-processor cores in September. A lead licensee, which is anonymous for now, has been working with preproduction RTL. MIPS isn't publicly disclosing upfront license fees and royalties. For more information, visit *www.mips.com/products/cores/32-64-bit-cores/mips32-1074k*.