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MICROPROCESSOR REPORT

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GODSON-3 ADDS VECTOR EXTENSIONS

Chinese Hope New Processors Will Beat World's Top Supercomputers

By Tom R. Halfhill {9/27/10-02}

Aiming to build the world's fastest supercomputer using domestic technology, the Chinese Academy of Sciences is boosting the performance of its home-grown Godson microprocessors with powerful vector-processing units, new SIMD instructions, additional CPU cores, and a leap to 28nm technology. Within a few years, the Chinese hope, an all-native machine will rule the Top 500 list of the world's biggest iron.

Three new Godson chips are in development. Godson-3C will be the fastest new member of the family, as well as the most sophisticated Chinese microprocessor yet disclosed. Scheduled for production in 2012, it will be manufactured in a 28nm process and will have 16 CPU cores—twice as many as Godson-3B, another new processor, which achieved first silicon in a 65nm process this month. A third new chip, Godson-2H, is a smaller single-core design with integrated GPU, memory controller, and peripheral controllers. Intended for low-cost PCs, netbooks, and embedded systems, Godson-2H will also be manufactured in 65nm and is slated for production in 2H11.

All three new Godson-3 chips are compatible with the MIPS64 architecture but add 256-bit vector-processing units (VPUs), which replace the conventional 64-bit FPUs of previous Godson designs and other MIPS-compatible processors. Each CPU core has two of these VPUs, and each VPU can execute four multiply-accumulate (MAC) instructions per clock cycle. Among more than 300 new instructions are single-instruction, multiple-data (SIMD) operations that pack several operands into each register.

Like all Godson processors, the new chips are the spawn of a government-funded project to develop native high technology. Most design work is done at the Institute of Computing Technology (ICT) at the Chinese Academy of Sciences in Beijing. Finished designs are transferred to a Chinese corporation for manufacturing and sale, and the chips are marketed under the commercial name Loongson (or "Dragon") almost exclusively for domestic consumption. (The "Godson" name has an arcane backstory that makes more sense in China.) The latest incarnation of the Chinese marketing company is Loongson Technology, which has about 200 employees.

Godson's Steady Evolution

China launched the Godson project in 2001 as part of the National High-Technology Development 863 Program, a government-funded research and development plan to create native technology for Chinese industries. (The 863 Program derives its name from the month and year of its inception: March 1986.) Today, the Godson project is funded mainly as a National Science and Technology Major Project. Among other projects in this category are nuclear power plants, automated machine tools, and lunar spacecraft. The Godson project is led by Dr. Weiwu Hu, an ICT professor and member of the National People's Congress of China. (See the sidebar, "A Conversation with Godson's Father," in *MPR 7/25/05-01*, "China's Emerging Microprocessors.")

The project's overarching goal is to design world-class microprocessors unencumbered by market pressures and foreign export restrictions. Some Godson processors, such as the new Godson-3B and Godson-3C, are high-performance chips for supercomputers and servers. Supercomputers are at the forefront of science, technology, and military research, so the nation with the fastest machines has a better chance of finding the answers first. China already has the world's second-fastest supercomputer on the Top 500 list (*www.top500.org*), but it's built with Intel

Xeon CPUs and Nvidia Tesla GPUs, not with natively designed microprocessors.

Other Godson processors, like the new Godson-2H, are smaller designs for low-cost Linux-based PCs and embedded systems. These chips are intended for domestic consumer and industrial applications. In particular, China is building millions of inexpensive Linux PCs to improve computer literacy and accelerate the nation's progress toward a post-industrial economy. (See *MPR 6/26/06-02*, "China's Microprocessor Dilemma.")

The first member of the Godson family appeared in 2002. Godson-1 was a single-issue 32-bit design that was largely but not fully compatible with the MIPS-II architecture. (At that time, ICT had no license from MIPS Technologies.) Even this relatively simple design revealed the architects' ambitions by supporting out-of-order execution, a feature not seen in genuine MIPS-II processors.

Godson-1 was quickly followed in 2003 by Godson-2, which stretched the architecture to 64 bits (patterned after the MIPS-III architecture and again without a MIPS license). Godson-2 was a superscalar processor that increased the issue rate to four instructions per cycle and deepened the pipeline to nine stages. Since then, Godson evolution has been rapid, as Figure 1 shows. Although it's doubtful that Godson-3C will match the fastest server processors from AMD, IBM, and Intel when it debuts in 2012, China's supercomputer architects hope to reach the pinnacle of the Top 500 list by sheer brute force, no matter what the cost.

After years of wrangling with MIPS Technologies, ICT purchased MIPS32 and MIPS64 architectural licenses in 2009. These are full commercial licenses, not the limited academic licenses usually sold to universities. ICT can design 32- and 64-bit processors that are fully compatible with the MIPS32 and MIPS64 architectures, including instructions and other features that MIPS has patented in the U.S. and other countries. The newest Godson processors are legitimate and original MIPS64-compatible designs with proprietary extensions, much like the MIPS-compatible processors from Broadcom, Cavium, Marvell, NetLogic, and other MIPS architectural licensees. (See *MPR 7/13/09-01*, "China Gets Right with MIPS.")

New Chips Span the Spectrum

Weiwu Hu traveled from Beijing to present Godson-3B, Godson-3C, and Godson-2H during the Hot Chips Symposium at Stanford University last month. These new chips span the spectrum from a low-cost single-core SoC for PCs and embedded systems (Godson-2H) to much more powerful 8-core (Godson-3B) and 16-core (Godson-3C) designs for servers and supercomputers.

All three chips have the same basic feature in common: the new GS464V CPU core, which is almost identical to the GS464 core introduced in 2006. The GS464V replaces the conventional 64-bit FPUs with proprietary 256-bit VPUs that still support the MIPS64 floating-point instructions. The more than 300 new instructions include MAC and SIMD operations that accelerate media processing, FFTs, digital filtering, and even the Linpack floating-point benchmarks. (These new instructions are similar to the x86 Advanced Vector eXtensions, or AVX, which will debut next year in AMD's Bulldozer and Intel's Sandy Bridge processors.) The older GS464 core had the usual 32 registers per FPU, each being 64 bits wide. As Figure 2 shows, the new VPUs share a pool of 128 registers, each being 256 bits wide.

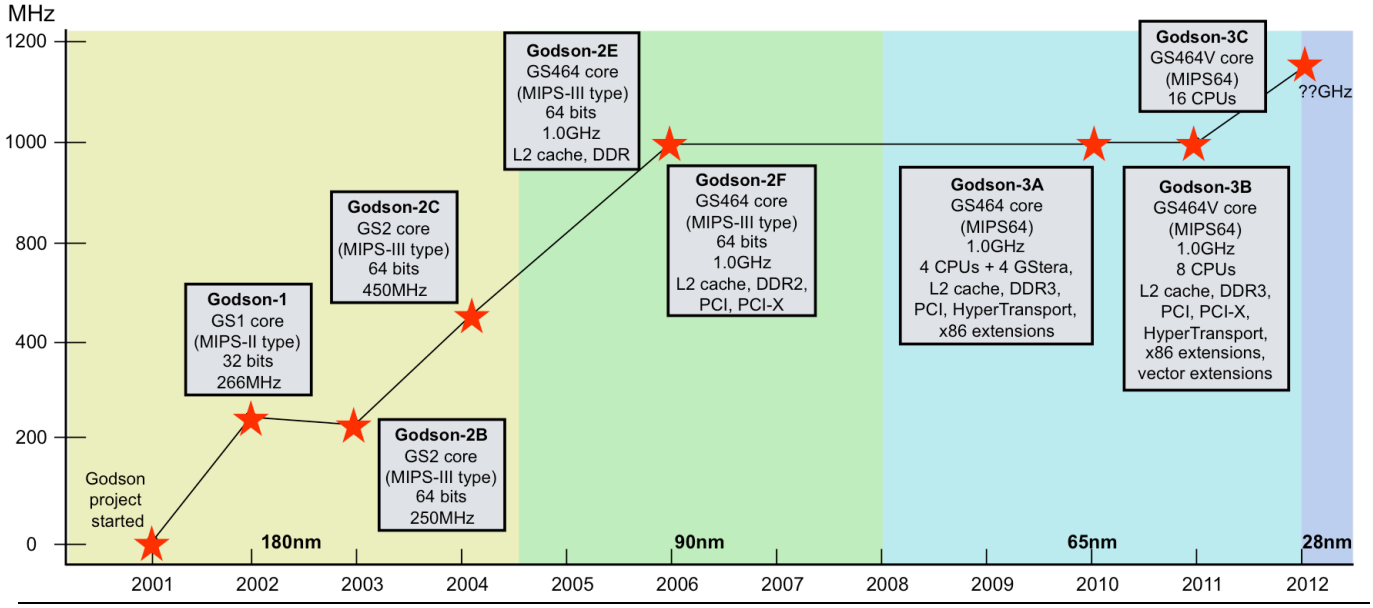

Figure 1. Milestones of Godson evolution. This chart shows major highlights of the Godson family since its inception in 2002; there are several variations of these processors. Some designs span more than one process technology. Dates are approximate and correspond to initial production. (Source: ICT and The Linley Group)

Each VPU can execute four MACs in parallel, so the GS464V can crunch eight MACs at a time for a total of 16 floating-point operations per clock cycle. Therefore, the maximum theoretical performance of the eight-core Godson-3B is 128 gigaflops at 1.0GHz. In comparison, today's Intel Xeons with Westmere-EP CPUs can execute only eight floating-point operations per cycle, but they can run at more than three times Godson-3B's clock speed.

Naturally, one cost of Godson's supercharged VPUs is a larger core. At 15mm^2 in 65nm bulk CMOS, the GS464V is 50% larger than the previous GS464 in the same process technology. The GS464V will almost certainly burn more power, too, though ICT hasn't disclosed CPU-level power consumption.

Keeping these hungry VPUs fed with data isn't easy. ICT is taking an unusual approach by using special DMA pathways that can bypass the L1 and L2 caches. The pathways are called Godson Super Links (GSLs), and the GS464V has three of them. A 128-bit-wide AXI interface connects the GSLs to the dual 64-bit memory controllers. Although the VPUs can load cached data in the usual fashion, the GSLs avoid data-dependent stalls after a cache miss, because the VPUs can immediately begin loading data from memory without waiting for the caches to refill.

To manage these direct links, the GS464V CPU has a DMA controller called a "memory-access coprocessor" or VECDMA (vector DMA controller), a proprietary controller that reorganizes incoming data for maximum efficiency before loading the vector registers. For example, a matrix-multiply instruction can operate more efficiently if the input operands are packed into the registers in a certain order; the DMA coprocessor makes it so. As Figure 3 shows, this coprocessor sits between the AXI interface, vector registers, and instruction pipelines.

DRAM Bandwidth Limits Performance

Bypassing the caches and going straight to memory can save time in some circumstances, but programs must use the detour sparingly. For one, initiating a burst read from DRAM will almost certainly require more clock cycles than hitting a cache. For another, memory bandwidth is a severe limitation of Godson-3B.

We don't know the latencies of Godson-3B's memory system, but we do have the specifications for Godson-3A: four clock cycles for the L1 data cache (for floating-point data), about 20 cycles for the L2 cache, and about 100 cycles for DRAM. Both Godson-3A and Godson-3B have virtually identical memory systems: 64KB L1 instruction and data caches (four-way set associative), 4MB of L2 cache (ditto), and dual 64-bit DDR3 memory controllers that run at a maximum of 400MHz (effectively 800MHz, using double-edge clocking). Godson-3B's memory latencies are probably similar, so the GSLs save time only if refilling and accessing the caches takes longer than going straight to memory.

Memory bandwidth is the other limitation. With DDR3-800 memory, Godson-3B has 12.8GB/s of bandwidth. DDR3-1600 memory would increase the bandwidth

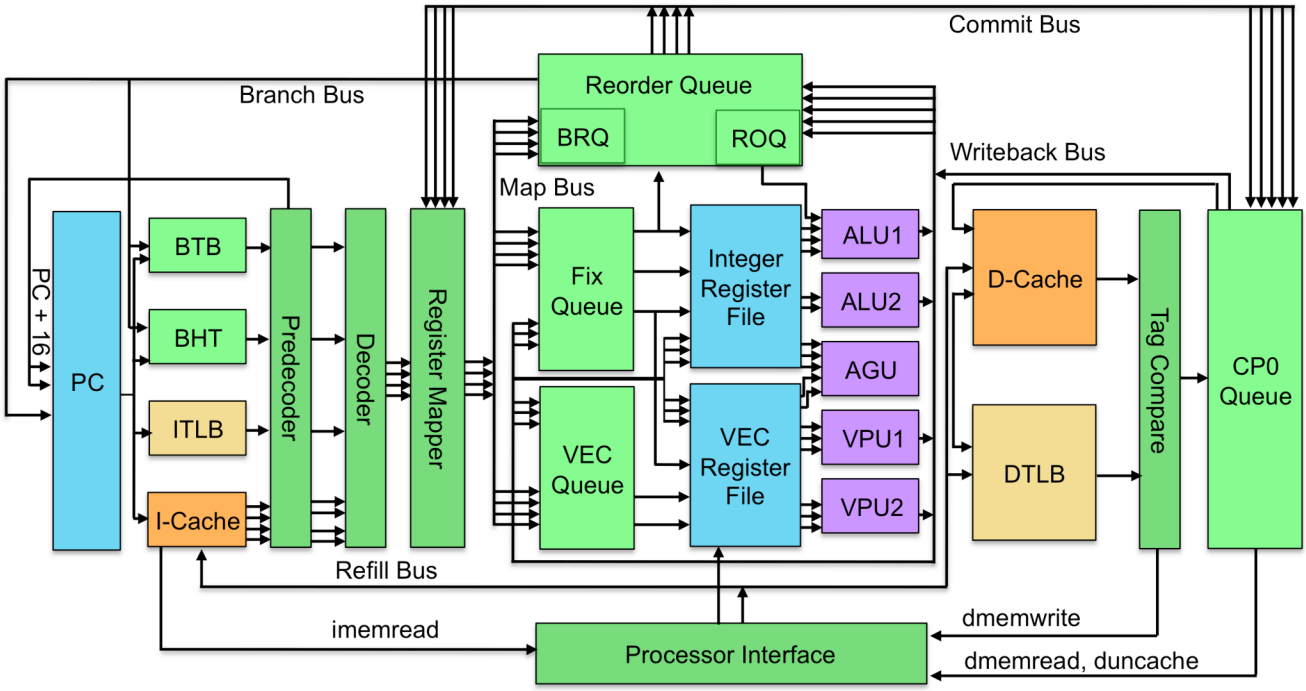

Figure 2. Godson GS464V block diagram. The main differences between this CPU core and the previous GS464 core are the new vector-processing units (VPUs) and their direct links to main memory, which can bypass the caches. ICT refers to this core as an XPU, combining the functions of a CPU, MPU (media-processing unit), GPU, and DSP. (Source: ICT)

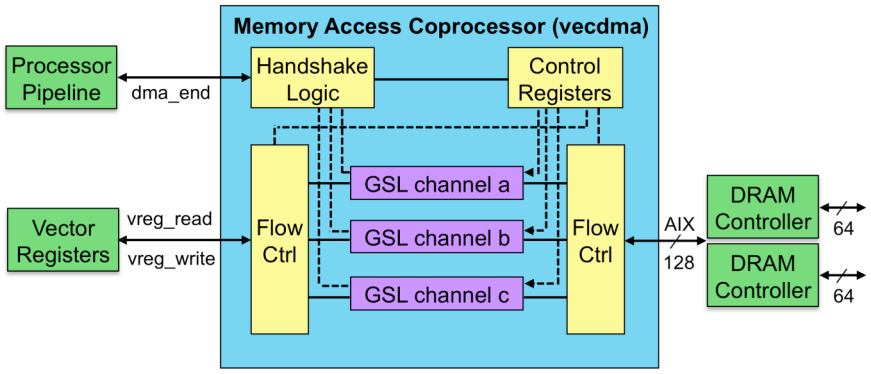

Figure 3. Godson's memory-access coprocessor. Another new feature of the GS464V, this proprietary DMA controller helps to feed the vector-processing units with data to prevent stalls after a cache miss. In addition to loading data directly from memory through three channels called Godson Super Links (GSLs), the controller performs flow control and rearranges the data for optimal vector processing. (Source: ICT)

to 25.6GB/s. But for even one GS464V to sustain 16 single-precision floating-point operations per cycle at 1.0GHz, it would need to load 128GB/s. Sustaining that rate with eight cores would consume 1TB/s—and we're not counting the additional bandwidth required to store results.

Consequently, Godson-3B can maintain peak performance for longer than brief spurts only by hitting the caches or by executing repetitive operations on relatively static data. Although many math-intensive algorithms do chew on the same data, this limitation makes Godson-3B primarily a number cruncher, not a data-flow machine. Of course, memory bandwidth restrains the performance of many microprocessors, not just that of Godson.

Nevertheless, according to ICT's simulations, Godson-3B achieves more than 93% of its peak theoretical performance when running the math-intensive components of the Linpack benchmark. The simulation uses an RTL model of the processor with eight GS464V cores, two DDR3 memory interfaces, and the new 64-bit MAC instructions. The same model surpasses 87% of its peak theoretical performance when calculating a 1,024-point floating-point FFT, completing the operation in 0.37 microseconds at a simulated clock speed of 1.0GHz. Using only one GS464V at the same frequency, the RTL simulation decodes H.264 video at 1080p resolution, surpassing 100 frames per second. The inner loops of these tasks often do perform repetitive operations on the same data.

Supercomputer Building Blocks

Like its immediate predecessor, Godson-3A, Godson-3B can be a building block for large systems. Using internal crossbars and external HyperTransport interfaces, mesh networks of Godson chips can scale to systems of almost any size. Clusters of processors can globally address each CPU's L2 cache. A hierarchical directory maintains cache coherence for clusters with up to 64 CPU cores—or for even larger clusters, depending on the implementation. Each physical CPU core can have its own directory entry. Alternatively, a group of CPU cores (called a "virtual core") can share a cache block.

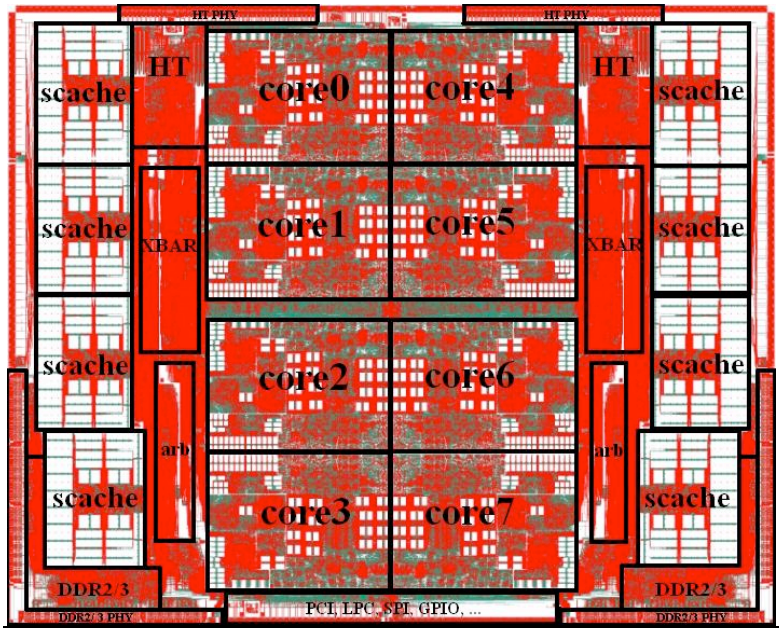

Figure 4. Godson-3B layout. This eight-CPU chip is the most powerful Godson processor to date. It's designed for servers, supercomputers, high-end embedded systems, and high-density signal processing. Although ICT says Godson-3B could enter production this year, that schedule seems optimistic. First silicon arrived from the fab in September. (Source: ICT)

As Figure 4 shows, Godson-3B is well integrated. In addition to eight CPUs and 4MB of L2 cache with ECC, it has two 64-bit DDR2/3 memory controllers with ECC, two 16-bit HyperTransport controllers (800MHz), a 32-bit PCI/PCI-X controller, and sundry other I/O interfaces (including UART, SPI, LPC, and GPIO). The 64KB L1 instruction cache is parity protected, and the 64KB L1 data cache has ECC. Fabricated in a 65nm bulk-CMOS process by ST-Microelectronics, Godson-3B measures 300mm^2 and typically consumes about 40W at 1.0GHz.

Godson-3B's most obvious limitation is its 65nm CMOS technology, which lags two generations behind Intel's newest 32nm high-*k* metal-gate (HKMG) technology. Godson chips have trouble breaking the 1.0GHz barrier, so they have relied more heavily on microarchitecture advancements (such as the new vector exten-

sions) to boost performance. In other words, they are brainiacs, not speed demons.

Although Godson-3B can execute twice as many floating-point operations per cycle as Intel's existing Xeon processors, Intel's superior fabrication technology more than compensates for the difference, and next year's Xeons will be much faster. Thanks to Intel's 32nm HKMG process, today's high-end Xeons reach a top speed of 3.46GHz. Consequently, the peak theoretical throughput of a six-core Xeon (Westmere-EP) is 166 gigaflops—30% more than an eight-core Godson-3B running at 1.0GHz.

Early next year, Intel will ship its new Sandy Bridge microarchitecture. An important feature is AVX, which adds more than 150 instructions to the existing Streaming SIMD Extensions (SSE), significantly boosting floating-point performance. Like Godson's vector extensions, AVX widens the floating-point data paths and registers to 256 bits, packing up to eight single-precision operands into each register. Floating-point performance will double, so Sandy Bridge will match the GS464V's peak throughput of 16 operations per cycle.

Intel hasn't announced Sandy Bridge clock speeds yet, but assuming the same 3.46GHz maximum frequency as today's Xeons, an eight-core Sandy Bridge with AVX could crunch 442 gigaflops—more than 3.4 times the performance of the eight-core Godson-3B. Intel demonstrated an eight-core Sandy Bridge chip at the Intel Developers Forum (IDF) in September. (See *MPR 9/27/10-01*, "Sandy Bridge Spans Generations.")

Yes, Even China Outsources

To build the world's fastest supercomputer using domestic technology, China must therefore resort to a greater extravagance of brute force. Only by knitting together many more Godson-3B processors can the Chinese overcome their current technical limitations of clock frequency and multicore integration.

The main obstacle is China's lagging fabrication technology. China outsourced Godson production to STMicro after reaching a licensing compromise with MIPS in 2007, before ICT obtained its own MIPS licenses in 2009. (See *MPR 4/23/07-01*, "Embedded Systems Conference Highlights.") STMicro continues to manufacture Godson chips at 65nm, severely restraining clock speeds—surely a frustration for Godson's ambitious designers.

Hence the planned move to 28nm technology for the next-generation Godson-3C, leapfrogging the 45nm and 32nm nodes. Although Hu revealed little about Godson-3C at Hot Chips, it appears to be a doubled version of the eight-core Godson-3B. It will have 16 CPU cores and twice as much L2 cache (8MB), and it's intended for the same high-performance computing applications. Godson-3C is scheduled for production in 2012 and is a better candidate for building a native supercomputer capable of topping the Top 500 list.

Apparently, ICT doesn't expect Chinese fabrication technology to become the state of the art by then, because Godson-3C production will be outsourced to STMicro again. Surprisingly, the backup plan is to cross the Taiwan Straits and use TSMC if STMicro can't deliver a 28nm process by 2012. TSMC began early 28nm production this year; Altera and Xilinx will begin using it for their FPGAs in 2011. For the Chinese, European foundry STMicro may be more politically correct than a Taiwanese foundry like TSMC, but any delay in STMicro's 28nm roadmap could push back Godson-3C's debut or force it to settle for inferior fabrication technology.

Single-CPU Godson-2H Cuts Costs

To promote China's strategy of building low-cost Linux PCs for schools, homes, and businesses, ICT has also designed a much simpler processor that combines elements of the Godson-2 and Godson-3 microarchitectures. As Figure 5 shows, Godson-2H integrates the new GS464V core with a GPU, memory controller, and several peripheral controllers. This chip will also be a useful SoC for embedded applications.

ICT hasn't disclosed many details about Godson-2H. It has a 1MB L2 cache and a DDR2/3 memory controller, plus USB, PCI Express, Serial ATA (SATA), and Gigabit Ethernet (GbE) interfaces. With on-chip AC97 audio and 2D/3D video, it's nearly a complete platform for entry-level desktop PCs and netbooks. ICT hasn't described the capabilities of the integrated GPU, but it's probably not in the same league as the ATI-derived GPU in AMD's Fusion

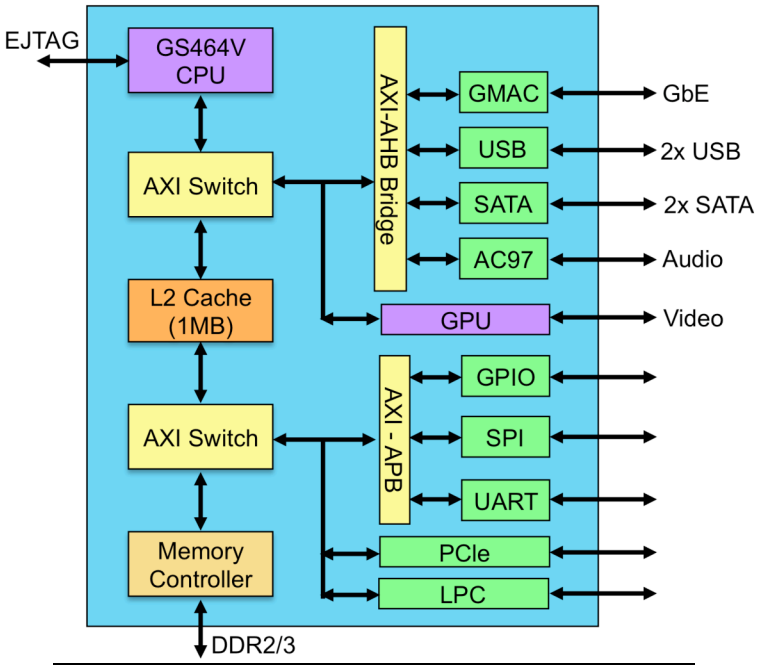

Figure 5. Godson-2H block diagram. This highly integrated processor is nearly a single-chip platform for Linux-based PCs. In concept, it's similar to AMD's "Ontario," the first GPU-integrated Fusion chip. (Source: ICT)

Price & Availability

Production is scheduled to commence in 4Q10 for Godson-3B (8 CPUs), in 2012 for Godson-3C (16 CPUs), and in 2H11 for Godson-2H (1 CPU). All three designs are being transferred to Loongson Technology for manufacturing and marketing under the Loongson/Dragon brand. No prices have been announced.

For more information about Loongson Technology, see *www.loongson.cn* (Chinese language).

For more information about the Institute of Computing Technology, Chinese Academy of Sciences, see *http://english.ict.cas.cn*.

chips. Like almost all other Godson chips manufactured in STMicro's 65nm process, Godson-2H's target clock speed is a pedestrian 1.0GHz. It's scheduled for production in 2H11.

Because Godson-2H has the same GS464V core as Godson-3B and Godson-3C, it supports the same 256-bit vector extensions, as well as the same "XBAR" x86 extensions that ICT announced with Godson-3A in 2008. The VPUs will be useful for media processing in PCs and consumer electronics; the x86 extensions help emulators run programs that haven't yet been ported to Linux and the MIPS architecture, easing the transition from Windows. (See *MPR 11/3/08-01*, "Godson-3 Emulates x86.")

Is Godson Aimed Too High?

Although Godson has made impressive progress in nine years, it hasn't achieved all the goals defined for it. In 2008, we reported China's ambition to build a supercomputer with performance exceeding one petaflops by 2010. China's Nebulae system broke that barrier this year, scoring 1.271 petaflops on the Linpack benchmark and capturing second place on the Top 500 list. As noted above, however, Nebulae is built with Xeon CPUs and Tesla GPUs. Of China's 24 supercomputers in the Top 500, none use Godson.

Nevertheless, a mere two years ago, China had only 12 supercomputers in the Top 500, and the fastest one ranked 111. Clearly, China is serious about topping this list and is committing enormous resources to the effort. By building world-class machines with imported technology, Chinese engineers are gaining vital experience. All they need is a Godson processor that's within spitting distance of Intel's fastest Xeon. Their biggest obstacles are China's laggard fabrication technology and a poorly optimized design that struggles to break 1.0GHz in 65nm. Even at 28nm, Godson's maximum clock speed will probably only double.

GS464V vector extensions are a partial attempt to circumvent those obstacles and match AVX. The Godson-3A of 2008 took a similar tack by supplementing its four CPUs with an equal number of proprietary floating-point coprocessors, which ICT dubbed "GStera" cores—Godson teraflops coprocessors. (We described GStera in our previously cited article, "Godson-3 Emulates x86.") We can't help noticing that Godson-3B and Godson-3C have dropped these coprocessors in favor of the new vector extensions and additional CPU cores. Evidently, GStera didn't deliver the goods.

Simply put, the Godson brainiacs desperately need more demon speed. Although architectural acrobatics can compensate for some clock-speed deficiency, Godson won't seriously challenge Xeon as long as its maximum frequency hovers around 1.0GHz. System designers can strive to compensate further by using more processors, but brute force has limits (and costs). Even if Godson-3C ships on time in 2012 and is fabricated in 28nm technology, processors such as Intel's Sandy Bridge, AMD's Bulldozer, and IBM's POWER will likely defend the summit of the Top 500 against a Godson-based challenger.

The Top 500 isn't everything, though. From a practical viewpoint, China can get all the processing muscle it needs by continuing to build world-class supercomputers with imported microprocessors. Godson can make a more substantial contribution at the other end of the CPU performance spectrum. By fostering a domestic industry of affordable PCs, consumer electronics, and efficient embedded systems, Godson can achieve a strategic national goal that's arguably better than winning a benchmark contest, prestigious though it may be. ♦