MOST SIGNIFICANT BITS

TEARS FOR TIER LOGIC

By Tom R. Halfhill {7/19/10-03}

FPGA startup Tier Logic looks doomed after failing to raise enough money to move its first chips into production. A last-ditch attempt to save the privately held company fell through last week, said Paul Hollingworth, vice president for marketing and sales.

Tier Logic, founded in Silicon Valley in March 2002, has spent about $20 million from its first-round investors and needs another $20 million to $30 million to bring its chips to market and reach breakeven, he said. Matrix Partners, the sole remaining investor, extended a bridge loan to keep Tier Logic alive for eight months during the search for additional funding, but that money is nearly gone, and the quest was unsuccessful. Another first-round investor, Walden International, pulled out last year.

Hollingworth said the situation is frustrating, because Tier Logic has operational samples of its first programmable-logic chips and has already taken orders from early customers. The company had planned to begin production by the end of this quarter.

Tier Logic's collapse will idle about 50 employees. Half are based at the company's headquarters in Santa Clara, California, and there's also a small sales office in Japan. The rest are in Colombo, the capital of Sri Lanka. Although few Silicon Valley companies employ engineers in that country, Hollingworth praised their talent and said their contribution was significant. Most were educated at the universities of Moratuwa and Peradeniya, the only technical colleges in Sri Lanka.

The company operated in stealth mode until March 10, when it announced its first TierFPGA and TierASIC devices. The FPGAs use a proprietary three-dimensional technology that puts the gate-configuration memory in an additional silicon layer. The configuration memory is SRAM implemented in thin-film transistors. By placing the configuration memory on top of the programmable fabric, Tier Logic can move the logic blocks closer together, reducing the chip's size, cost, and power. And by converting the SRAM layer into a hard-wired layer using a proprietary process, Tier Logic can turn a TierFPGA into a TierASIC without further development work by customers. (See the sidebar, "Another Three-Dimensional FPGA Debuts," in *MPR 3/29/10-01*, "Tabula's Time Machine.")

Tier Logic has won more than 50 patents for its technology. Those patents and other assets will probably be sold to a competitor for far less than the original investment. Competitors that stand to gain from Tier Logic's demise include programmable-logic newcomers Silicon Blue and Tabula, as well as the established market leaders, Altera and Xilinx. It's not surprising that Tier Logic couldn't survive on $20 million—a paltry bankroll for launching a semiconductor company these days. But it's a shame that the company's innovative technology will not reach the market. ♦