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FREESCALE P5 RAISES QORIQ'S I.Q.

New Networking Chips Will Exceed 2.0GHz, Debut 64-Bit CPU

By Tom R. Halfhill {7/5/10-01}

Freescale Semiconductor is making the leap to 2.2GHz and 64 bits. Although Intel and most MIPS-based competitors are already shipping 64-bit network processors, Freescale has stuck with the 32-bit Power Architecture CPUs that have been the cornerstone of its PowerQuicc line since the 1990s. Although Freescale will continue making 32-bit processors for years to come, its new P5-series chips in the QorIQ family will introduce a 64-bit Power Architecture core, which is capable of multigigahertz clock speeds.

QorIQ (pronounced "Core I.Q.") is eclipsing the popular PowerQuicc families of networking and communications processors (see *MPR 7/7/08-01*, "Freescale's Multicore Makeover"). At the recent Freescale Technology Forum in Orlando—back from hibernation after the Great Recession of 2009—the company announced three new QorIQ chips: the P3041, P5010, and P5020. These are the first P3- and P5-series chips in the QorIQ family, which is summarized in Table 1.

The P5 is the biggest news, because it represents for Freescale's customers the first increase in single-thread performance in more than four years. Its 64-bit Power e5500 CPU is scheduled to debut next year at 2.2GHz, nearly 50% faster than the current high-end MPC8572. Designed by Freescale, Power e5500 is a 64-bit extension of the company's 32-bit Power e500mc. The new CPU will bring higher performance to Freescale's product line, which is particularly valuable in control-plane applications, where Intel's x86 Xeon processors have been replacing PowerQuicc processors at important customers like Cisco. In addition, 64-bit addressing allows Power e5500 to access more physical memory for larger routing tables and other applications.

Freescale designed the single-core P5010 and dual-core P5020 processors mainly for control-plane duties in switches, security appliances, storage-area networks, and service-provider routers. They also serve industrial, aerospace, and military applications on single-board computers. Both processors will deliver their 2.2GHz speed while staying below 30W.

	P1 Series	P2 Series	P3 Series	P4 Series	P5 Series
Chips Announced	P1011, P1012, P1013, P1020, P1021, P1022	P2010, P2020	P3041	P4040, P4080	P5010, P5020
Sampling	4Q09–1Q10	1Q09	4Q10 (est)	4Q09, 3Q09	4Q10 (est)
Production	4Q10 (est)	2Q10	2H11 (est)	3Q10	2H11 (est)
CPU Cores	Power e500v2	Power e500v2	Power e500mc	Power e500mc	Power e5500
CPUs Per Chip	2 CPUs	1 or 2 CPUs	4 CPUs	4 or 8 CPUs	1 or 2 CPUs
CPU Freq (max)	800MHz	1.2GHz	1.5GHz	1.5GHz	2.2GHz
IP Forwarding	Up to 2Gb/s	Up to 4Gb/s	Up to 10Gb/s	Up to 20Gb/s	Up to 10Gb/s
On-Chip Network	PowerQUICC crossbar	PowerQUICC crossbar	CoreNet fabric	CoreNet fabric	CoreNet fabric
Power (max)	5W	8W	15W	30W	30W
Typical Applications	Integrated services routers, home-media hubs, NAS	Carrier-class VoIP gateways, wireless media gateways, base stations	Converged media gateways, SSL & IPsec firewalls, access gateways	Metro edge routers, IMS controllers, radio-network control, serving-node routers	Service-provider routers, network admission control, storage networks

Table 1. Freescale Semiconductor's QorIQ family. Freescale announced QorIQ in 2008 to supersede the MPC and PowerQuicc families of networking and communications processors. The latest announcements populate the previously empty P3 and P5 branches of the QorIQ family tree. (Source: Freescale)

By contrast, the new QorIQ P3041 processor has the same 32-bit Power e500mc CPU as do P4-series QorIQ chips. The P3041 is a quad-core design that's more power efficient and less expensive than the existing QorIQ P4040. The P3041 is intended primarily for integrated control- and data-plane duties in routers, enterprise switches, and wireless base stations. All the new P3 and P5 chips are scheduled to sample in 4Q10, with production slated for 2H11.

The P3 offers a new midrange point in the QorIQ line that will help defend against increasing multicore competition from Cavium Networks and NetLogic. The P5's improvement in control-plane performance is sure to please Freescale's current customers, but it leaves the door open to higher-power chips from Intel.

QorIQ Strengthens Freescale

Freescale announced the first six QorIQ processors in mid-2008 and has announced seven more QorIQ chips since then. Of these 13 chips, 4 are in production and 6 more are sampling. The newly announced chips are scheduled to reach the market in about a year. Of the five series in the QorIQ family, three series—the P3, P4, and P5—are built on a genuinely new foundation.

The P1 and P2 series are PowerQuicc-type designs renamed to fill a role as the low-end members of the QorIQ family. All P1 and P2 chips use the Power e500v2 CPU, which offers greater performance than the Power e300 CPU found in low-end PowerQuicc chips. The P1 and P2 have one or two CPUs per chip, versus one CPU in the low-cost PowerQuicc processors. They use the same PowerQuicc-style crossbar bus for the on-chip network that links CPUs with acceleration engines, I/O controllers, and other integrated components. Those components, however, are generally the same as those integrated in the P3, P4, and P5 series. Thanks to 45nm technology, the P1 and P2 greatly improve both performance per dollar and performance per watt compared with their 90nm predecessors.

The first QorIQ product built from the ground up is the eight-core P4080, which was announced in 2008. The P4080 remains the largest-scale multicore chip in the family. To support the larger number of CPUs, it has the newer Power e500mc ("multicore") CPU and the new CoreNet fabric, a more sophisticated on-chip network for complex designs. The P4080 was followed by the quad-core P4040, a similar design with half as many CPUs. The P4040 is the only other P4-series chip announced to date.

The P4040 and P4080 are Freescale's first chips with more than two CPUs, and they put the company squarely into the multicore market that has been dominated by Cavium and NetLogic. The P4080 is the first multicore networking processor with a high-performance switch fabric and three-level cache hierarchy—features that competitors are adopting in their next-generation (but as yet unsampled) multicore designs.

Freescale left the P3 and P5 series unpopulated when unveiling the QorIQ family in 2008 and promised to announce the first members of those branches later. Now Freescale has fulfilled that promise, although the new chips have yet to sample. Like P4-series chips, the quad-core P3041 is intended for applications requiring control- and data-plane processing on a single chip. The P5 series is intended to be the highest-performance branch of the QorIQ family for control-plane processing, although P5 chips retain some data-plane features.

When they enter production in 2H11, the P4 and P5 will be manufactured by Global Foundries or IBM in a 45nm silicon-on-insulator (SOI) process. Freescale skipped 65nm technology, beating Cavium and NetLogic to 45nm. Although Intel is manufacturing some PC and server processors in 32nm and plans to start 22nm production in 2011, the newest Xeon processors marketed for networking and communications are still manufactured in 45nm.

To stay in the control-plane game, high thread-level throughput is vital, and high clock speeds are the quickest way to get there. The maximum clock frequencies of the P5010 and P5020 chips are 2.2GHz. This limit holds power consumption below the 30W threshold that Freescale says its customers consider tolerable for their applications. The P5010 and P5020 have advantages over today's Xeon processors in performance per watt and integration, but because they won't ship for a year, Intel has some time to close the gap. Freescale says the Power e5500 core can reach 2.5GHz, albeit at higher power levels, so the company may release faster versions of the P5 processors in the future.

Stretching the e500mc to 64 Bits

The new Power e5500 core builds on the foundation of Freescale's Power e500v2 and Power e500mc 32-bit cores. All existing QorIQ P1-, P2-, and P4-series chips use the e500v2 and e500mc. The latter CPU, introduced in 2008, is a multicore variant of the e500v2 (see the sidebar, "The New, Improved Power e500mc Processor Core," in *MPR 7/7/08-01*, "Freescale's Multicore Makeover").

Freescale has been working on 64-bit CPUs for seven years. In 2003, before Freescale spun off from Motorola, the company began designing a 64-bit CPU, called PowerPC e700, that was intended for Apple computers. When Apple dumped PowerPC for the Intel x86, Freescale retargeted the e700 at embedded systems. The project was terminated in early 2008. Shortly thereafter, Freescale began retrofitting Power e500mc with the 64-bit features of the e700.

The resulting Power e5500 implements most, but not all, of the 64-bit extensions defined in version 2.06 of the Power Architecture instruction-set architecture (commonly known as Power ISA v2.06). This ISA is an outgrowth of the Power.org industry consortium that IBM founded in 2004 to promote the Power Architecture, which was formerly known as PowerPC. Freescale joined the open-membership

consortium in 2006 (see *MPR 3/6/06-01*, "Freescale Strengthens Power.Org," and *MPR 12/27/04-02*, "Bringing Power to the People").

Power.org released the Power ISA v2.06 specification in February 2009. It's the newest Power ISA, and it includes extensions defined for Freescale's Power e500mc and IBM's Power7 server processor. (IBM has been making 64-bit Power processors since Power3 in 1998.) Among other things, Power ISA v2.06 has a new subset of vector and scalar floating-point instructions (known as VSX) and new Book III-E embedded extensions for virtualization and hypervisors. Although Freescale's Power e5500 supports the Book III-E extensions, it doesn't support VSX.

In most respects, Power e5500 is similar to Power e500mc. Both CPUs have seven-stage, two-way superscalar pipelines for integer instructions, 32KB instruction caches, and 32KB data caches. Both support back-side L2 caches and front-side L3 caches. Power e5500 and e500mc have an additional privileged-execution mode not found in earlier designs, plus extended virtual addressing, privileged interrupts, atomic read/modify/write operations, larger cache lines (64 bytes), and optional cache stashing (which prefetches data into any level of cache without waiting for a load instruction to reference the data).

What's different? The Power e5500 CPU expands the 32-bit general-purpose registers to 64 bits; addresses up to 64GB of physical memory; allows back-side L2 caches of up to 512KB instead of 128KB; has newly optimized ALUs; has a new, faster FPU; and can switch between 32- and 64-bit modes under program control. The Power e500mc already had some 64-bit registers and a few instructions for manipulating them, so the new microarchitecture isn't a drastic change. Mode switching—if supported by the operating system—permits backward compatibility with 32-bit programs.

Freescale says integer performance has improved by 20% over the Power e500mc and by 25% over the Power e500v2. The Power e5500 delivers 3.0 Dhrystone MIPS per megahertz, versus 2.5 DMIPS per megahertz for Power e500mc. One reason is the 64-bit architecture, which can move twice as much data per clock cycle, improving Dhrystone throughput by 10%. Freescale attributes the rest of the improvement to optimized software libraries for string compares and other operations; faster divides and register operations in the ALUs; and better branch prediction through implementation of a link stack.

The FPU in Power e5500 is twice as fast at single-precision math and four times faster at double precision than the FPU in Power e500mc. One reason for the difference is that Power e5500's FPU runs at the full CPU-core frequency, whereas Power e500mc's FPU runs at half the CPU frequency. In addition, Freescale tweaked the double-precision floating-point instructions in Power e5500 to double their throughput per clock cycle.

In other respects, the FPUs in Power e5500 and Power e500mc are the same. Both are conventional FPUs, unlike the Power e500v2's signal-processing engine (SPE), which was derived from the AltiVec vector-processing engine. So far, QorIQ processors support neither AltiVec nor VSX, so they lack the vector-processing instructions found in either instruction set. Freescale has expressed no plans for supporting AltiVec in future products, although it may add VSX if customers need it.

Power Consumption Limits Speed

Freescale pitches Power e5500 as a higher-performance alternative for control-plane software running on single-core or multicore processors. Choosing to emphasize performance per watt over peak performance, Freescale limits maximum power consumption of the P5010 and P5020 to less than 30W, a level appropriate for tightly packed systems with small fans or passive cooling. Customers with larger systems that can safely exceed that threshold may look elsewhere for their processors. Figure 1 is a block diagram of the dual-core P5020.

Table 2 compares the P5010 and P5020 with four existing chips in Freescale's product line. All stay below 30W or thereabouts. Two of them—the MPC8641D and PowerQuicc III MPC8572E—are candidates for replacement by the new chips. They were cutting-edge technology a few

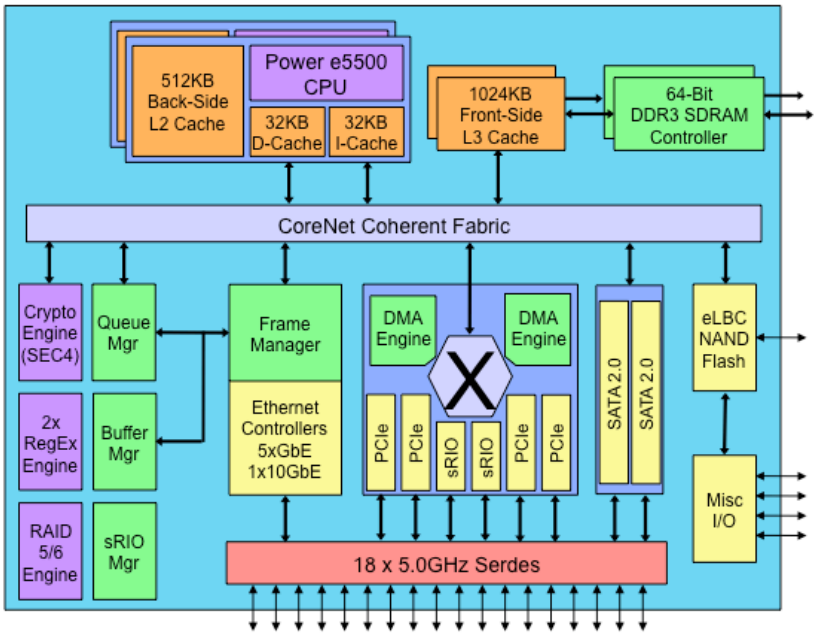

Figure 1 Freescale QorIQ P5020 block diagram. With two of Freescale's new 64-bit Power e5500 CPU cores, the P5020 is a highly integrated control-plane processor with some data-plane acceleration. The P5010 is a single-core version.

years ago, but their older 90nm SOI process limits them to a maximum clock speed of 1.5GHz. Their on-chip networks are less sophisticated than the QorIQ family's CoreNet fabric, but their shared buses are sufficient for single- and dual-core designs. Note that Freescale has been shipping a 1.7GHz Power processor (the MPC7448) since 2005, so the 2.2GHz P5010 and P5020 represent the first boost in single-thread performance in five years. The single-core MPC7448, like the MPC8641, uses Freescale's Power e600, a 32-bit CPU that is more powerful than Power e500 (see *MPR 7/5/05-01*, "PowerPC Ain't Dead Yet").

The other two chips in this table—QorIQ P4040 and QorIQ P4080—are now entering production and represent multicore 32-bit alternatives to the 64-bit P5010 and P5020. The P4040 and P4080 compensate for their lower clock speed by offering more CPUs—four or eight, versus one or two in the P5010 and P5020. The P4 chips also have faster pattern-matching engines and faster cryptography accelerators. Freescale considers the P4040 and P4080 more suitable for systems that shoulder both control- and data-plane duties, mainly because additional CPUs provide more opportunities for packet-level parallel processing.

By contrast, the single-core P5010 and dual-core P5020 are better suited for control-plane software, which is less parallelizable. Nevertheless, they retain the data-plane acceleration engines found in other QorIQ (and many

	QorIQ P5010	QorIQ P5020	QorIQ P4040	QorIQ P4080	PowerQUICC III MPC8572E	MPC MPC8641D
CPU Type	Power e5500	Power e5500	Power e500mc	Power e500mc	Power e500v2	Power e600
Arch. Width	64 bits	64 bits	32 bits	32 bits	32 bits	32 bits
Pipeline	7 stages	7 stages	7 stages	7 stages	7 stages	7 stages
CPUs Per Chip	1 CPU	2 CPUs	4 CPUs	8 CPUs	2 CPUs	2 CPUs
CPU Freq (max)	2.2GHz	2.2GHz	1.5GHz	1.5GHz	1.5GHz	1.5GHz
L1 Cache (I / D)	32KB / 32KB per CPU	32KB / 32KB per CPU	32KB / 32KB per CPU	32KB / 32KB per CPU	32KB / 32KB per CPU	32KB / 32KB per CPU
L2 Cache	512KB	512KB per CPU	128KB per CPU	128KB per CPU	1MB shared	1MB per CPU ECC
L3 Cache	1MB ECC	2MB shared, ECC	2MB shared	2MB shared	—	—
Coherent On-Chip Bus	QorIQ CoreNet	QorIQ CoreNet	QorIQ CoreNet	QorIQ CoreNet	PowerQUICC crossbar	PowerQUICC crossbar
Memory Controller	DDR3 / 3L 1 x 32 / 64 bits Up to 1.3GHz ECC	DDR3 / 3L 2 x 32 / 64 bits Up to 1.3GHz ECC	DDR2 / DDR3 2 x 64 bits Up to 1.3GHz ECC	DDR2 / DDR3 2 x 64 bits Up to 1.3GHz ECC	DDR2 / DDR3 2 x 64 bits Up to 800MHz ECC	DDR2 2 x 64 bits Up to 600MHz ECC
DMA Controller	2 x 4 channels	2 x 4 channels	2 x 4 channels	2 x 4 channels	2 x 4 channels	1 x 4 channels
PCI Express	4 x PCIe	4 x PCIe	3 x PCIe	3 x PCIe	3 x PCIe	2 x PCIe
Ethernet Controllers	5 x GbE 1 x 10GbE	5 x GbE 1 x 10GbE	8 x GbE 2 x 10GbE	8 x GbE 2 x 10GbE	4 x GbE 1 x 10GbE	4 x GbE
Serdes	18 lanes	18 lanes	18 lanes	18 lanes	12 lanes	16 lanes
Serial RapidIO	2 x sRIO	2 x sRIO	2 x sRIO	2 x sRIO	1 x sRIO	1 x sRIO
Frame Manager	1	1	2	2	—	—
Other I/O	2 DUARTs, 4 x I^2C, SPI	2 DUARTs, 4 x I^2C, SPI	2 DUARTs, 4 x I^2C, SPI	2 DUARTs, 4 x I^2C, SPI	1 DUART, 2 x I^2C	1 DUART, 2 x I^2C
USB 2.0	2 with PHYs	2 with PHYs	2, no PHYs	2, no PHYs	—	—
Serial ATA	2 x 3Gb/s	2 x 3Gb/s	—	—	—	—
RAID Engine	RAID5/6	RAID5/6	RAID5	RAID5	RAID5	—
SD / MMC	Yes	Yes	Yes	Yes	—	—
Crypto Accel	Yes	Yes	Yes	Yes	Yes	—
RegEx Engine	Yes	Yes	Yes	Yes	Yes	—
Real-Time Debug	Yes	Yes	Yes	Yes	—	—
IC Process	45nm SOI	45nm SOI	45nm SOI	45nm SOI	90nm SOI	90nm SOI
Voltage (CPU)	1.1V	1.1V	0.9–1.1V	0.9–1.1V	1.1V	1.1V
Power (max)	22W*	30W	21W	30W	39W	32W*
Package	FC-PBGA 1,295 pins	FC-PBGA 1,295 pins	FC-PBGA 1,295 pins	FC-PBGA 1,295 pins	FC-PBGA 1,023 pins	FC-CBGA 1,023 pins
Sampling	4Q10 (est)	4Q10 (est)	4Q09	3Q09	2Q07	1Q06
Production	2H11 (est)	2H11 (est)	2H10 (est)	2H10 (est)	3Q08	4Q07
List Price	$150*	$225*	$250*	$400*	$142–$189	$374–$450

Table 2 Comparison of Freescale's new QorIQ P5 chips with existing Freescale chips. The most notable feature of the P5 series is the new 64-bit Power e5500 CPU; all of Freescale's other Power Architecture chips have 32-bit CPUs. Also, the P5010 and P5020 are clocked at 2.2GHz—46% faster than the maximum clock speeds of the existing chips. (Source: Freescale, except *The Linley Group estimate)

PowerQuicc) chips. In pure control-plane applications, some of these engines are not needed. The RAID accelerators and Serial ATA (SATA) interfaces, however, position the P5 for high-end RAID controllers, storage-area network (SAN) devices, and network-attached storage (NAS) equipment.

To save board space in tight system designs, the P5010 and P5020 integrate additional features. Their dual USB 2.0 controllers have on-chip physical-layer (PHY) interfaces, whereas the P4 chips require external PHYs. The P5 chips have two SATA interfaces and acceleration logic for RAID6—features missing from the P4040 and P4080. And the P5 chips have four PCI Express interfaces (Gen 2), versus the three such interfaces of their P4 brethren. Otherwise, the QorIQ P4 and P5 series are much the same, preserving pin compatibility and software compatibility (in 32-bit mode). Both series are better integrated than the older PowerQuicc designs.

P5 Outruns Competitors

Table 3 compares the P5010 and P5020 with potential competitors from Cavium, Intel, and NetLogic. The Cavium Octeon II CN6320 and NetLogic XLS608 are the most similar rivals, because they integrate most of the same I/O interfaces, peripherals, and accelerators needed for networking and communications. Intel's entry is Xeon LC3528, a recent introduction formerly code-named Jasper Forest. A two-chip set, the Xeon product is less integrated than competing processors.

	Freescale QorIQ P5010	Freescale QorIQ P5020	Cavium Octeon II CN6320	Intel Xeon LC3528	NetLogic XLS XLS608
CPU Type	Power e5500	Power e5500	cnMIPS64-R2	x86 Core i7	MIPS64-R2
Arch. Width	64 bits	64 bits	64 bits	64 bits	64 bits
Pipeline	7 stages	7 stages	9 stages	16 stages	10 stages
Issue Rate	2 per cycle	2 per cycle	2 per cycle	3 per cycle	1 per cycle
CPUs Per Chip	1 CPU	2 CPUs	2 CPUs	2 CPUs (4 threads)	2 CPUs (8 threads)
CPU Freq (max)	2.2GHz	2.2GHz	1.5GHz	1.73GHz	1.2GHz
L1 Cache (I / D)	32KB / 32KB per CPU	32KB / 32KB per CPU	37KB / 32KB per CPU	32KB / 32KB per CPU	32KB / 32KB per CPU
L2 Cache	512KB ECC	512KB per CPU ECC	2MB shared ECC	256KB per CPU ECC	1MB shared ECC
L3 Cache	1MB, ECC	2MB shared, ECC	—	4MB shared	—
Memory Controller	DDR3 / 3L 1 x 32 / 64 bits Up to 1.3GHz ECC	DDR3 / 3L 2 x 32 / 64 bits Up to 1.3GHz ECC	DDR3 1 x 64 bits Up to 1.6GHz ECC	DDR3 2 x 64 bits Up to 1.06GHz ECC	DDR2 2 x 64 bits / 4 x 32 bits Up to 800MHz ECC
PCI Express	4 x PCIe	4 x PCIe	2 x PCIe	4 x PCIe	4 x PCIe
Ethernet Controllers	5 x GbE 1 x 10GbE	5 x GbE 1 x 10GbE	4 x GbE or 1 x 10GbE	1 x GbE†	8 x GbE
Serdes	18 lanes	18 lanes	12 lanes	16 lanes	12 lanes
Serial RapidIO	2 x sRIO	2 x sRIO	1 x sRIO	—	4 x sRIO
Other I/O	2 DUARTs, 4 x I^2C, SPI	2 DUARTs, 4 x I^2C, SPI	2 UARTs, 2 x I^2C	SPI†	2 UARTs, 2 x I^2C
USB 2.0	2 with PHYs	2 with PHYs	2 with PHYs	12†, no PHYs	2, no PHYs
Serial ATA	2 x 3Gb/s	2 x 3Gb/s	—	6 x 3GB/s†	—
RAID5/6 Engine	Yes	Yes	Yes	Yes	—
Other I/O	SD / MMC	SD / MMC	CompactFlash	PCI†, GPIO†, audio†	Flash
Crypto Accel	Yes	Yes	Yes	—	Yes
RegEx Engine	Yes	Yes	Yes	—	—
IC Process	45nm SOI	45nm SOI	65nm G	45nm high-*k*	90nm G
Voltage (CPU)	1.1V	1.1V	Not disclosed	Xeon: 1.99V* I/O hub: 1.05V	1.2V @1.2GHz
Power	30W max	30W max	17W max	Xeon: 35W TDP I/O hub: 5W	20W max
Package	FC-PBGA 1,023 pins 37.5mm	FC-PBGA 1,023 pins 37.5mm	FC-BGA 900 pins 31mm	Xeon: FC-LGA 1,366 pins 42.5 x 45mm I/O hub: FC-BGA 951 pins, 27mm	BGA 957 pins
Production	2H11 (est)	2H11 (est)	2H11 (est)	2Q10	2007
List Price	$150*	$225*	$59*	Xeon: $302 (1ku) I/O hub: $31 (1ku)	$150*

Table 3 Comparison of Freescale's QorIQ P5 series with competitors. All are 64-bit processors, like QorIQ P5010 and P5020. The Xeon processor requires a second chip to provide the I/O features built into the other chips. †Requires Intel BD3420 I/O hub. (Source: vendors, except *The Linley Group estimate)

Cavium's CN6320 is a dual-core member of the Octeon II family; some members of this family have as many as six CPUs. The CN6320 lags behind Freescale's P5 chips in clock speed (1.5GHz versus 2.2GHz), probably because it's manufactured in a 65nm bulk-CMOS process, which is a generation behind Freescale's 45nm SOI. Octeon II chips have dual-issue superscalar CPUs, but they execute instructions strictly in order, unlike the out-of-order Power e5500, giving the Freescale chips a theoretical advantage in instructions per cycle. On the other hand, the dual-core CN6320 uses much less power than the dual-core P5020—only 7W maximum, versus Freescale's estimate of "less than 30W." Cavium's six-CPU CN6335 is rated at only 17W maximum, but throwing four more CPUs at a control-plane instruction stream probably wouldn't help.

Freescale's P5020 burns more power not only because it's faster, but also because it's better equipped. For example, its SATA controllers make the P5020 a superior solution for storage applications. Also, the P5020 has 3MB of L2 and L3 cache—50% more cache than the CN6320. Overall, the P5020 is better suited to larger chores than is the CN6320, but at the cost of higher power consumption and a much higher price, according to our estimates.

NetLogic's dual-core XLS608 is by far the oldest and weakest design in this group, having entered production in 2007. It's based on a single-issue MIPS64-compatible CPU with in-order execution. It can manage four threads per CPU, but that's more threads than most control-plane software can put to good use. Whereas all the other chips support DDR3 memory at speeds exceeding 1.0GHz, the XLS608 stops at 800MHz DDR2. It's the only chip in this group without 10G Ethernet, though it partially compensates by offering a few more Gigabit Ethernet controllers. It has no SATA controllers, no RAID acceleration, and no USB PHYs.

The aging XLS608 is nearing obsolescence, but we include it because NetLogic hasn't replaced it yet. The new XLP family has the latest bells and whistles and is much better positioned to compete with Freescale's P5 processors. The first XLP design, however, is a large eight-core chip intended for applications that are different from those of the single-core P5010 and dual-core P5020. A single- or dual-core XLP would make trouble for Freescale. We expect NetLogic to announce and perhaps sample such chips before the P5 chips sample later this year.

Intel's Two-Chip Solution

Intel's Xeon LC3528 is the least-integrated chip in this group, even though it's the most recent. Other than four PCI Express interfaces and RAID acceleration, it has almost none of the features built into today's networking and communications processors, because it's based on one of Intel's server processors. The Xeon chip needs Intel's separate BD3420 "platform controller hub" to provide most of the I/O controllers and accelerators that are standard in other chips.

Intel's leadership in fabrication technology—the LC3528 is manufactured in Intel's 45nm high-*k* metal-gate process—allows Jasper Forest to achieve clock frequencies of up to 2.4GHz. The LC3528's speed, however, is limited to reduce power consumption. The LC3528 normally runs at 1.73GHz and can reach 1.87GHz in Turbo Mode. The lower frequency is the sustainable speed, which is more important for networking. Both speeds are well below those of Freescale's 2.2GHz P5010 and P5020. Those chips aren't scheduled to enter production until 2H11, however, whereas the LC3528 is available now. By 2H11, Intel will almost certainly use its 32nm process to manufacture faster embedded processors that consume less power.

Until then, the LC3528 has some architectural advantages to compensate for its lower clock frequency. Intel's Hyper-Threading technology can run two threads on each CPU, and those CPUs have triple-issue out-of-order pipelines, so they are capable of wider superscalar execution than the dual-issue Power e5500. Of course, those features (and the x86 architecture) come at a price. With a thermal design power (TDP) of 35W (plus 5W TDP for the I/O hub), the LC3528 is the hottest alternative in this group. It's also expensive, costing $302 for the CPU chip plus $31 for the hub.

Conspicuously missing from this comparison is AppliedMicro (formerly known as AMCC), Freescale's only serious Power Architecture competitor. Last fall, AppliedMicro announced a potential contender, the dual-core APM83290 processor. But in June, AppliedMicro told *Microprocessor Report* that the APM83290 has been canceled as a product (see *MPR 7/5/10-02*, "AppliedMicro Sinks Titan-IC"). For now, at least, AppliedMicro has nothing to match QorIQ P5020.

Assuming they ship on time, Freescale's P5010 and P5020 will be very good control-plane processors for applications below 30W. Cavium's fastest dual-core chip is much slower for pure control-plane applications requiring high single-thread performance. Intel's solution requires two chips, gives up some clock speed, burns more power, and is expensive. NetLogic needs a smaller member of its new XLP family to compete in this derby. For existing Freescale customers in particular, the P5010 and P5020 will be excellent upgrades.

P3041 Inaugurates P3 Series

Whereas the P5 series establishes a new high end for control-plane processing within the QorIQ family, the new P3 series fills a small gap between the existing P2 and P4 series. Like those chips, the P3 is suited for data-plane applications and other applications that mix control- and data-plane processing on one chip. So far, the sole member of the P3 series is the new quad-core P3041, which uses Freescale's 32-bit Power e500mc CPUs instead of the 64-bit Power e5500. The P3041 doesn't explicitly replace any existing chips in Freescale's large product catalog, but it's a logical upgrade from some PowerQuicc III processors.

The P3041 is an economy-model alternative to the similar QorIQ P4040, another quad-core design. Actually, the P3041 and P4040 are so similar that they could be members of the same series; Freescale is slicing its product branding very thinly here. Freescale derived the P4040 from the eight-core P4080, so it's more heavily equipped. It has three more Ethernet controllers, an additional frame manager, an additional memory controller, and twice as much L3 cache. It has one less PCI Express controller, no SATA, and no USB PHYs, however. Also, the P3041's serial RapidIO controller supports IEC Type 11 messaging and is four times faster at Type 9 messaging. In addition, the P3041 adds some hardware support for virtualization.

Surprisingly, the P3041 consumes about 20% to 30% less power than the P4040. Freescale says the P4040 consumes 21W maximum and less than 15W typical, versus the P3041's 15W maximum and less than 12W typical. Whereas the P4040 was a first-generation QorIQ design cut down from the eight-core P4080, the P3041 is a second-generation design with an optimized CoreNet fabric, better layout, a smaller L3 cache (1MB versus 2MB), one less memory controller, and one less frame manager. Also, Freescale says the P3041's cache subsystem has better power management.

The P3041's pin compatibility with and architectural similarities to the P4040 allow customers to design lower-power, lower-cost systems without starting from scratch. (Freescale hasn't announced pricing for the P3041 but hints it will cost "significantly less" than the P4040.) With its lower price and lower power, the P3041 is the clear winner for new system designs. Other likely candidates for replacement by the P3041 are three PowerQuicc III chips: the MPC8548E, MPC8536E, and MPC8544E. (Table 2 lists two additional chips the P3041 could replace: the dual-core PowerQuicc III MPC8572E and the MPC8641D.)

P3 Wins on Power Efficiency

Table 4 compares the P3041 with two potential competitors: Cavium's Octeon II CN6330 and NetLogic's XLS616. All are quad-core processors. (Intel's quad-core processors use far too much power to be considered competition.) The Cavium and NetLogic chips have 64-bit architectures—not really an advantage in midrange applications. Both are in-order machines, and NetLogic's CPUs have only one pipeline, whereas the Power e500mc is a dual-issue out-of-order CPU. The Cavium and NetLogic CPUs favor slightly deeper pipelines, which permit slightly higher clock speeds, but they pay a greater penalty for mispredicted branches. Moreover, they lag one or two generations behind the P3041 in process technology, negating their extra depth.

The XLS616 partially compensates with multithreading. Each CPU can switch among four threads, improving CPU utilization and throughput in applications (such as packet processing) that have a large number of independent threads. NetLogic gained this product line last year by acquiring RMI, which designed the MIPS64-compatible CPU. (For more details about this multithreaded CPU, see *MPR 5/17/05-01*, "A New MIPS Powerhouse Arrives.")

An interesting feature of the P3041 is the Power e500mc's hardware support for hypervisors. With a hypervisor, the P3041 can run two operating systems concurrently without bringing down the whole system if one of them crashes. This capability is useful when the P3041 handles both control-plane and data-plane duties, which often use two different operating systems or two instances of the same operating system.

	Freescale QorIQ P3041	Cavium Octeon II CN6330	NetLogic XLS XLS616
CPU Type	Power e500mc	cnMIPS64-R2	MIPS64-R2
Arch. Width	32 bits	64 bits	64 bits
Pipeline	7 stages	9 stages	10 stages
Issue Rate	2 per cycle	2 per cycle	1 per cycle
CPUs Per Chip	4 CPUs	4 CPUs	4 CPUs
Multithreading	—	—	4 threads per CPU
CPU Freq (max)	1.5GHz	1.5GHz	1.2GHz
L1 Cache (I / D)	32KB / 32KB per CPU	37KB / 32KB per CPU	32KB / 32KB per CPU
L2 Cache	128KB per CPU	2MB shared ECC	1MB shared ECC
L3 Cache	1MB shared, ECC	—	—
Memory Controller	DDR3 / 3L 1 x 32 / 64 bits Up to 1.3GHz ECC	DDR3 1 x 64 bits Up to 1.6GHz ECC	DDR2 2 x 64 bits or 4 x 32 bits Up to 800MHz ECC
PCI Express	4 x PCIe	2 x PCIe	4 x PCIe (or 4 x sRIO)
Ethernet Controllers	5 x GbE 1 x 10GbE	4 x GbE or 1 x 10GbE	8 x GbE or 2 x 10GbE
Serdes	18 lanes	12 lanes	12 lanes
Serial RapidIO	2 x sRIO	1 x sRIO	4 x sRIO (or 4 x PCIe)
Other I/O	2 DUARTs, 4 x I^2C, SPI	2 UARTs, 2 x I^2C	2 UARTs, 2 x I^2C
USB 2.0	2 with PHYs	2 with PHYs	2, no PHYs
Serial ATA	2 x 3Gb/s	—	—
RAID Engine	RAID5	RAID5/6	—
SD / MMC	Yes	CompactFlash	—
Crypto Accel	Yes	Yes	Yes
RegEx Engine	Yes	Yes	—
IC Process	45nm SOI	65nm G	90nm G
Voltage (CPU)	1.0V	Not disclosed	0.9V–1.2V
Power	15W max	17W max	12W–30W max
Package	FC-PBGA 1,295 pins	FC-BGA 900 pins	BGA 957 pins
Sampling	4Q10 (est)	4Q10 (est)	3Q08
Production	2H11 (est)	2H11 (est)	1Q09
List Price	$150	Not disclosed	$175*

Table 4. Comparison of Freescale's QorIQ P3041 with two quad-core competitors. As the newest chip, the P3041 benefits from smaller fabrication technology that's a generation or two ahead of its rivals. (Source: vendors, except *The Linley Group estimate)

Price and Availability

Freescale Semiconductor's new P3041, P5010, and P5020 chips are scheduled to begin sampling in 4Q10. Production is scheduled for 2H11. Freescale hasn't announced pricing. All members of the P3, P4, and P5 series are pin compatible.

For more information about the P5010 and P5020, access www.freescale.com/webapp/sps/site/prod_summary.jsp?code=P5020

For more information about the P3041, access www.freescale.com/webapp/sps/site/prod_summary.jsp?code=P3041

All these companies churn their product lines every few years, so judging the "winner" depends on when the snapshot is taken. The P3041 looks better now but won't reach the market for a year, giving Cavium and NetLogic time to counterpunch. We expect NetLogic will soon replace the obsolete XLS616 with dual- and quad-core XLP-family processors. Manufactured in 40nm bulk CMOS, they would compare more favorably with Freescale's 45nm SOI chips.

QorIQ Fulfills Freescale's Vision

Since introducing the QorIQ family in 2008, Freescale has announced 13 chips in five series (P1 through P5). With the new P3 and P5 series, the breadth of the QorIQ family is now visible. The simplest P1 designs have one 32-bit CPU and consume less than 5W; the most complex P4 and P5 designs have eight 32-bit CPUs or two 64-bit CPUs and stay below 30W. All are richly endowed with caches, memory controllers, I/O interfaces, and packet-acceleration logic. The P3, P4, and P5 series are pin compatible.

There's more to come. Having completed the rollout of its P-series processors, Freescale's next QorIQ products will initiate the T series, which will be built in 32nm or 28nm technology. *MPR* believes the T4 could scale to 16 CPUs and the T5 could surpass 2.5GHz without exceeding 30W. We expect the first T-series products (probably in the T4 class) to sample in 2011. Meanwhile, the company must deliver the P3 and P5 chips on schedule.

Eventually, QorIQ will supersede all members of the aging MPC and PowerQuicc families, which have never progressed beyond two CPUs. A full year before introducing QorIQ, Freescale outlined its future multicore strategy and the technology developed for it, including the Power e500mc processor core and the CoreNet interconnect that knits the on-chip components together. At that time, Freescale said CoreNet would be capable of linking at least 32 CPUs in a coherent on-chip network (see *MPR 8/27/07-01*, "Freescale's Multicore Strategy").

To compete with rivals like Intel for control-plane applications, Freescale needs not just more CPUs, but also better CPUs. The dual-issue 64-bit Power e5500 is an important step in that direction, because it makes the P5 series suitable for larger systems. To compete more effectively with data-plane rivals like Cavium and NetLogic, Freescale needs a multithreaded CPU. Intel finds two-way Hyper-Threading useful even for its control-plane processors—it's just enough threading to mask some pipeline stalls. Chips like the P3041 that handle both control- and data-plane processing could use wider superscalar issue and multithreading. Programming languages, APIs, and development tools are making rapid progress, so there's never been a better time to think parallel.

Prime Beneficiary: Existing Customers

For designers invested in the Power Architecture, the alternatives are few. AppliedMicro is still struggling to make its first dual-core chip, IBM no longer offers standard products, LSI only has a single product, and P.A. Semi was eaten by Apple.

For designers willing to port their software to a new architecture (or those who already have), Cavium and Intel offer strong alternatives. For data-plane designs, Cavium offers a broad line of compatible multicore processors scaling from 1 to 32 CPUs. The P3 and other QorIQ processors offer better performance per watt, however, thanks to fabrication in 45nm SOI, and they also offer hardware support for hypervisors. For most control-plane applications, the P5 has a significant advantage in performance per watt over Xeon. For the largest networking systems that can tolerate processors consuming 40W or more, Intel's products deliver greater single-thread performance.

Intel is concentrating more effort on reducing power consumption, thereby threatening to become Freescale's main competitor. Future Westmere or even Atom-based processors could offer serious competition for the P5 at power levels below 30W. In storage applications, security equipment, and single-board computers, Intel is already a formidable competitor.

The best customers for Freescale's new P3 and P5 chips are PowerQuicc users and, in the case of the P3, even some existing QorIQ users. The P3041 is a lower-power and less-expensive version of the P4040. The P5010 and P5020 offer a sizable single-thread performance increase over current MPC and PowerQuicc products, and they finally bring Freescale into the land of 64 bits. Freescale remains the leading vendor of networking and communications processors, so it has many customers needing an upgrade. With a focus on performance per watt, the new P3 and P5 processors strengthen the QorIQ line for both control-plane and data-plane applications. ♦