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MICROPROCESSOR REPORT

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INTEL CUTS ATOM'S POWER

Atom-Based Moorestown Chip Set Aims for Smartphones and Tablets

By Tom R. Halfhill and Linley Gwennap {5/31/10-01}

Intel's seemingly quixotic ambition to compete with ARM in cell phones began two years ago with Atom, a clean-slate approach to designing a lower-power x86 processor. Atom reverted to a simpler microarchitecture that dramatically reduced power consumption (relative to PC processors) and quickly dominated the emerging netbook-computer market. But the first-generation Atom and its companion chips are still far too power-hungry for smartphones and tablets—two market segments with even more growth potential than netbooks.

Now, Intel is taking another step, and it's a big one. Moorestown is Intel's code-name for a platform that includes a highly integrated Atom processor, a lower-power system-logic chip, a mixed-signal chip, low-level software, and improved system-level power management. The platform is intended for high-end smartphones, tablet computers, and the handheld computing devices that Intel formerly called mobile Internet devices, or MIDs. It will compete with processors designed for trendy products like the Apple iPhone, Nexus One, and Nokia N900, but probably not with more-integrated processors designed for mainstream smartphones, like the Blackberry Bold and Blackberry Curve.

As Figure 1 shows, Moorestown is much better integrated than the first-generation Menlow platform. Numerous system functions formerly segregated in the I/O hub have been moved to the CPU chip, and the new I/O hub gets a dramatic process shrink from 130nm to 65nm. With help from many other improvements, Moorestown slashes both active and idle power consumption while holding the line on performance. Indeed, in some cases, Moorestown actually boosts performance over Menlow. It's the fastest-clocked processor in its class, reaching clock speeds of 1.5GHz in smartphones and 1.9GHz when taking advantage of the larger thermal envelope in tablet-sized devices.

Moorestown sampled to customers in 2Q09 and is currently shipping to OEMs in volume. Intel says the first tablets and handheld devices built on the platform should appear this summer. (Intel isn't naming the OEMs; their announcements will come later. See the sidebar, "Atomic Smartphones.") Moorestown-based smartphones, which

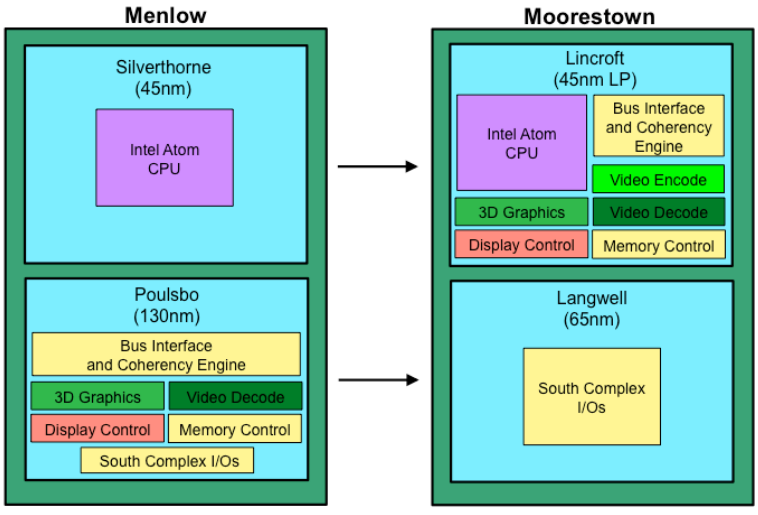

Figure 1. Menlow versus Moorestown integration. Intel's second-generation Moorestown platform uses the same Atom CPU core as Menlow but dramatically improves the level of integration. The microprocessor chip, code-named Lincroft, absorbs several functions previously found in Poulsbo, the Menlow I/O hub.

Atomic Smartphones

Although Intel has been cagey about disclosing smartphone customers, two companies have displayed prototypes of Moorestown-based smartphones. At the Consumer Electronics Show last January, Korean giant LG demonstrated the GW990, which looks like the stretch-limo version of an iPhone. Measuring 147mm×64mm, the GW990 sports a 4.8-inch display capable of widescreen (16:9) content without cropping. It includes all the usual smartphone features and runs the Moblin/Meego version of Linux. Since then, however, LG has decided not to introduce the GW990.

Under contract from Intel, a Finnish design house called Aava Mobile has developed a prototype Moorestown smartphone that also looks eerily like an iPhone. It measures 125mm×64mm×11mm, making it about the same thickness and width as an iPhone but about 10% longer. The Aava design integrates an ST-Ericsson (formerly EMP) modem to provide 3G-cellular capability, a Marvell 8W8688 Bluetooth/Wi-Fi chip, and an Infineon PMB2525 GPS chip, in addition to the three Moorestown chips. The design also includes a 3.8-inch touchscreen, two cameras, two microphones, a compass, and an accelerometer.

Intel used the Aava design for much of its benchmarking. Despite its modest size, the phone includes a 1,500mAh battery, which has about 30% more capacity than the iPhone's battery and 15% more than that of the Nexus One (a popular Android phone). This larger battery aids Intel in claiming battery life comparable to that of leading smartphones.

Aava does not plan to market its phone, but instead will license it to OEMs wishing to quickly deploy this type of smartphone. The company offers a complete reference design and can customize it. Aava currently supports Moblin/Meego and Android on the Moorestown platform. For more information, access www.aavamobile.com.

require more testing and regulatory approval, will appear later—probably around the end of this year.

Moorestown is a significant step for Intel. As the first x86 chip set suitable for smartphones, it establishes a foothold in an important market. *Microprocessor Report* concludes, however, that Moorestown still trails its competitors in both power and integration. Although Intel has made heroic efforts to reduce the power consumption of an x86 PC chip set, virtually all competitors use ARM's simpler RISC architecture, which consumes even less power while delivering sufficient performance. In addition, ARM licensees such as Qualcomm and Texas Instruments (TI) have years of experience designing highly integrated SoCs for cellular handsets. Their newest smartphone processors surpass Moorestown in features, integration, and software support. Thus, Intel's quest to dismember ARM still has a long way to go.

No Longer a PC-Style Chip Set

Comparing Moorestown with Menlow, Intel claims a 50× reduction in idle power, a 20× reduction in active audio power (e.g., when playing MP3 files), and a 2× to 3× reduction in active power when browsing the web or playing videos. Collectively, Moorestown's chips are 40% smaller than Menlow's and require 50% less board space. Intel says Moorestown's 3D-graphics performance is twice as fast.

At first glance, Intel's claims seem incredible for a mere one-generation hop. But keep in mind that Menlow looks nothing like a smartphone chip set. At its heart are a discrete Atom microprocessor and a system-logic chip with distinctly PC features, such as an ATA-IDE interface for hard-disk drives. Menlow is capable of running desktop operating systems and software with respectable performance. It enabled PC vendors to design small netbook computers that quickly became the fastest-growing category of PCs in 2008 and 2009. Menlow also appears in small desktop PCs (nettops) and media-center PCs for living rooms.

Smartphones are an entirely different ballgame. Their maximum power envelope is less than the standby power of a desktop PC. The most widely publicized of Intel's claims is that Moorestown uses 50× less power than Menlow. Many news stories, however, didn't note that the 50× reduction is for *idle* power, not active power. Menlow's I/O hub, code-named Poulsbo, doesn't even have a powered-down idle mode. Obviously, Intel had tremendous room for improvement.

Better integration was Intel's first goal. Menlow implements the Atom processor as a discrete microprocessor chip (code-named Silverthorne) with minimal system integration. Intel crammed almost all system functions into Poulsbo, the I/O hub. Intel manufactures Silverthorne in a conventional 45nm CMOS process and relegates Poulsbo to an older and less efficient 130nm process.

Intel's thermal design power (TDP) for Silverthorne and Poulsbo is 2.0W, and even in idle mode, they use at least 1.0W. That's good enough for netbooks, but Menlow clearly wasn't designed for smartphones and other handheld devices. Poulsbo's package measures 22mm, which is small for a PC system-logic chip but rather large for a smartphone chip. And Menlow requires myriad companion chips, such as discrete PHYs for the USB interfaces, that bloat the size of the system board. (See the sidebar, "Atom's System Controller Slashes Power, Too," in MPR 4/7/08-01, "Intel's Tiny Atom.")

Moorestown represents a major restructuring. The biggest difference is that Intel moved almost all the important system functions from the I/O hub to the microprocessor chip. This chip is code-named Lincroft, and the I/O hub is code-named Langwell. A third component is a mixed-signal chip (code-named Briertown) sourced from third-party suppliers allied with Intel. (For definitions of relevant Intel code-names, see the sidebar, "Decoding Intel's Code Names.")

Decoding Intel's Code-Names

Even the pros have trouble remembering all of Intel's product code-names. Here's a quick guide to the code-names relevant to the Moorestown announcement.

Azalia: digital-audio logic embedded in the Poulsbo I/O chip.

Bonnell: the first-generation Atom x86 microarchitecture. Introduced in 2008, it's found in all Atom-based chips to date, including Silverthorne, Lincroft, and Tunnel Creek.

Briertown: a highly integrated mixed-signal IC, part of Intel's Moorestown platform for smartphones and tablets. Briertown MSICs are actually supplied by third parties: Freescale, Maxim, and NEC/Renesas.

Evans Peak: a wireless-radio chip for the Moorestown platform that combines Bluetooth, GPS, Wi-Fi, and WiMax functions.

Geyserville: a version of Intel's SpeedStep technology that dynamically adjusts a microprocessor's clock frequency and voltage to optimize power consumption and performance. The Atom processor in the Moorestown platform uses a burst-mode variation known as Enhanced Geyserville or Enhanced SpeedStep.

Langwell: an I/O chip paired with the CPU chip in the Moorestown platform for smartphones and tablets. Officially called the Intel Platform Controller Hub MP20, it includes features not integrated in the Atom Z6xx-series processor chip (Lincroft).

Lincroft: the CPU chip in the Moorestown platform for smartphones and tablets. Officially called the Atom Z6xx series (part numbers will vary with clock speeds and other features), this chip is paired with an I/O chip (Langwell).

Medfield: the next-generation smartphone platform beyond Moorestown. Expected to ship next year, it will combine the features of Moorestown's Lincroft and Langwell chips into a single device built in a 32nm LP process.

Menlow: the first chip set based on Intel's Atom microprocessor. Menlow includes an Atom Z5xx-series processor chip (part numbers vary with clock speeds and other features) and an I/O chip (Poulsbo). Most often found in netbook and nettop PCs, Menlow is being superseded by Pine Trail-M and Pine Trail-D.

Moorestown: Intel's latest and lowest-power chip-set platform using the Atom microprocessor. Intended primarily for smartphones and tablets, Moorestown includes an Atom Z6xx-series processor chip (Lincroft), an I/O chip (Langwell), and a mixed-signal IC (Briertown). Lincroft and Langwell are available from Intel; Briertown is available from third-party suppliers.

Oak Trail: a future Atom-based chip set for slates, tablets, and other handheld computers. It uses the same Lincroft processor chip as Moorestown but a different I/O-hub chip, and it can run Windows 7 Home Premium.

Pine Trail: an Atom-based platform introduced this year for netbook PCs. Also known as Pine Trail-M, it includes Pineview, the Atom N450 or Atom N470 CPU chip. Pine Trail-D is a variation for Atom-based desktop (nettop) PCs. Some chips will have dual Atom cores.

Pineview: an Atom variant (also called Pineview-M) introduced this year for netbook PCs. Officially called Atom N450 or Atom N470, it's part of the Pine Trail-M platform. Pineview-D is a variation for Atom-based desktop (nettop) PCs and is officially called Atom D410 and Atom D510.

Poulsbo: an I/O chip paired with the CPU chip in the Menlow platform. Officially called the Intel System Controller Hub, it includes features not integrated in the Atom Z5xx-series processor chip (Silverthorne). It's found mainly in netbook PCs.

Queens Bay: a new Atom-based embedded chip set. It's similar to Moorestown but is intended for embedded systems other than smartphones and tablets. It includes the Tunnel Creek processor chip and Topcliff I/O chip.

Silverthorne: the CPU chip in the Menlow platform. Officially called the Atom Z5xx series (part numbers vary with clock speeds and other features), this chip is paired with an I/O chip (Poulsbo). Found mainly in netbook and nettop PCs, it is being superseded by Pineview-M and Pineview-D.

Topcliff: an I/O chip paired with the CPU chip in the Queens Bay platform. It includes features not integrated in the Atom processor chip (Tunnel Creek) and is intended for embedded systems other than smartphones and tablets.

Tunnel Creek: the CPU chip in the Queens Bay platform. This Atom-based processor is paired with an I/O chip (Topcliff). Intended for embedded systems other than smartphones and tablets.

Integration Makes the Difference

The Atom CPU core in Lincroft remains unchanged from the original Atom microarchitecture (code-named Bonnell) we described in 2008. (See *MPR 4/7/08-01*, "Intel's Tiny Atom.") As implemented in Moorestown, it's still an x86 single-core CPU with two-way superscalar execution and dual Hyper-Threading. It has the same 32KB instruction cache, 24KB data cache, and 512KB L2 cache. Although Atom implements Intel's 64-it x86 extensions, they are disabled in the Menlow/Moorestown silicon.

As Figure 2 shows, Lincroft absorbs the display adapter, 3D-graphics accelerator, video encode/decode engine, and memory controller. Intel manufactures Lincroft in a special low-leakage variation of its 45nm high-*k* metal-gate process (which we refer to as 45nm LP). Officially, Intel refers to Lincroft as the Intel Atom Processor Z6xx series; different part numbers will denote the various speed grades. (Intel hasn't announced actual chips, but clock speeds are expected to reach 1.5GHz in smartphones and 1.9GHz in tablets.) Silverthorne, which remains in the product line, is officially known as the Atom Z5xx series.

Like Intel's recent Nehalem and Westmere processors, Lincroft integrates the memory controller and CPU on a single chip. This approach reduces power consumption by moving the front-side bus on chip; once retrieved from DRAM, memory data doesn't have to make another power-hungry chip-to-chip crossing. This shorter pathway also reduces the effective memory latency, improving performance slightly. Lincroft, however, trims the width of the memory interface to 32 bits—half the width of Menlow's memory interface. This reduction in memory bandwidth could hamper performance.

To reduce power in smartphones, Lincroft supports low-power (LP) DRAM at speeds of up to DDR-400. For tablets, Lincroft also supports standard SDRAM at up to DDR2-800, but it does not support DDR3 SDRAM, which will be less expensive than DDR2 when Moorestown-based systems reach production. Intel plans to add DDR3 support to Medfield, the next-generation chip set beyond Moorestown that is scheduled for production late next year.

Lincroft's integrated display controller supports two video interfaces: LVDS (low-voltage differential signaling) at screen resolutions up to 1,366×768 pixels and MIPI-DSI (Mobile Industry Processor Interface–Display Serial Interface) at resolutions up to 1,024×600 pixels. LVDS is more common, but MIPI is gaining popularity in small devices because it uses less power. (Menlow doesn't support MIPI.) These screen resolutions are more than enough for smartphones and are well suited to tablet-sized displays.

Process Shrink Enables Faster Graphics

Intel's integrated graphics are a frequent target of derision in the desktop PC market, where discrete graphics processors and video cards from AMD and Nvidia rule the roost. In the past, 3D graphics and video playback were less important in mobile PCs and handhelds, but that's changing. Increasingly, mobile communications devices are serving as entertainment devices, too. Today's users want to watch streaming video, download movies, and play games.

Menlow was criticized for its relatively poor graphics performance; Nvidia built a cottage industry around this shortcoming. Luckily for Intel, most netbook users don't expect their tiny computers to match the performance of a larger-screen notebook PC, much less a desktop PC. A few netbooks, such as Hewlett-Packard's Mini 311, redress the grievance by substituting Nvidia's Ion chip for Intel's Poulsbo, despite stiff disincentives from Intel. (Buying an Atom processor by itself is more expensive than buying it with Poulsbo.)

Moorestown responds to critics by doubling the performance of the 3D-graphics engine. For both Menlow and Moorestown, Intel licensed the PowerVR SGX-535 engine from Imagination Technologies, a British company. PowerVR SGX supports DirectX 9, OpenGL ES 1.1/2.0, and OpenVG 1.1. Apple's iPhone 3GS also uses this graphics engine, as do many other phones. (At last report, Intel owns 14% of Imagination Technologies; Apple owns 3.6%.)

Moorestown relocates the graphics engine from the I/O hub to the CPU chip, which Intel fabricates in its 45nm LP high-*k* metal-gate process. Even discounting the metal-gate wizardry, this process is three generations better than the moth-eaten 130nm process used for Poulsbo. The dramatic process shrink and tighter coupling with the CPU allowed Intel to double the maximum clock speed of the graphics engine from 200MHz to 400MHz. (OEMs may run the engine at a lower frequency to save power.) Also, Intel and Imagination say they have further optimized their software drivers for the engine.

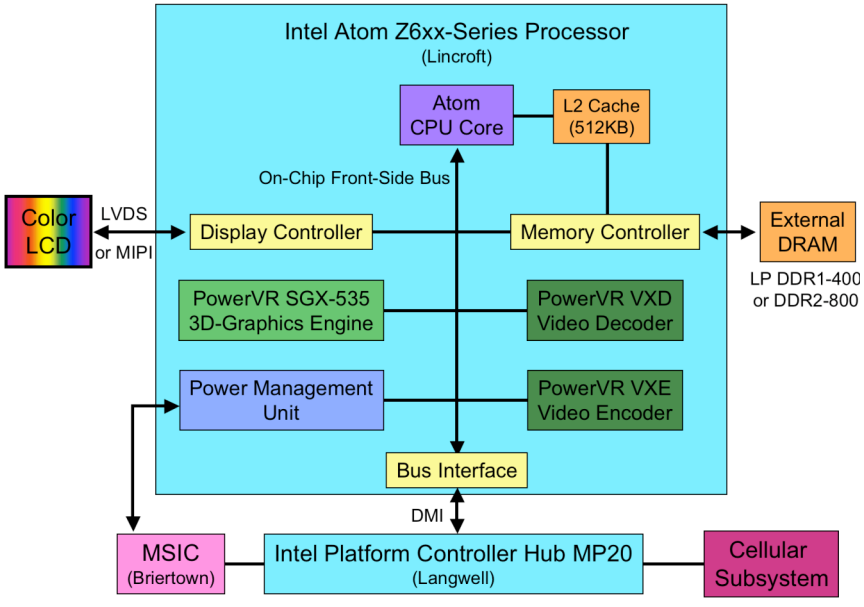

Figure 2. Lincroft block diagram. Intel hasn't publicly disclosed the interface that connects Lincroft and Langwell, but we believe it's a variation of Intel's proprietary Direct Media Interface (DMI).

Better Video Decoding and Encoding

For video playback, Moorestown uses Imagination Technologies' PowerVR VXD decoder. This, too, is basically unchanged from Menlow, but the Moorestown implementation is faster, again owing to the dramatic process shrink. Although Menlow was technically capable of playing high-definition video at 1,080-pixel resolution, driver problems hampered performance—part of the reason why some OEMs replace Poulsbo with Nvidia's Ion chip.

Intel says Moorestown can play 1080p video at 30 frames per second (fps) using MPEG2, MPEG4, H.264, VC1, or WMV9. In some situations, Moorestown can simultaneously play multiple video streams, including one stream in HD and

another in SD. The decoder's maximum vertical resolution of 1,080 pixels is actually higher than Moorestown's displays can handle, so the display controller automatically scales the video to fit a smaller screen. Otherwise, users would have to transcode the HD video before playing it—a slow and power-sapping task.

Although some competing products can decode 1080p video, Intel claims its smartphone chip set can handle 1080p H.264 High Profile, which is used for Blu-ray discs and many broadcast formats. Products that implement only H.264 Baseline Profile do not support some aspects of the standard, such as B slices and interlacing, that are required for High Profile implementations.

In addition to better decoding, Moorestown can encode a video stream; Menlow has no encoding engine. This capability is necessary if the OEM wishes to build a high-resolution video camera into the end product. Lincroft uses Imagination's PowerVR VXE video encoder, which supports multiple codecs: MPEG4 (broadcast TV), H.263 (videoconferencing), and H.264 Baseline Profile (Level 3, 720p, 30fps). Note that the VXE encoder can't quite handle the same 1080p resolution as the VXD decoder.

With both a video decoder and video encoder, Moorestown can do some real-time transcoding, which Intel believes will be an important function for high-end smartphones. (Some video streams may be encoded in a format that the tablet or smartphone can't directly display.) The video engines are useful for other tasks, too. For example, the encoder can compress still-image files in JPEG format, and the decoder can decompress them, although Intel is using a dedicated image-processing engine in Langwell for those functions.

The Lincroft die measures 65mm^2 in Intel's 45nm technology. As the die photos in Figure 3 show, Lincroft's extra features make it nearly three times larger than the Silverthorne processor chip. Imagination Technologies' 3D-graphics engine and video accelerators actually occupy more silicon on Lincroft than do the Atom CPU core and 512KB L2 cache. As synthesizable blocks, they're not quite as area-optimized as the CPU, but they pull their weight by offloading heavy-duty processing from the CPU. Overall, Lincroft is slightly larger than the Apple A4 application processor (used in the iPad), which measures 53mm^2 in Samsung's 45nm technology and does not require a separate south-bridge chip.

With their newly enhanced graphics, video, and display capabilities, Moorestown-based systems will be equally adept at entertainment and communications—a vital nexus for smartphones and the emerging tablet market. Good graphics and video will set high-end smartphones apart from mainstream phones.

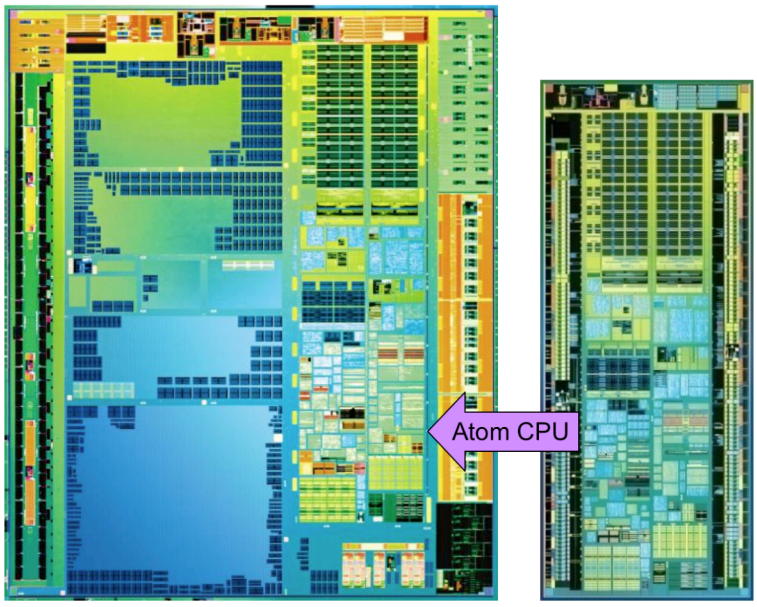

Figure 3. Die-photo comparison of Lincroft versus Silverthorne. Lincroft, shown on the left, is a highly integrated microprocessor chip that still measures only 65mm^2. Although it's nearly three times as large as the first-generation Silverthorne chip (24mm^2), it contains additional functions. Silverthorne has 47 million transistors, and Lincroft has 140 million. (Photos courtesy of Intel.)

Langwell Integrates I/O

The Langwell system-logic chip is an I/O hub, similar to a south-bridge chip in a PC. It integrates most system functions not implemented in the microprocessor or north-bridge chip. (In Moorestown, most north-bridge functions are integrated with the microprocessor.) Unlike Poulsbo, Langwell absorbs the flash-memory controller and the camera-sensor interface, reducing the total chip count and conserving board space. Intel contracts with TSMC to manufacture Langwell in a 65nm LP CMOS process.

Officially known as the Intel Platform Controller Hub MP20, Langwell includes the critical I/O functions (USB 2.0, USB OTG, HDMI, eMMC, and SDIO) needed in a smartphone, along with support for two camera sensors—typically a five-megapixel outward-facing sensor and an inward-facing VGA-resolution sensor for video-conferencing—via parallel or serial (MIPI-DSI) interfaces. As in Menlow, the I/O hub contains a dedicated image-processing engine that performs functions such as auto exposure, auto white balance, noise reduction, and JPEG compression on the images from the cameras. (Intel licensed the image-processing engine from an undisclosed third party; *MPR* believes it's a Silicon Hive signal processor.) A small decryption engine allows boot code to be encrypted for greater security.

Langwell supervises all these functions with a 32-bit RISC processor licensed from ARC International, which was acquired by Virage Logic last year. (See *MPR 9/14/09-01*, "Summer Shopping

Moorestown Goes Embedded

At the Beijing Intel Developers Forum in April, Intel unveiled the Tunnel Creek processor for embedded applications other than smartphones and tablets. Although the company touts Tunnel Creek as an SoC, it's part of a two-chip set that is a variant of Moorestown.

Tunnel Creek has basically the same processor as Lincroft in a larger 22mm BGA package. The larger package is less expensive to manufacture and to attach to a PC board, reducing system cost. Like Lincroft, Tunnel Creek integrates a memory controller, graphics acceleration, and a display controller along with the Atom CPU. No speed grades were disclosed, but we expect Tunnel Creek to offer speeds up to 1.9GHz, similar to the faster versions of Lincroft.

Unlike the original embedded Atom processor (the N270), Tunnel Creek uses four PCI Express I/O lanes to connect to the south-bridge chip. This approach enables the processor to be combined with third-party I/O chips or ASICs. Most of the time, however, the Tunnel Creek processor will be used as part of the Queens Bay platform, which also includes a new I/O hub known as Topcliff. This chip provides common embedded interfaces such as Gigabit Ethernet, USB, SATA, CAN, and SDIO. Topcliff comes in a 23mm BGA package, making it much smaller than its embedded predecessor, the Intel 945G chip set.

Target applications of Queens Bay include in-car information systems (hence the CAN interface), industrial automation, multimedia-capable Internet Protocol phones, and digital signs. The Queens Bay chips reportedly sampled in 3Q09 and should enter production by 4Q10, when their formal launch is planned.

For embedded designers seeking a small, inexpensive x86 processor, Queens Bay provides an excellent solution. In fact, the size reduction from Menlow allows Intel to target new markets, such as in-dash systems. Competitors such as Marvell, however, offer true SoC solutions that are smaller and less expensive than Queens Bay. Intel says it is developing single-chip designs to better compete against these RISC-based products. For designers who are not wedded to the x86 instruction set, Queens Bay brings Intel closer to the mark but still not in the center ring.

Spree.") The ARC processor also offloads audio processing from the Atom CPU, allowing the main CPU to sleep while the user is listening to music or other audio. As a result, Intel says a Moorestown device can deliver 48 hours of MP3 playback from a 1,500mAh battery.

For embedded systems, Intel is offering a variation of Moorestown code-named Queens Bay. This platform substitutes a different I/O-hub chip that provides popular embedded functions such as Ethernet. (See the sidebar, "Moorestown Goes Embedded.") Another version, Oak Trail, is for Windows 7 tablets. Intel may develop additional I/O-hub variants for other applications.

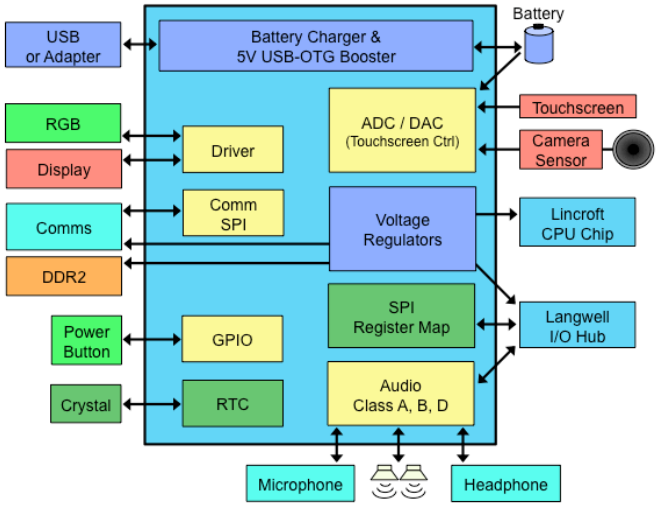

Figure 4. Briertown block diagram. Officially known as the Mixed-Signal IC (MSIC), this chip includes I/O interfaces, audio logic, and miscellaneous features required to support the Lincroft and Langwell chips. Intel relies on partners to manufacture the MSIC.

Third Parties Provide Analog Functions

Lincroft and Langwell are much better integrated than the Silverthorne-Poulsbo combo, but they still require additional chips—such as cellular transceivers, Wi-Fi, GPS, and Bluetooth—to fulfill necessary system functions. Intel has outsourced the design and manufacture of those chips to other companies. This strategy allows more room for differentiation among customers using the Moorestown platform, and it lets Intel concentrate on the higher-value parts.

One companion chip is a mixed-signal IC code-named Briertown. As Figure 4 shows, it integrates analog audio functions, voltage regulators, an ADC/DAC, battery-charging logic, a real-time clock, general-purpose I/O interfaces, and other features. These functions required several additional chips in the Menlow platform. The ADC and DAC can connect to a touchscreen, eliminating the need for a separate controller chip. Briertown also includes the PHY for the USB OTG controller implemented in Langwell.

Intel's manufacturing processes are not well suited to this type of mixed-signal design, and the company's design library lacks some of the necessary analog building blocks. For these reasons, the company turned to third parties to help design and manufacture the MSIC. Moorestown customers can buy it from Freescale Semiconductor, Maxim, or NEC (now Renesas).

In previous discussions of Moorestown, Intel disclosed a fourth chip, code-named Evans Peak, that the company was developing internally. This device combines wireless functions such as Bluetooth, GPS, Wi-Fi, and WiMax. Evans Peak, however, was conspicuously absent from the recent Moorestown announcement. Either Intel is de-emphasizing it or is still working on the complex design.

Several third parties offer products that deliver these standard functions.

Multiple Approaches to Power Reduction

Intel has reduced Lincroft's power consumption in several ways: higher integration, a lower-leakage fabrication process, better on-chip power management, enhanced voltage-frequency scaling, a new "burst mode" that dynamically adjusts performance within thermal limits, and a more thorough approach to power management in the operating system.

First is integration. Relocating the most frequently used system functions from the I/O hub to the processor chip saves power by dramatically reducing chip-to-chip bus traffic. Internal buses require less drive current than external buses, so they can operate at lower voltages. I/O transistors associated with the internal buses can be smaller and more power-efficient, too.

Second, Intel is manufacturing Lincroft in a low-leakage variation of the company's standard 45nm high-*k* metal-gate CMOS process. This 45nm LP process is specifically tuned for SoCs and is part of the manufacturing line at all of Intel's 45nm fabs. As with other low-leakage processes, it slightly increases dynamic power consumption but significantly reduces current leakage. Overall, power consumption is lower if the system spends most of its time sleeping—a usage profile typical of cell phones.

Intel's 45nm LP process has other benefits as well. Instead of standardizing on a single type of logic transistor throughout the design, it uses transistors of different sizes tailored to the circuit's drive current. For example, Lincroft must drive its I/O transistors at a higher voltage (1.8V) than its logic transistors, so they're slightly larger. Intel says the 45nm LP process slashes current leakage by more than 50% compared with the company's conventional 45nm process—without sacrificing performance.

Intel's third approach to reducing power consumption is to implement greater flexibility in power distribution throughout the chip. Lincroft has 19 separate "power islands": electrically independent regions that can be powered up or down as required. In addition, Intel has increased the amount of clock gating on the chip. Clock gating allows smaller blocks of logic within the power islands to switch off when not needed. (Briertown integrates the clock generator, too, eliminating the need for a separate clock chip.) These coarse- and fine-grained power domains reduce both dynamic power and passive power.

Speed Scaling Saves Power

Fourth, Lincroft supports an enhanced version of Intel's SpeedStep technology, which enables a microprocessor to vary its own clock frequency and core voltage to match the software load and thermal requirements. Code-named Enhanced Geyserville, this technology allows the Atom CPU in Lincroft to reduce its core frequency far below Silverthorne's 600MHz floor. (Intel won't publicly disclose Lincroft's minimum core frequency, but unsubstantiated reports claim it's as low as 200MHz.) Power consumption scales linearly with clock frequency (assuming the same voltage), so the lower floor is significant. Reducing the core voltage is even more significant, because power varies at a squared rate with voltage. Intel hasn't publicly specified the voltage range for Lincroft.

To optimize performance, a new "burst mode" in Lincroft lets the CPU increase its clock speed for brief periods when thermal conditions allow it. Don't confuse this burst mode with DRAM burst reads or Intel's Turbo Boost mode in Core i5 and Core i7 multicore processors for PCs and servers. As implemented in those processors,

Turbo mode automatically overclocks one core in a multicore processor to increase performance while the other cores remain idle or run at a lower clock speed. By contrast, Lincroft's burst mode accelerates the lone CPU core to its maximum clock frequency or thereabouts to quickly finish a task, then settles back to a slower, cooler clock speed. It can also vary the speed of the on-chip front-side bus.

Figure 5 illustrates a burst-mode sequence. This figure implies that the processor will spend most of its time in a throttled state while only occasionally operating at its rated speed. Assuming a constant core voltage, a microprocessor will use the same amount of power when executing a given task at different clock speeds, so burst mode saves power only if the processor can reduce the voltage as well as the clock frequency when idling. In fact, this approach runs counter to the sprint-and-sleep approach used with Menlow.

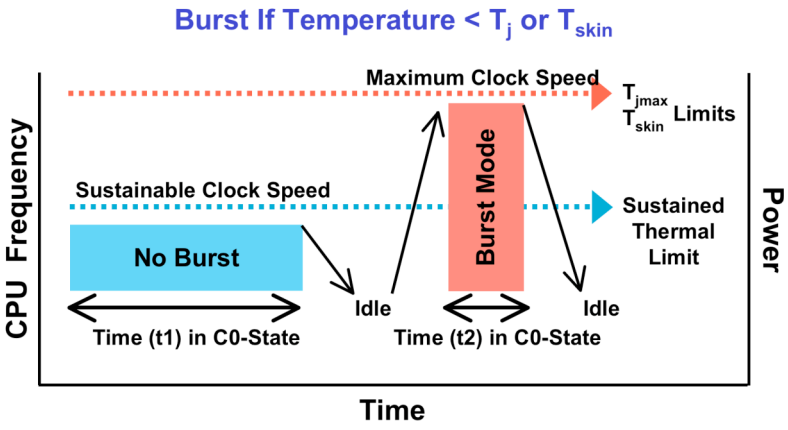

Figure 5. Lincroft's burst mode. This technique allows the Atom CPU to briefly accelerate to its rated clock speed before throttling back to a thermally sustainable speed. The T_{skin} temperature variable in this figure represents the maximum comfortable heat dissipation for a handheld smartphone—about 2.0W. Hotter temperatures make the phone uncomfortable to hold. T_j is a more familiar variable that represents the chip's junction temperature; T_{jmax} is the maximum allowable junction temperature.

Instead of saving power, burst mode appears designed to squeeze Atom into the limited thermal capacity of a thin smartphone design.

An important implication of burst mode is that Intel's specified maximum clock frequencies for Lincroft are unsustainable for prolonged periods. The Atom processor can briefly burst to those high clock speeds when thermal conditions are favorable, but most of the time, it must downshift to a lower speed to avoid overheating. This limitation takes some shine off Lincroft's industry-leading clock frequencies. Competing processors in this class have lower maximum clock speeds, but those speeds are more sustainable. Lincroft, however, can probably match the lower sustainable clock frequencies of competing processors and can burst to higher speeds when possible.

New Low-Power States

Intel's fifth approach to power reduction is the debut of two new low-power states in Lincroft. PC designers already are familiar with the existing x86 power states oriented toward PC processors: C0 (full power, everything active) through C6 (deep sleep, almost everything inactive). Lincroft introduces the S0i1 and S0i3 power states. (Intel says an S0i2 state will appear in future handheld devices.)

Intel's nomenclature is a little confusing here, because Lincroft continues to support C0 through C6, which collectively are included in S0. S0i1 and S0i3 are actually intermediate system-level states (hence the uppercase "S" and lowercase "i"), whereas C0 through C6 are CPU-only power states. S0 is the highest power state for the whole system. In a smartphone, for example, S0 includes not only the CPU chip but also all the other chips, the display, the keypad, and the I/O interfaces—everything.

Table 1 describes the new power states. In S0i1 mode, the system is largely idle but continues to display a static web page or the device's home page. Although the CPU enters C6 deep-sleep mode and stores its state in SRAM, the system remains ready to process user interaction. By contrast, S0i3 downshifts the system into the lowest-power standby mode. The system expects no user interaction for a while and turns off the C6 SRAM, but it continues to supply control signals that keep the DRAM in self-refresh mode. Intel cautions that S0i2 and S0i3 are *not* directly comparable with the existing PC power states known as S4 and S5.

Moorestown can enter S0i3 standby mode in 400 microseconds and exit in 3,100 microseconds. Lincroft's power consumption in this mode is only 100 microwatts. Intel estimates that the total system power consumption for a smartphone in this standby mode will be 21mW. In comparison, a system using the first-generation Menlow chip set, which lacks a fully idle standby mode, consumes at least 1.4W in its lower-power mode. Hence, Intel claims a 50× power reduction.

Intel hasn't specified Moorestown's power consumption in S0i1 mode. The chip set can enter this mode in 600 microseconds and exit in 1,200 microseconds. Because leaving this mode is three times faster than leaving S0i3 mode, it's more suitable for brief pauses in interaction as the user views a web page or other content.

Figure 6 shows infrared photographs of Lincroft's thermal characteristics when operating at full power and in S0i1 mode. In the latter mode, most of the chip is shut down, leaving only a few blocks consuming power. (The small block illuminated in the lower-right corner of the photo is the SRAM that stores the Atom processor's CPU state.) When the chip enters the deeper-sleep S0i3 power state (not shown), essentially everything shuts down, and the thermal image goes dark.

Despite all these efforts to reduce power consumption, Intel hasn't captured the lead in this market. The company has done an excellent job minimizing idle power, putting its processors on a par with those from companies that have spent years optimizing their mobile devices. As Table 2 shows, Intel says a Moorestown device can achieve 10 days of standby time on a 1,500mAh battery—more than most cell phones today.

Most users, however, don't simply leave their smartphones in their pocket for days on end. Intel has also measured the performance of its Moorestown prototype while running a variety of other tasks. These measurements show significant improvement from Menlow. More importantly, they are fairly competitive with the battery life of leading smartphones. Some of these phones,

	System Power States		
	S0	S0i1	S0i3
Power-State Description	Highest system power state; fully active	Idle, but display is active, ready for user interaction	Lowest system power state; standby mode, no user interaction
Atom CPU	C0–C6 power states	C6 (deep sleep)	Off
C6 SRAM, Wake Logic	On	On	Off
DDR DRAM	On, self-refresh	Self-refresh	Self-refresh
Power Manager	On	On	Off
Graphics	On, power-gated	Power-gated	Off
Video Decode	On, power-gated	Power-gated	Off
Video Encode	On, power-gated	Power-gated	Off
Display	On	Off	Off
Display Controller	On, power-gated	Power-gated	Off
Links to I/O Hub	On, power-gated	Power-gated	Off
Entry Latency	Not applicable	600 microseconds	400 microseconds
Exit Latency	Not applicable	1,200 microseconds	3,100 microseconds
Power	Not specified	Not specified	100 microwatts

Table 1. Power states for systems built with Intel's Moorestown chip set. S0i1 and S0i3 are new intermediate power states for the entire system, not just for the CPU or chip set. S0i1 is considered an "idle" mode, but the system can display a web page or other static content while remaining ready for user interaction. S0i3 is a lower-power standby mode that shuts off almost everything but DRAM refresh.

however, use a battery with less than 1,500mAh capacity. Furthermore, the battery life of the platform is determined by many system-level factors, such as the power usage of the display and cellular subsystem.

New Hooks for Operating Systems

All the new power-saving features built into the hardware would be fruitless without a system-level approach to managing power consumption. Therefore, another critical part of the management (OSPM). The driver-level software in mobile operating systems must monitor the system's thermals, estimate the amount of processing power required by applications, and shift the system into the appropriate power state. The operating system is also responsible for invoking Moorestown's burst mode when necessary.

Managing this balancing act requires the hardware, firmware, and software to work closely together. As Intel says, the operating system's policy manager must "conduct the system like an orchestra." Consequently, Intel has added new operating-system hooks to Moorestown and is working with software developers to optimize the drivers.

Both Lincroft and Langwell have their own power-management logic, eliminating the need for the external chips found in some systems. Additional power-management logic is built into the mixed-signal Briertown chip supplied by Intel's partners. So far, the mobile operating systems announced to work with Moorestown are Android, Meego, and Moblin.

Android is Google's Gnu/Linux-based cross-platform operating system for mobile devices and is the up-and-coming challenger to Apple's proprietary iPhone OS. Moblin is Intel's own Gnu/Linux-based mobile OS. Meego is a relatively new open-source project that's a mash-up of Moblin and Nokia's Maemo. It's likely that Intel's own programmers (or those at recently acquired Wind River Systems) are doing all or most of the work to optimize these operating systems for Moorestown.

Intel is almost certainly working with other operating-system vendors but declines to comment. Note the absence of any Microsoft operating systems, such as Windows Phone 7, Windows Phone 8, and Windows CE, from Intel's list. Microsoft dominates the desktop but not the pocket. Intel's future Oak Trail chip set—which uses the Lincroft processor chip but a different I/O hub—will support Windows 7 Home Premium on slates, tablets, and other handheld computers, however.

Intel has downplayed any interest in supporting Symbian, the world's most popular smartphone operating system. Another notable absentee is Palm's WebOS. Once considered a dark-horse contender from a company in decline, WebOS suddenly gained momentum when Hewlett-Packard announced its $1.2 billion acquisition of Palm on April 28. The deal spurred rumors that HP will dump Microsoft's Windows 7 from the much-anticipated Slate tablet and replace it with WebOS. Slate is reportedly based on Menlow, not Moorestown, and is touted as the leading candidate to challenge Apple's fast-selling iPad.

System Function	Battery Life (1,500mAh)	Improvement Moorestown vs. Menlow
3G Phone Call	~6 hours	Not applicable
Web Browsing~ (Wi-Fi)	5 hours	2x
Video Playback (1080p)	~4 hours	Not applicable
Video Playback (720p)	~5 hours	3x
MP3 Audio Playback	~2 days	>20x
Standby	>10 days	>50x

Table 2. Estimated battery life of a Moorestown smartphone. Intel obtained these estimates when testing early silicon of the chip set. Note that these estimates include the power consumption of the whole system, not just the Moorestown chip set.

Cortex-A9 Offers Performance Challenge

In the smartphone market, Moorestown faces a number of competitors, ranging from market leaders, such as TI's OMAP and Qualcomm's Snapdragon, to new entrants, such as Nvidia's Tegra and ST-Ericsson's U8500. Many of these competitors have established strong relationships with leading smartphone suppliers. To break into this market, Intel must convince at least some of these suppliers that it has a better processor.

Although Moorestown offers a compelling performance advantage over currently shipping phones, we don't expect Moorestown-based smartphones to ship until late

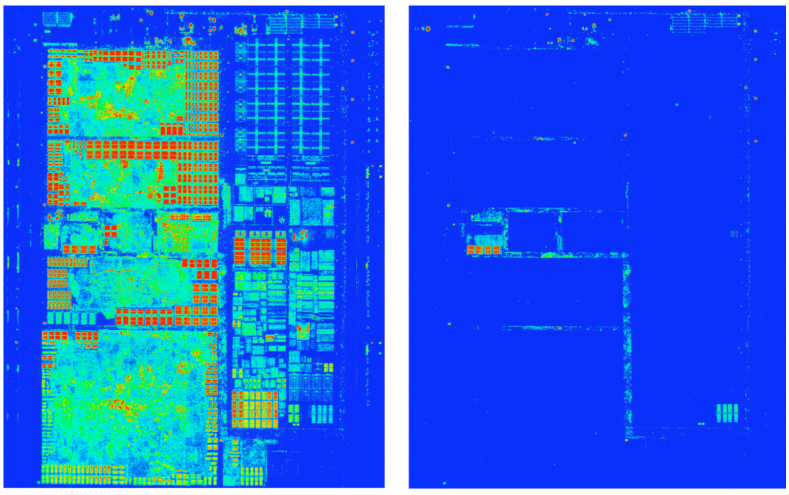

Figure 6. Thermal images of Lincroft in two different power states. At left, the chip is running in full-power mode (S0/C0). At right, the chip is idling in the S0i1 state but is still able to display static content on the screen and respond to user input. (Photos courtesy of Intel.)

this year or early next year. By that time, many competing phones will be using processors like the OMAP 4430, U8500, and Tegra 2 that include two ARM Cortex-A9 CPUs running at speeds of up to 1.0GHz. Qualcomm plans to increase the speed of its ARM-compatible Scorpion CPU to 1.3GHz in that timeframe and expects to have dual-CPU processors available shortly thereafter.

Comparing the performance of smartphone processors is difficult, owing to the lack of accepted benchmarks. Intel touts Atom's far better SPECmark scores even compared with a dual-CPU Cortex-A9 configuration, but ARM has never published SPECmark scores for its processors; Intel's comparison is based on its own internal tests of ARM processors. Furthermore, Intel has spent a decade optimizing its CPUs and compilers to produce superior scores on SPECmark (which was originally designed as a workstation benchmark). It is doubtful that the company has spent as much time optimizing its compilers for other vendors' CPUs.

Cortex-A9 is a dual-issue superscalar CPU with instruction-reordering capability. Atom is also dual-issue but lacks instruction reordering and has a longer, unwieldy pipeline. Their differences are fundamental: the x86 architecture's CISC instructions simply require more logic to decode and execute than ARM's RISC instructions do. A hard macro of ARM's dual-core Cortex-A9 is about the same size as a single-core Atom. On the other hand, Atom's Hyper-Threading can boost performance in ways that the single-threaded Cortex-A9 cannot. (For background on Cortex-A9, see *MPR 11/9/09-01*, "More Applications for OMAP4.")

On the basis of the sparse benchmark results available for both processors, we expect Atom and Cortex-A9 to deliver about the same performance per cycle for pure CPU-bound applications. For example, ARM claims 2.5 Dhrystone MIPS per megahertz per core, or an aggregate 5.0DMIPS/MHz for the standard dual-core configuration. Intel claims 4.8DMIPS/MHz for a 1.5GHz Atom processor running a single thread of unoptimized code, or 5.4DMIPS/MHz with optimized code.

Using EEMBC's CoreMark benchmark, ARM quotes 2.9 CoreMarks per megahertz per core for Cortex-A9. An Atom processor running a single CoreMark instance scored only 1.8 CoreMarks/MHz. But with Hyper-Threading enabled, two different Atom processors (N450 and N270) running dual threads at 1.0GHz and 1.6GHz (respectively) scored 2.8 CoreMarks/MHz. Note that all versions of Moorestown, unlike some versions of Menlow, implement Hyper-Threading. (For information about CoreMark, see *MPR 6/8/09-01*, "EEMBC's Dhrystone Killer.")

With a single-threaded workload, a 1.5GHz Atom should still outperform a 1.0GHz Cortex-A9 because of its faster clock speed. With two threads, Intel says Atom gains about 35% from its Hyper-Threading, although the CoreMark results measure a larger gain. The dual Cortex-A9 configuration can double its peak performance, delivering the equivalent of a single core at 2.0GHz. Depending on its specific characteristics, one application may fare better on Atom and another on the dual Cortex-A9 CPUs, but we don't see a compelling performance advantage for Atom. (For more about Atom-versus-ARM benchmarking, see The Linley Group's blog post at: *http://blog.linleygroup.com/2010/04/arm-outmuscles-atom-on-benchmark.html*.)

The main reason that smartphone users need a fast CPU is to display web pages. Current devices often take 10 seconds or more to render

	Intel Atom Z6xx + MP20	Texas Instruments OMAP 4430	Qualcomm SnapDragon QSD8650A
Application CPU	Atom	2x Cortex-A9	Scorpion
CPU Instruction Set	x86	ARMv7	ARMv7
CPU Clock Speed	1.5GHz†	1.0GHz	1.3GHz
CPU Threads	2 threads	2 (1 per core)	1 thread
L2 Cache	512KB	1MB	256KB
3D Engine	PowerVR SGX-535	PowerVR SGX-540	ATI
3D Performance	48 million/s	35 million/s	27 million/s
Video Engine(s)	PowerVR VXE / VXD	TI proprietary	Qualcomm proprietary
Video Decoding	1080p HP	1080p HP	720p
Audio Engine	Integrated	Integrated	Integrated
Camera Support	5 megapixels	20 megapixels	12 megapixels
Power Mgmt IC	MSIC	TWL6030	PM7540
Touchscreen Control	In MP20	External	Integrated
TV Output	HDMI	Analog, HDMI	Analog
USB Ports	3 + PHYs	3 + PHYs	1 + PHY
Analog Audio	In MSIC	TWL6040	Integrated
Package-on-Package Memory (PoP)	No	Yes	No
IC Process	Atom: 45nm LP MP20: 65nm LP	45nm LP	45nm LP
Active Power (typ)	1,000mW*	650mW*	450mW*
Chip Package(s)	Atom: 13.8mm BGA MP20: 14mm BGA	12mm BGA	15mm BGA*
Production	2Q10	4Q10 (est)	4Q10 (est)
First Phones	4Q10*	1Q11*	1Q11*
Cellular Baseband	EMP DB3200	Third-party	Integrated
Cellular PMIC	EMP AB3100	Third-party	In PM7540
Cellular RF	EMP RF3300	Third-party	QTR8600
BT+FM+GPS+WiFi	Marvell, Infineon	WiLink 7	QTR8600, WCN1312
Total Chips	8 chips	7 chips	4 chips

Table 3. Comparison of Intel's Moorestown with leading smartphone processors. Moorestown is a big improvement for Intel but still lags behind the integration level seen in competing chips. "Total Chips" includes the application processor, cellular baseband, cellular RF, power manager, Bluetooth, FM radio, Wi-Fi, and GPS chips. †Intel specifies a maximum clock speed at 1.5GHz for smartphones and 1.9GHz for tablets. (Source: vendors, except *The Linley Group estimate.).

pages from popular sites. Intel's own benchmark testing showed that Moorestown can render web pages 2× to 3× faster than unnamed contemporary smartphones. Dual-CPU 1.0GHz Cortex-A9 configurations, however, are likely to deliver 2× to 3× the performance of the 600MHz Cortex-A8 processor in the iPhone 3GS, for example.

A good smartphone requires more than just a fast CPU. On the basis of 3D triangles per second (a poor but widely used graphics-performance metric), Moorestown matches up well against most leading smartphone processors, even exceeding the performance of some, as Table 3 shows. Nvidia's Tegra 2 (not shown in the table) has the handheld 3D lead at 88 million triangles per second.

Video is another important performance factor. Although 1080p support is unusual in today's phones, it is common in next-generation smartphone processors. Not all of these processors, however, can support MPEG4 High Profile at this resolution—a feat that is required to play Blu-ray discs. So far, only Intel and TI (for OMAP4) claim 1080p High Profile support.

Integration Is Better But Not Best

Compared with Menlow, Intel has made significant strides in reducing the system-level chip count for a smartphone. Indeed, the fact that Moorestown can fit into devices such as the Aava Mobile phone and the LG GW990 (see the sidebar, "Atomic Smartphones") indicates that Intel is approaching parity in its level of integration. Integration is tremendously important in handheld devices because it reduces size, power, and (in most cases) cost.

But Intel cannot get around the fact that Moorestown requires two chips to deliver the traditional application-processor features that every other competitor delivers in one chip. Langwell, with its bulky 14mm package, is a device that is completely unnecessary when using competing application processors. As Table 3 shows, TI's OMAP4430 package measures 144mm^2, whereas the two Moorestown chips total 386mm^2—about 2.5× the size. TI's design requires a separate analog audio chip, a function that Intel integrates into Briertown, but that chip adds only 49mm^2 to the OMAP platform. OMAP4 can include a DRAM chip in the same package, however, thereby saving board space. (See *MPR 11/9/09-01*, "More Applications for OMAP4.")

Even application processors such as OMAP4 are becoming passé, however, because OEMs are increasingly turning to integrated smartphone processors that combine the application processor (AP) and cellular baseband (BB) in a single chip. Some chip vendors, including Intel, argue that integrated AP+BB chips aren't necessarily desirable, because they leave less room for OEMs to differentiate their products for different market segments or geographical regions. Also, Intel says that Moorestown is intended for high-end smartphones, tablets, and other handheld computing devices that need less integration than mainstream smartphones do.

Nevertheless, we believe the smartphone industry will continue to move toward higher integration. As Figure 7 shows, despite explosive growth in total smartphone shipments, we expect the number of application processors shipped into smartphones will be stable or shrink slightly over the next several years. The portion of smartphones using integrated processors (AP+BB) will grow from 40% in 2009 to 73% in 2014, according to The Linley Group's forecast.

Qualcomm's smartphone processors set the pace for integration. The Snapdragon QSD8650, for example, includes a complete application processor as well as an HSPA cellular baseband. This integration not only eliminates a separate baseband chip, but it also eliminates the separate power-management IC (PMIC) that it generally requires. (See *MPR 3/22/10-01*, "Snapdragon Success.")

In another feat of integration, Qualcomm has combined the cellular-RF circuitry with complete Bluetooth, FM, and GPS functions, all in a single package (the QTR8600). As a result, a complete smartphone platform can be built from only four chips: the QSD8650, the QTR8600, the PM7540 analog chip, and the WCN1312 for Wi-Fi. As Table 3 shows, this platform requires exactly half as many chips as Moorestown for the same features. Even the next-generation Medfield chip set isn't expected to match Qualcomm's level of integration.

Many smartphone makers prefer to purchase all the chips in a platform from a single vendor. This approach simplifies the design project, eliminates finger-pointing when something goes wrong, and enables the chip supplier to offer bundle discounts (as Intel does with Silverthorne and Poulsbo in the Menlow platform). Vendors such as Broadcom, Qualcomm, ST-Ericsson offer complete solutions. Even TI offers all the components except the cellular

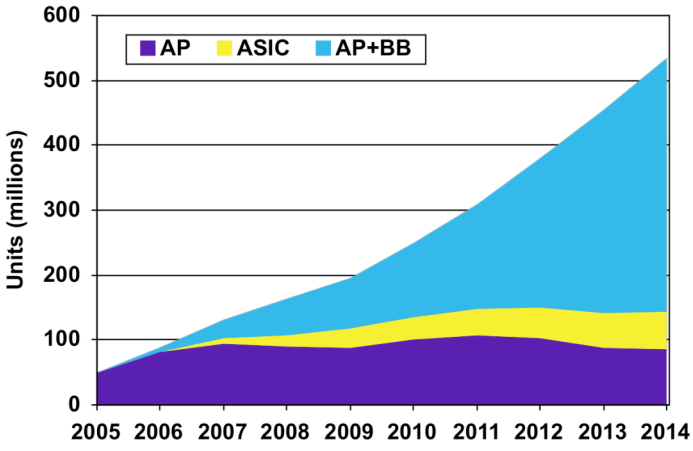

Figure 7. Forecast of smartphone processor shipments from 2005 to 2014. This figure compares shipments of application processors (APs) and integrated processors that also include the cellular baseband (BB). The ASIC category represents Apple's iPhone processors. (Source: The Linley Group)

Price and Availability

Intel's Moorestown chip set for smartphones and tablets is now shipping to customers. Intel-supplied components include an Atom Z6xx-series processor chip (code-named Lincroft) and the Intel Platform Controller Hub MP20 (code-named Langwell). A third chip, the MSIC, is available from Freescale, Maxim, and NEC/Renesas.

Intel isn't publicly disclosing prices for Moorestown devices. We estimate that the smartphone speed grades carry a list price of less than $25 and the tablet speed grades carry a list price of less than $45. For more information, visit: *www.intel.com/pressroom/archive/releases/2010/20100504comp.htm*.

subsystem. The Intel platform, in contrast, requires three to five suppliers. Although large OEMs will not be daunted, smaller phone makers may blanch at the task and may have to pay a design house to help with the project.

One Step at a Time

Despite Intel's market positioning, we find Moorestown more competitive for tablets and midsized devices than for smartphones and other handhelds. The company has made great strides in reducing both the size and power consumption of its Atom products, but the Moorestown phone designs still appear to be a bit too large and a bit too power hungry. Intel hopes that Moorestown will demonstrate superior performance on web-page downloads and other common end-user tasks, but outrunning Cortex-A9 processors will be far more difficult than besting today's older-generation phones. Intel must demonstrate a compelling performance advantage to convince a potential customer to port its entire software stack from ARM to x86.

We expect Moorestown to win a few phone designs, either with small phone makers or in fringe designs from larger OEMs. LG's withdrawal of the Moorestown-based GW990, however, is not a good sign. Intel is proud of its partnership with Nokia, but the world's leading phone maker has made it clear that Meego (and therefore Moorestown) is only for tablets and other emerging devices; it is sticking with Symbian for its mainstream smartphones.

The next turn of the crank is a third-generation Atom-based platform, code-named Medfield. Intel promises that Medfield will be a true single-chip application processor, putting it on a par with products such as OMAP. Medfield will also move to Intel's 32nm process, providing additional power reduction, performance increases, or both. Medfield could even include dual Atom CPUs, providing a potential performance advantage over dual-CPU Cortex-A9 designs. Medfield is scheduled to sample later this year and to appear in smartphones around the end of 2011.

Medfield should give Intel a stronger entrée into the smartphone market, but only into the shrinking portion that relies on standalone application processors. To access the bulk of that market, Intel must integrate a cellular baseband into its processor. The company has a license for Nokia's baseband technology and could create an integrated processor, but such a product would probably not be ready for smartphones until 2012 or 2013, particularly considering the interoperability testing and regulatory qualification required for a new cellular processor. (Intel is also rumored to be considering an acquisition of Infineon's cellular business, a deal that is unlikely to accelerate any integration plans.) Thus, Intel is taking only the first step on a long path toward becoming a leading smartphone supplier.

In the meantime, Moorestown is well suited to the emerging category of tablet computers. Apple has invigorated this category with the launch of its iPad, and a slew of similar products is likely to appear over the next year. In these larger devices, minor differences in processor size and power are not important; the emphasis is on performance. Despite its use of x86 processors in its larger computers, Apple has committed to an internal ARM-based design for the iPad. (See *MPR 4/26/10-02*, "Why Apple Wants Intrinsity.")

Intel's traditional strengths as the world's largest semiconductor company have not yet been fully felt in the handheld market. Intel has vast engineering resources and arguably the best digital-IC fabrication technology on the planet. That combination should allow Intel to design and manufacture the most highly integrated and most power-efficient smartphone processors. Counterbalancing those strengths, however, Intel is handicapped by a CPU architecture that is not renowned for simplicity and low power consumption and that is not as well supported by smartphone software.

Intel's competitors in this market are smaller companies individually, but together, they constitute a powerful coalition behind the ARM architecture—a CPU architecture that *is* renowned for simplicity and low power and that is firmly entrenched among hardware designers and software developers. Collectively, they have far more smartphone-processor design projects underway than Intel does. And because they can license the ARM architecture as well as ARM processor cores, they have more room to differentiate their SoCs. The RISC versus CISC wars of the 1990s have resumed—and, this time, the x86 is the challenger. ♦