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# SUMMER SHOPPING SPREE

## *Intel Buys Cilk Arts and RapidMind; Virage Logic Wants ARC*

*By Tom R. Halfhill {9/14/09-01}*

Three recent business deals are of special interest to programmers and chip developers. First, Intel has acquired Cilk Arts and RapidMind, two small but brainy companies specializing in development tools for parallel programming. Second, Virage Logic is buying ARC International, which will alter the competitive landscape for licensable embedded-processor cores.

All these moves are further evidence that forward-thinking companies are taking advantage of recessionary prices to strengthen their positions for recovery. Intel's late-summer purchases of Cilk Arts and RapidMind (for prices undisclosed) follow its early-summer $884 million acquisition of Wind River Systems. Virage Logic's bid for ARC will add synthesizable microprocessor cores and configurable-processor technology to its growing portfolio of licensable intellectual property (IP).

Although these deals might have happened even without the impetus of a recession, the global economic downturn has beaten down stock prices and weakened many companies whose health was marginal to begin with. (See *MPR 6/29/09-02*, "Tough Times Bring Change.")

### Parallel Minds Think Alike

By acquiring Cilk Arts and RapidMind, Intel is making a strong attempt to improve software development and performance on its increasingly complex multicore processors. Intel already has tools for parallel programming, of course, but the acquisitions bring alternative technologies and fresh engineering talent to Intel's team.

Cilk Arts grew from a project at the Massachusetts Institute of Technology (MIT) and was a privately held company. Cilk++ is an extension of C++ that adds only three new keywords to the language. The Cilk++ compiler and run-time system are compatible with Windows XP and most versions of GNU/Linux. Cilk++ targets 32-bit x86 processors, but Intel will probably add support for 64-bit x86 processors as well.

Proponents claim Cilk++ is easier to learn than alternative parallel-programming languages and is more compatible with existing serial code. Cilk++ includes a "race detector" and new "hyperobject" constructs to prevent race conditions, deadlocks, and other problems associated with multithreaded code. (See *MPR 4/30/07-02*, "The Dread of Threads.")

RapidMind was a private company founded in 2004 and based in Ontario. The RapidMind Multicore Development Platform includes an application-programming interface (API), new constructs for expressing data-level parallelism in C++, and a sophisticated hardware-abstraction layer. This layer includes a run-time code optimizer and a multiprocessor load balancer. Programmers expose data parallelism by writing functions that operate on specially typed arrays.

Thanks to RapidMind's hardware-abstraction layer, a single C++ source can run on different microprocessor architectures. Originally, RapidMind supported IBM's Cell Broadband Engine and the GPUs from AMD/ATI and Nvidia. In 2007, RapidMind added support for the Intel x86 architecture. (For our analysis of the RapidMind platform, see *MPR 11/26/07-01*, "Parallel Processing For the x86.")

Intel says it will continue to sell the RapidMind platform and support RapidMind's customers. As with the Wind River

acquisition, some developers worry that Intel isn't committed to supporting non-Intel CPU architectures in the long term. However, Intel says it stands to win more business by moving the whole industry forward in these areas. In addition, Intel has good reasons to maintain cross-platform compatibility.

### Intel Is Multiplatform, Too

RapidMind's cross-platform features are potentially valuable to Intel. If the RapidMind platform supported Itanium, software developers could easily move parallel code between that architecture and the x86. More likely, RapidMind's processor-agnostic technology would make it easier for developers to move parallel code between Intel's conventional x86 multicore processors and future Larrabee processors. Although Larrabee is based on the x86, there are enough differences from Intel's other x86 processors to make porting more difficult than a simple recompilation.

The first Larrabee chips, expected next year, will probably integrate a dozen or more x86 cores and will be designed for 3D-graphics processing and high-performance computing. Each core will have at least one, and probably several, 16-wide vector-processing units, plus new single-instruction multiple-data (SIMD) operations. The unusually wide vector units provide opportunities for data-level parallelism beyond the multiple cores. In addition, Larrabee supports hardware-managed and software-managed threads for task-level parallelism—a complex multilevel threading model that Intel calls "braided parallelism." (See *MPR 9/29/08-01*, "Intel's Larrabee Redefines GPUs.")

Developers working under nondisclosure agreements have been writing software for Larrabee for more than a year. They've been using Intel's existing parallel-programming tools, but the RapidMind platform is an interesting alternative—especially for existing RapidMind customers that already have production code running on one of the other architectures the platform supports. Moving that code to Larrabee should be relatively easy.

The RapidMind acquisition brings Intel a mature parallel-programming platform that offers programmers a higher level of abstraction than Nvidia's CUDA extensions for C and AMD's ATI Stream. Nvidia has been making great strides with its CUDA development tools and run-time platform for Nvidia GPUs. Some customers are reporting performance gains exceeding two orders of magnitude, and CUDA is taught at 200 universities worldwide. AMD's ATI Stream is a similar solution for ATI GPUs but hasn't caught fire to the same degree. (See *MPR 1/28/08-01*, "Parallel Processing With CUDA," and *MPR 12/22/08-01*, "AMD's Stream Becomes a River.")

However, the Cilk and RapidMind acquisitions pose two challenges for Intel. The first is technical: integrating Cilk++ and the RapidMind platform with Intel's existing parallel-programming tools, run-time platforms, and APIs—or, at least, ensuring peaceful coexistence with them. Intel's second challenge is marketing: helping developers figure out which of these technologies is the best solution for their problem.

### Too Many Choices?

The technical challenge looks formidable. Intel already has its Threading Building Blocks (a C++ template library for multithreading), Intel Parallel Studio (supplemental parallel-programming tools for Microsoft's Visual Studio C/C++), Intel Integrated Performance Primitives (a library of multicore software functions for C++), and a beta version of Intel Ct Technology (data-parallel extensions for C++). In addition, Intel supports OpenMP, an open-standard API for parallel programming in C/C++ and Fortran, and OpenCL, an open-standard framework for parallel programming in C++ on heterogeneous architectures. (See "OpenCL Tries to Standardize Parallel Programming" in *MPR 12/22/08-01*, "AMD's Stream Becomes a River.")

To that smorgasbord, add RapidMind and Cilk++. The first obvious collision is between RapidMind and Ct. Both technologies extend C++ with data-parallel expressions, and both use hardware abstraction to hide the CPU architecture from programmers. Cilk++ appears to overlap Ct, too, as well as duplicating some features of the Threading Building Blocks.

Ct is a beta-stage product, so Intel has time to integrate it with Cilk++ and RapidMind before the formal introduction, planned for next year. In a blog post on the Intel website, Intel engineer James Reinders wrote, "This year we'll introduce the beta for our product based on Intel Ct technology, and next year we'll introduce the result of integration of Cilk++ as well as RapidMind into our product lines...[and] more things to unveil too."

It's not clear how the Threading Building Blocks will fit into the puzzle, or how these acquisitions might alter Intel's roles in the OpenMP and OpenCL consortiums. RapidMind and Ct focus tightly on data parallelism, whereas Cilk++ and the Threading Building Blocks tend to be more general in scope. The Threading Building Blocks are more portable, whereas Cilk++ requires a specially modified compiler. In some cases, a single program might use multiple technologies. But even if Intel can unite these different approaches, budding parallel programmers will face confusing choices for years to come. (See *MPR 7/28/08-02*, "Tools for Multicore Processors.")

Meanwhile, both Apple and Microsoft are introducing 64-bit operating systems with new APIs and other features for parallel processing. In August, Apple released Snow Leopard (Mac OS X 10.6), which supports OpenCL and Apple's new Grand Central Dispatch (GCD) technology. GCD can distribute general-purpose workloads across the processors of a multicore CPU and across the programmable shaders of a GPU. On October 22, Microsoft plans to release Windows 7, whose DirectCompute API also supports general-purpose processing on GPUs. Parallel processing is finally going mainstream.

Intel's marketing challenge is to guide developers toward the best solution for their particular application—and to discourage developers from using competing solutions. Intel must make a persuasive case that its multiplicity of parallel-programming tools won't lead developers into a technical cul-de-sac that strays from emerging industry standards.

### Virage Logic Bids for ARC

While software developers struggle with parallel programming, chip developers are watching Virage Logic's bid to acquire ARC International (formerly ARC Cores). This deal is the most significant alteration of the processor-IP landscape since Tensilica entered the market 11 years ago.

Four companies dominate the market for licensable 32-bit embedded-processor cores: ARM, ARC, MIPS Technologies, and Tensilica. For a long time, *Microprocessor Report* has believed that only two will eventually survive—ARM and one other. ARM is the only company consistently earning healthy profits and consistently growing. MIPS has its ups and downs. Tensilica's fortunes are difficult to measure, because it's the only one still held privately. Founded in 1997, Tensilica has never gained the momentum for a public offering. In June, the company was reinforced by another round of financing led by NTT DoCoMo.

ARC has never been profitable. It was spawned from Argonaut Software in 1995, became a fully independent company in 1998, and went public at the crest of the dot-com boom in 2000. ARC made a dazzling debut on the London Stock Exchange at £2.10 per share and soon soared above £4.00.

Then the dot-com bubble burst. Although ARC isn't a dot-com company, it was dragged down with most other tech-industry stocks and soon was peddling shares for a mere 18 pence. Virage Logic is offering ARC's long-suffering stockholders 16.25 pence, which amounts to £25.2 million ($41 million). The sale was foreshadowed last May when ARC CEO Carl Schlachte was replaced by board member Geoff Bristow, who has been cutting costs to make the company more viable. *[Full disclosure: this writer worked at ARC from 2000 to 2002 but sold all stock upon rejoining* MPR *in August 2002.]*

Virage Logic was founded in 1996 and went public only a month before ARC did in 2000. Like ARC, Virage Logic has struggled for years. Both companies have found the IP-licensing business difficult, mainly because ARM is so dominant. But whereas ARC competes directly with ARM by licensing processor cores, Virage Logic sells other types of IP: physical libraries, peripheral cores (especially I/O controllers), and memory. Even so, there's an uncomfortable overlap with ARM, which also has peripheral IP and a large physical-IP business after spending $913 million to buy Artisan Components in 2004. (See *MPR 9/7/04-01*, "ARM Extends Its Reach.")

By acquiring ARC, Virage Logic is boldly repositioning itself as a direct competitor of ARM. ARC's processor cores and related IP will give Virage Logic a product catalog that nearly matches ARM's in scope. ARM offers a greater number of processor cores, but ARC's processors are configurable, so developers can create a virtually infinite number of variations. Ironically, though, Virage Logic is essentially duplicating a strategy that failed ARC in the early 2000s.

### For More Information

Cilk Arts:
*www.cilk.com*
RapidMind:
*www.rapidmind.com*
Intel's blog post about the Cilk Arts acquisition:
*http://software.intel.com/en-us/blogs/2009/07/31/cilk-intel/*
Intel's blog post about the RapidMind acquisition:
*http://software.intel.com/en-us/blogs/2009/08/19/rapidmind-intel/*
Intel's Ct Technology:
*http://software.intel.com/en-us/data-parallel/*
Cilk Project at MIT:
*http://supertech.csail.mit.edu/cilk/*
EDN's coverage of the RapidMind acquisition:
*www.edn.com/article/CA6685291.html*
ARC International:
*www.arc.com*
Virage Logic's tender for ARC International:
*http://investors.viragelogic.com/releasedetail.cfm?ReleaseID=403723*

### One-Stop Shop for IP

Securities regulations prevent ARC and Virage Logic from saying much about the pending deal, but Virage Logic CEO Alex Shubat told *MPR* that he wants to make his company a "one-stop shop" for licensable IP. If ARC's shareholders approve the sale, chip developers will be able to license from Virage Logic almost everything they need to design an SoC: synthesizable 32-bit processor cores, peripheral soft-IP cores, synthesizable memory, physical libraries, and development tools.

It sounds compelling—but ARC unsuccessfully tried the same strategy 10 years ago. In 1999 and 2000, ARC acquired Metaware, a software-development tools company; VAutomation, a peripheral-IP company; and Precise Software, a system-software company. The goal was the same: assemble a one-stop shop for SoC developers. (See *MPR 4/10/00-03*, "ARC Cores Builds IP Library.")

ARC's strategy was torpedoed by several problems. Integrating these disparate lines of business was difficult, and synchronizing their product releases was almost impossible. Ideally, a new ARC processor core would debut with compatible peripheral cores, newly ported system software, and fully supportive development tools. In practice,

synchronicity was rarely achieved, largely because ARC's engineering resources were too thinly spread.

Integrating and coordinating the management of these lines of business was another obstacle. In addition, ARC was competing not only with powerhouses like ARM, but also with third-party vendors whose only focus was peripheral cores, system software, or tools. And the cellular-telephony boom that lifted ARM to stardom largely bypassed ARC.

After Carl Schlachte became CEO in 2004, ARC shifted away from this broad strategy toward narrower markets. In recent years, ARC has specialized in multimedia, offering preconfigured platforms for audio and video processing. (See *MPR 10/15/07-01*, "ARC Encodes Digital Video.")

### Avoiding the Pitfalls of History

Tensilica and MIPS are becoming more specialized, too. This summer, Tensilica introduced its first processor core optimized for baseband processing, soon followed by a lower-end DSP core. (See *MPR 8/10/09-01*, "Tensilica Plays Baseband.")

MIPS tried to expand its scope in 2007 by acquiring Chipidea, a Portuguese company specializing in analog IP. But in a bruising reverse, MIPS sold that business to Synopsys last May, losing $125 million in the exchange. (See *MPR 6/29/09-02*, "Tough Times Bring Change.")

By reviving the "one-stop shop" strategy that caused so much grief for ARC and MIPS, Virage Logic appears to be thumbing its nose at George Santayana. Nevertheless, CEO Alex Shubat sees an opportunity. The combined company will be larger than ARC ever was, and the combined customer list will be more impressive.

Whereas ARC never had more than 300 employees and has dipped close to 100 after recent cuts, Virage Logic has almost 400 people, even before the acquisition. Shubat told *MPR* that Virage Logic plans to retain most ARC employees, especially in engineering, because there's virtually no product overlap. And Virage Logic has more than 350 customers spread all over the globe, although ARC has a respectable customer base, too.

By assembling a larger organization with enough resources to support a broad product line, Shubat hopes to dodge the problems that wrecked ARC's attempt to become a one-stop shop earlier in this decade. Nevertheless, *MPR* believes that Virage Logic is betting the company on a hard-to-execute strategy. The additional resources will be counterbalanced by the additional direct competition. ARM is an even bigger company with an even more impressive customer base.

### Consolidation Is Inevitable

Intel and Virage Logic are consolidating two different segments of the industry that need consolidation. On the software side, programmers are pleading for solutions to their parallel-programming problems and are bewildered by the number of different answers. By integrating RapidMind and Cilk++ with Ct, Intel can bring a little more coherence to the chaos—though it may come at the expense of non-Intel CPU architectures.

On the hardware side, the problem isn't too many choices—it's that ARM is the only processor-IP company that's thriving. ARC, MIPS, and Tensilica have been merely surviving. Now ARC appears to be leaving the scene as an independent company, seeking refuge in a larger organization. It's still the same fight, though. We expect this segment to eventually contract around two gainfully profitable survivors.