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# TENSILICA PLAYS BASEBAND

## *New ConnX DSP Core Aims for Low-Power Wireless Communications*

*By Tom R. Halfhill {8/10/09-01}*

Tensilica's ConnX Baseband Engine—a CPU/DSP core optimized for wireless baseband processing—signals a new direction for the 12-year-old company. Although Tensilica says most of the 350 million processor cores it has shipped are performing DSP tasks already,

Tensilica has always styled itself as a vendor of configurable RISC CPUs. Now, with ConnX BBE, the company is making a major play for DSPs.

It's easy to see why. The cellphone industry is gearing up for a global transition to fourth-generation (4G) wireless telephony, which will boost data-transfer speeds to about 100Mb/s and make mobile Internet access nearly universal. A likely extension of 4G technology is Long-Term Evolution (LTE), which could reach 1.0Gb/s in advanced phases. Figure 1 shows In-Stat's forecasts for these technologies.

Meanwhile, netbooks, smartphones, and other mobile Internet devices are bridging the gap between voice-oriented cellphones and data-oriented PCs. Some of these devices can connect to either cellular or Wi-Fi networks. Additional wireless opportunities include WiMAX, DTV, terrestrial digital radio, and satellite radio. All told, we're witnessing the biggest explosion in radio communications since the invention of the transistor.

And every "radio"—in this context, the chip-scale wireless transmit/receive unit—needs a baseband processor. The baseband does the grunt work of converting modulated wireless signals into useful digital data, and vice versa. The convoluted signals require several DSP-intensive steps to process, relying heavily on algorithms with complex FFT and FIR filters.

Indeed, some next-generation radios will need multiple baseband engines to shoulder the workload. To meet those needs, ConnX BBE has provisions for multicore designs. Depending on the implementation, Tensilica's baseband engine is suitable for infrastructure equipment (e.g., base stations) as well as for mobile communication devices.

### ConnX Extends Existing Cores

As noted above, most of Tensilica's Xtensa CPU cores are already working as DSPs, at least part time. Tensilica's highly configurable CPUs have offered signal-processing capabilities since 2000, when the optional Vectra DSP extensions for the Xtensa III made their debut. (See *MPR 6/19/00-02*, "Vector DSP, FPU Extend Xtensa.")

In 2004, Tensilica significantly enhanced those capabilities by introducing the Xtensa LX processor and optional

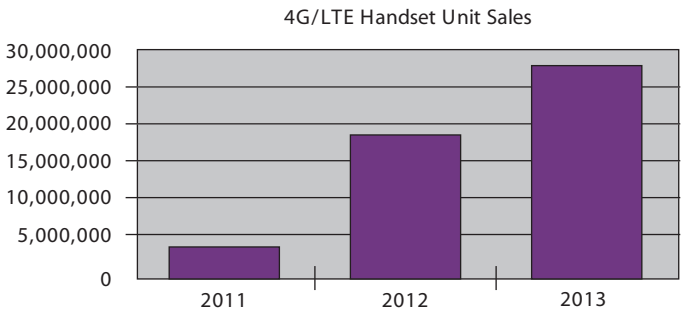


**Figure 1.** In-Stat expects sales of 4G/LTE cellular handsets to reach 27.7 million units in 2013. Although some analysts are predicting much faster growth, In-Stat's forecasts are tempered by the likely slower growth of 4G/LTE networks. (Source: *2Q09 Cellular Subscriptions and Handset Database*, by Scott Scherer, In-Stat research analyst.)

Vectra LX extensions. Vectra LX is a 16-bit fixed-point configurable DSP engine. It uses 64-bit instruction words with three issue slots for ALU, multiply-accumulate (MAC), and load/store operations. (See *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.")

The ConnX family builds on that experience. The foundation of the first ConnX baseband engine is the Xtensa LX2 configurable processor core introduced in 2006. (See *MPR 12/4/06-02*, "Tensilica Upgrades Xtensa Cores.") To this, Tensilica has added the Vectra LX extensions (now renamed the ConnX Vectra DSP Engine) plus new instructions for baseband processing. All together, ConnX BBE has 285 DSP/baseband instructions.

Future members of the ConnX family may build further on this foundation or introduce entirely new cores. Configurability is still very much a feature, so developers can create additional instructions and extensions. Although the ConnX BBE core isn't available for general licensing until September, an unnamed lead customer with early access taped out a design in June.

Tensilica's new strategy is a direct challenge to Ceva, the leading provider of licensable DSP cores. Ceva claims 18% of the total market for basebands, shipping 46 million units in 2Q09, mostly in cellphones. One of Ceva's most notable design wins is the Infineon baseband chip in the hot-selling Apple iPhone 3GS. Among other Ceva licensees are Broadcom, MediaTek, Spreadtrum, and ST-Ericsson.

Another direct competitor for Tensilica is NXP, a corporate descendant of Philips Electronics. In 2007, NXP introduced the CoolFlux BSP, a licensable baseband core. It's much smaller than Tensilica's baseband engine but has less parallelism. NXP says a customer has built the CoolFlux BSP into a WiMAX chip and a 4G baseband.

The biggest player in basebands is Qualcomm—one of many semiconductor companies that sells standard parts, not synthesizable cores. Qualcomm is climbing to the top of the market, because Texas Instruments and Freescale Semiconductor are leaving the baseband merchant-chip business. Note that chip suppliers are potential customers for Tensilica if they license ConnX for future designs.

### Baseband Processors Evolve

Today's baseband processors supplement the DSP core with application-specific logic for the most compute-intensive tasks. But scaling those designs to 4G and LTE technologies may be difficult. When performance requirements outrun the pace of Moore's law, process shrinks alone don't allow conventional DSP cores to keep up. Adding more blocks of dedicated logic isn't always energy efficient and sacrifices programmability. And programmability, or "software-defined radio," is vital for supporting multiple telephony standards in diverse global markets.

Another trend is the integration of baseband processors with application processors, creating hybrids known as communications processors. Today, most cellphones use a DSP for baseband processing and a separate SoC (usually with an ARM processor core) to run the operating system and application software. The baseband chip may also have CPU (often an ARM core) serving as a master controller. Integrating all those functions in a single chip—or in a multichip package—can save money, power, and space.

Tensilica is positioning itself at the intersection of these trends. Fundamentally, the Xtensa LX2 processor is a general-purpose RISC CPU. Signal-processing extensions make it a high-performance 16-bit fixed-point DSP, and additional extensions make it an effective baseband processor. Yet the core retains its ability to run general-purpose software, including control software, because the Xtensa instruction set is intact. Consequently, a multicore design doesn't necessarily need a separate master CPU. And the core remains user configurable, so developers can add extensions specific to their applications, offering a path to differentiation.

Because a ConnX BBE isn't exactly a CPU, a DSP, or even a CPU with ordinary DSP extensions, Tensilica refers to it generically as a data-plane processing unit (DPU). As the term implies, a DPU is intended mainly for running data-plane workloads. Although, theoretically, a ConnX BBE could run control-plane software and application software, the disparate workload wouldn't be optimal. Even if the baseband is integrated with the application processor, the ConnX BBE will most likely work alongside an ARM core—although Tensilica wouldn't mind seeing an Xtensa core in that role, too.

Tensilica isn't a newcomer to this market. The company's existing telephony customers include Fujitsu, NEC, and Panasonic, all of which licensed the Xtensa LX2 last year for next-generation cellphones. In July, Blue Wonder Communications, a German startup, licensed the Xtensa LX2 for a future LTE baseband modem. DesignArt Networks uses Xtensa processors for baseband and control functions in cellular base stations.

Another key relationship was revealed in June. DoCoMo Capital—the investment arm of NTT DoCoMo, Japan's largest cellular network operator—has invested an undisclosed sum in Tensilica. All four of Tensilica's existing venture-capital investors joined the round. It was Tensilica's first outside funding since 2004.

Although Tensilica, like many companies, has suffered layoffs and cutbacks during this recession, CTO Chris Rowen claims the company didn't need the additional funding to survive. Rowen says the money will bolster Tensilica's research and development at a critical juncture. As Tensilica expands its presence in the wireless market, DoCoMo's public endorsement might be more important than the cash investment.

### Inside the ConnX BBE

The ConnX BBE differs from most baseband processors in that it springs from a RISC CPU architecture, not a DSP architecture. That difference isn't necessarily a handicap. Tensilica's 545CK processor—based on the same Xtensa LX2 core as ConnX BBE—is the fastest licensable DSP core on the

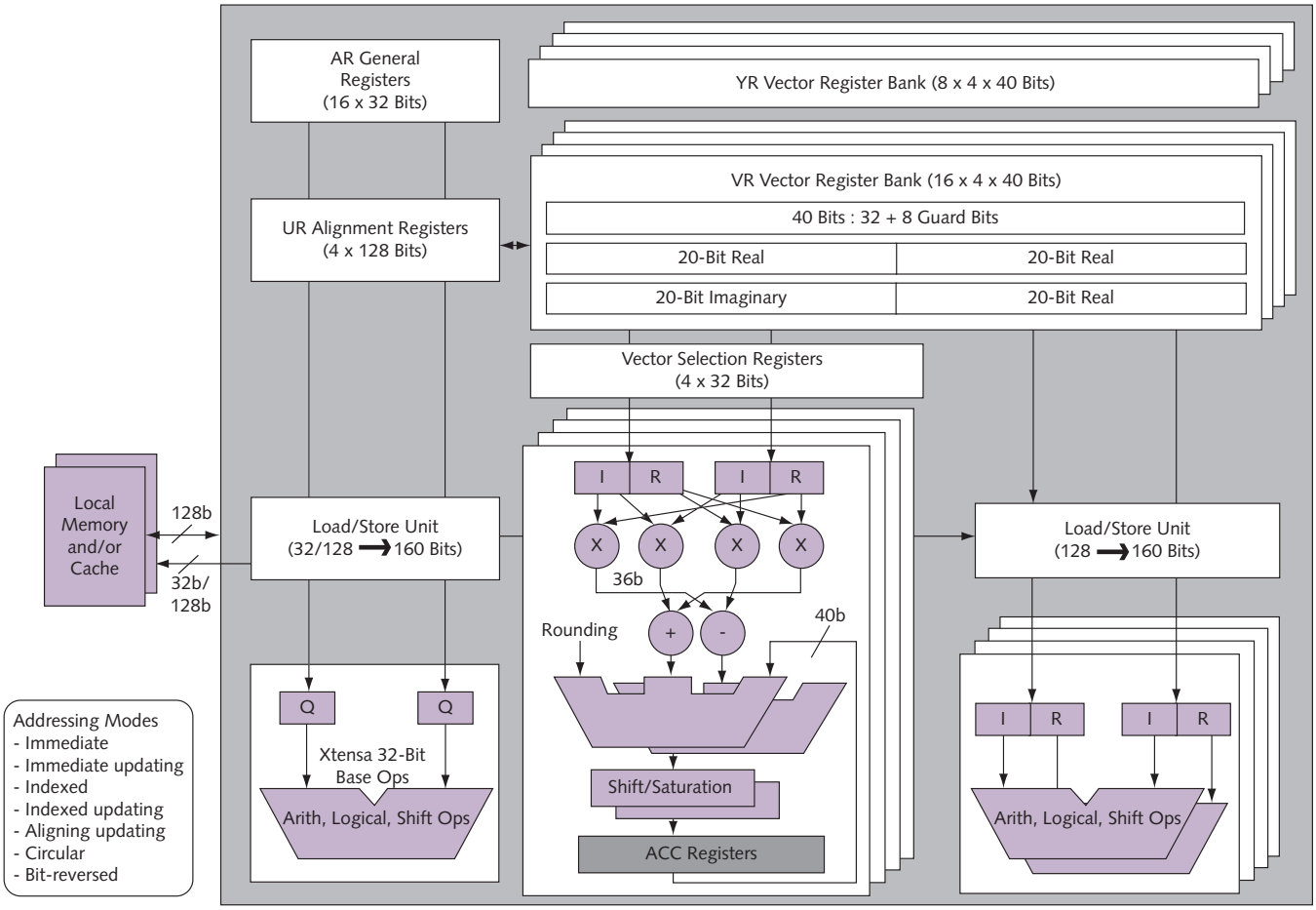


**Figure 2.** ConnX Baseband Engine block diagram. ConnX BBE is based on the Xtensa LX2 core with Vectra LX DSP extensions, but Tensilica has added additional instructions for baseband processing. Note the diverse register files, which avoid contentions for a single bank of registers. The wide load/store units help keep the computation units fed with data.

market, according to BDTI benchmarks. (See *MPR 3/20/06-01*, "Tensilica's Preconfigured Cores.")

That core, formerly known as the Diamond Standard 545CK, has been renamed the ConnX 545CK. "ConnX" is the new umbrella brand for all of Tensilica's communications DSPs, not just the baseband cores. (Tensilica also has audio and video DSPs.)

Figure 2 is a high-level block diagram of the new ConnX BBE. Unusual features are 18-bit multipliers, three-slot VLIW instructions, eight-way SIMD instructions, multiple register files, and dual 128-bit-wide memory interfaces. All these features are inherited from the Xtensa LX2 and Vectra LX.

Most baseband DSPs have 16-bit datapaths. Nominally, the ConnX BBE does, too. In practice, additional guard bits provide extra precision for many operations. ALU instructions and registers that handle 16-bit operands actually represent the values in 20 bits. ALU instructions and registers that handle 32-bit operands represent the values in 40 bits. Multipliers use 18 bits when manipulating 16-bit operands, producing 36-bit results stored in 40-bit registers. SIMD operations include MAC instructions, and the ConnX BBE can execute sixteen 18- x 18-bit MACs in parallel.

Guard bits are common, though not universal, in DSPs. Ideally, to conserve silicon and optimize performance, datapaths and registers should be no wider than they need to be. Ceva's DSPs have 16-bit datapaths with four guard bits per 16-bit operand. Accumulators are 40 bits wide, providing eight guard bits for 32-bit results.

NXP's CoolFlux BSP has 24-bit datapaths, but it also has 28- and 56-bit ALUs and accumulators (including guard bits). Thanks to a suggestion by NXP's lead customer—an undisclosed WiMAX chip vendor—the CoolFlux BSP can split its 24-bit datapaths to handle pairs of 12-bit operations. For example, it can multiply two 12-bit values and store a 24-bit product in a 28-bit accumulator, including four guard bits. As with the extended registers in Tensilica's and Ceva's DSP cores, the extra precision improves the fidelity of signal processing.

## Wider Parallelism With FLIX

Tensilica's baseband engine builds on VLIW and SIMD extensions to the basic Xtensa CPU core. The most powerful DSP architectures that emerged in the 1990s introduced VLIW to signal processing, so it's not surprising that Tensilica followed suit.

| FFT / FIR Filters | 512 Complex Points | 1,024 Complex Points | 2,048 Complex Points | 4,096 Complex Points | 8,192 Complex Points |
|---|---|---|---|---|---|
| FFT (No Bit-Reverse) | 811 | 1,810 | 3,493 | 7,921 | 15,726 |
| FFT (Natural Order) | 853 | 1,812 | 3,630 | 7,930 | 16,247 |
| FIR (8-Tap) | 1,050 | 2,100 | 4,200 | 8,300 | 16,400 |

**Table 1.** ConnX BBE performance for various FFT and FIR functions. Thanks to new instructions added specifically for baseband processing, the ConnX BBE is much faster at these tasks than a Tensilica processor with unmodified DSP extensions. It's three times faster than Tensilica's 545CK processor core, which BDTI has benchmarked as the fastest licensable DSP core on the market. (Data source: Tensilica.)

To be sticky about it, though, Tensilica's implementation is more LIW than VLIW. Instead of the 128- or 256-bit *very long* instruction words that high-end DSPs use, Tensilica uses 64-bit *long* instruction words. Each 64-bit word contains three operations, which can vary in length.

Tensilica built these instructions using its FLexible Instruction eXtensions (FLIX), which allow Tensilica (and its customers) to define their own 64-bit instruction words and operations. Packing three operations into a 64-bit instruction word saves memory and allows the processor to issue all three ops in parallel to different function units. This powerful feature is largely responsible for the stellar performance of the DSP extensions. (See *MPR 11/25/02-06*, "FLIX: The New Xtensa ISA Mix.")

Each 64-bit FLIX instruction word may contain an ALU operation, an 18- x 18-bit MAC operation, and one or two load/store operations. The dual load/store unit has two 128-bit memory interfaces and can sign-extend or round an operand while reading or writing. Programs can freely mix 64-bit instruction words with the 16- and 24-bit RISC instructions (up to 153 of them) that comprise the processor's general-purpose instruction set.

A common drawback of VLIW is that instruction words can't always be filled with useful operations. In those cases, no-operation (NOP) instructions must occupy the empty slots to maintain the uniformity of the instruction words. NOPs waste memory and I/O bandwidth. Although Tensilica's FLIX instructions are subject to this drawback, their relatively short length (64 bits instead of 128 or 256 bits) minimizes the problem.

```
short a[128], b[128];
void conv()
{
  int i;
  for (i=0; i<128; i++) {
    a[i] = b[i] + b[i-1];
  }
}
```

```
loopgtz a4,.LBB30_conv
{ lvs16a.iu v2,u0,a2,16;
  mov160 v1,v0;
  mov160 v0,v2; }
{ svs16.iu v4,a3,16;
  sel v3,v2,v0,s0;
  add20 v4,v3,v1; }
```

**Figure 3.** Tensilica's compiler converts ANSI C into vectorized machine code for the three-slot 64-bit instruction words. In this example, a small C function (top) has a 128-iteration loop. The compiler decomposed the loop (bottom) into two instruction words—each with three operations—and only 16 iterations.

## New Baseband Instructions

ConnX BBE's special ingredient is the new instructions created specifically for baseband processing. As with all other extensions to the basic Xtensa processor core, Tensilica wrote the instructions in Tensilica Instruction Extension (TIE) language, a proprietary HDL resembling Verilog.

Before synthesizing the core, developers can use Tensilica's configuration tools to choose which DSP and baseband instructions to implement. Omitting unwanted instructions will save a little silicon and power. If developers implement all the options, 285 instructions will be added to the base instruction set.

Of particular note are new instructions for optimizing fast Fourier transforms (FFT) and finite impulse response (FIR) filters—often-used functions in baseband processing. Some instructions can perform a radix-2 or radix-4 butterfly function in a single clock cycle. Others are optimized for the fused multiply-add operations typically used in FIR filters. SIMD instructions can perform 4, 8, or 16 operations in parallel. As many as sixteen 18- x 18-bit MACs can execute per cycle. Table 1 lists some performance statistics of a ConnX BBE engine.

Despite its RISC CPU ancestry, ConnX BBE has all the conveniences of a modern DSP: zero-overhead looping, flexible addressing modes, complex instructions combining two or more arithmetic operations, numerous bit-manipulation instructions, and multiply instructions with saturation or rounding. Many instructions are designed to reduce the overhead of loads and stores. For instance, the processor can use the full width of its 128-bit I/O interfaces even when reading or writing unaligned data.

The large instruction set would be intimidating if programmers had to write their code in assembly language. Although DSP programmers are among the last assembly holdouts, Tensilica says compiled C is entirely practical with ConnX BBE. Indeed, so far, Tensilica has written all its ConnX function libraries in C. The secret is Tensilica's vectorizing compiler, which translates high-level code into parallel machine code. Figure 3 shows an example.

If necessary, programmers can write assembly code for ConnX BBE, but the complexity of a

VLIW/SIMD architecture is a strong deterrent. Writing the code is almost secondary to scheduling the code, and efficient scheduling requires thorough knowledge of the capabilities of the function units and capacity of the I/O interfaces.

### Multiple Cores Add Performance

Figure 4 illustrates a typical single-core implementation using ConnX BBE with a bridge to an AHB or AXI system bus. Tensilica's proprietary Processor Interface (PIF) is designed to be agnostic in this respect—it's capable of connecting to almost any on-chip network through a low-latency bus bridge. Developers can configure the PIF to widths up to 128 bits. However, note that some DSP cores (such as Ceva-XC) natively support AHB/AXI buses without a bridge.

For next-generation cellphones, one baseband engine may not suffice. Tensilica estimates that the baseband processor in an LTE phone will need to execute 15,000 complex (2K) FFTs per second to decode signals received by the antenna—and that's for only one antenna. LTE phones will probably have two to four antennas in a multiple-input, multiple-output (MIMO) array. MIMO arrays allow the phone to transmit and receive a signal that's duplicated on multiple channels. This technique reduces the signal degradation caused by multipath reflection, the phone's mobility, and other sources of interference.

Ceva claims its licensees are finding that a single Ceva-XC core delivers enough performance for next-generation 4G/LTE phones, at least for speeds up to LTE CAT5 (300Mb/s). However, Tensilica anticipates that multiple ConnX BBE cores will be necessary and is estimating the performance of clusters with up to eight cores.

Tensilica offers two options for intercore communication: hardware message passing and distributed shared memory. Both provide high bandwidth, but they have different trade-offs and programming models. Some developers may prefer

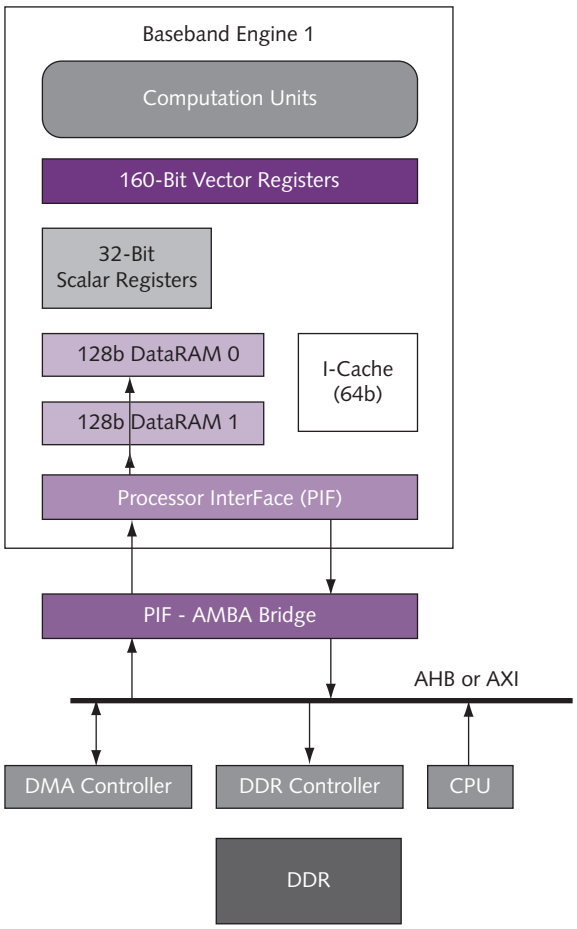


**Figure 4.** System I/O with a single-core ConnX BBE design. Although this example has a bridge to an AHB bus, Tensilica's Processor Interface (PIF) works with virtually any bus; Tensilica provides an AMBA bridge with the core. The DMA and DDR controllers shown here are third-party IP blocks. The CPU could be another Tensilica Xtensa core or any other processor.

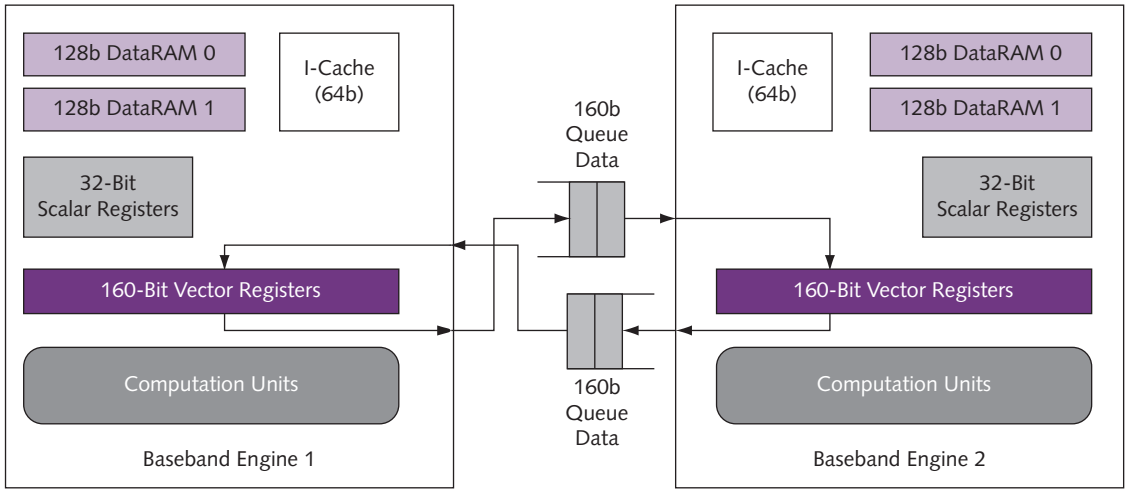


**Figure 5.** Hardware message passing in a dual-core ConnX BBE design. Special queues with hardware handshaking link the cores directly together, reducing synchronization overhead. Queues are user-configurable, up to 160 bits wide. Note that a full-width queue matches the capacity of a ConnX BBE 160-bit vector-register file. Each core has two such files, which can store four 40-bit values or eight 20-bit values.

the programming model they used in a previous design. In other cases, developers may wish to use both methods.

Figure 5 illustrates hardware message passing, which is more efficient for workloads requiring frequent synchronization. For example, if two cores execute a loop in parallel and exchange data after each iteration, the ratio of synchronization to data transfers is relatively high. Hardware message passing reduces that overhead by wiring the cores directly together through special queues. The configurable queues can be 160 bits wide, providing 8GB/s of bandwidth at 400MHz. Hardware handshaking minimizes the time spent synchronizing a shared workload, but it's probably less efficient than an alternative solution that gets by with only one core.

Figure 6 illustrates Tensilica's distributed shared-memory model. It ties all cores together using 128-bit interconnects linked to their PIFs. This method is more efficient when the cores share relatively large amounts of data with less frequent synchronization. Software manages the synchronization while exchanging data through a shared-memory buffer. One core must fill the buffer and release it before another core can access it. This model tends to be more cost effective, because RAM arrays are cheaper than implementing FIFO buffers in hardware.

### Accommodating Additional Logic

In a shared-memory model, the aggregate intercore bandwidth varies, depending on the number of cores. A dual-core design can exchange 32 bytes per cycle (12.5GB/s at 400MHz). An eight-core design can exchange 128 bytes per cycle (50GB/s at 400MHz).

Note that neither method of intercore communication—shared memory or message passing—limits the I/O bandwidth for load/store operations. Each core can write 16 bytes per cycle to its internal data RAM, read 16 bytes per cycle from internal data RAM, and read or write 16 bytes per cycle to another core in the cluster, simultaneously.

It's possible to combine the two intercore-communication models. A hybrid design might use shared-memory buffers to exchange large blocks of data while using queues and hardware handshaking to manage synchronization. To reduce design complexity, the queues could be only 32 bits wide and could communicate through general-purpose registers instead of vector registers. This hybrid approach would simplify programming somewhat, because synchronization needn't be handled in software. However, software partitioning and task scheduling would still require some attention.

The number of ConnX BBE cores required for a design depends on the application and on the amount of application-specific logic in the signal chain. Tensilica acknowledges that ConnX engines won't replace all the dedicated logic. Sometimes, developers prefer to reuse logic from a previous design instead of porting the task to a programmable DSP. In other cases, dedicated logic remains more efficient than a programmable processor.

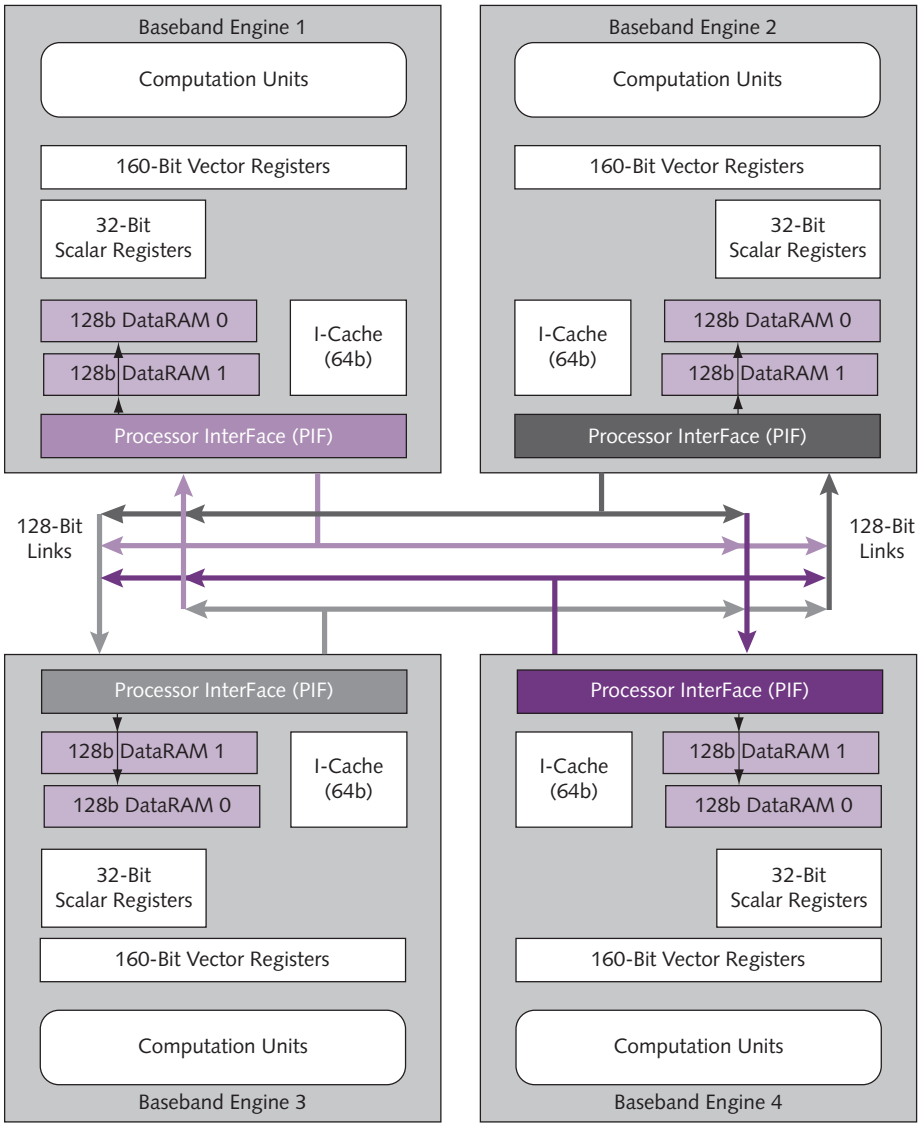


**Figure 6.** Distributed shared memory in a quad-core ConnX BBE design. In this model, the engines exchange information through shared-memory buffers, with software handling the synchronization. The engines communicate over their 128-bit processor interfaces. Tensilica provides SystemC models for these multicore designs—both a cycle-accurate model and a faster bit-accurate model.

Likely candidates for auxiliary logic blocks are the Viterbi decoder, Turbo decoder, and hybrid automatic repeat request (HARQ) unit. All play important roles in error correction and signal fidelity. Figure 7 illustrates Tensilica's concept for the input chain of an LTE radio.

Developers can integrate application-specific logic directly with the core instead of attaching the blocks to a bridged I/O bus. The core's HDL has special "hooks" for this purpose, plus new instructions for interacting with the logic. In effect, the dedicated logic becomes part of the core, operating virtually as a peer to the processor's own function units. Developers can integrate any number of logic blocks in this manner. It's like having an unlimited number of "pins" for tightly coupled logic.

### Growing Competition for DSPs

ConnX faces two kinds of competition. One kind is the baseband chips sold as standard parts by the likes of Broadcom, Ericsson, Freescale, Icera, Infineon, InterDigital, MediaTek, Sandbridge, STMicroelectronics, Qualcomm, and others. (TI and Freescale are bailing out of this crowded business, leaving Qualcomm as the market leader.) But some of these competitors are potential customers, if Tensilica can sell them a ConnX license for their next-generation chips.

The other competition is more direct: companies such as Ceva and NXP that, like Tensilica, sell baseband DSP cores as licensable intellectual property (IP). Both kinds of competition will flourish in the marketplace for years to come. Standard parts are less flexible but readily available off the shelf. Licensable cores offer more design freedom, but designing a custom chip is costly and time consuming.

Core licensing is Tensilica's bread-and-butter business. For years, however, Ceva has been the leader in licensable DSP cores, making it the company to beat. The latest Ceva-XC core is based on the Ceva-X DSP, which is already shipping in volume in 3G and 3.5G baseband chips. This foothold gives Ceva an advantage when competing for next-generation designs, because developers can reuse their software with Ceva-XC.

NXP's CoolFlux BSP is an up-and-coming contender. NXP created this baseband core by extending the CoolFlux DSP audio processor, much as Tensilica customized the Xtensa LX2 processor to make ConnX BBE. Although little was known about the CoolFlux BSP until recently, NXP has been quietly licensing the core since late 2007.

Both Tensilica and Ceva use VLIW for instruction-level parallelism and SIMD instructions for data parallelism, but the similarities pretty much end there. Tensilica's VLIW has three slots, and only one slot can have a SIMD instruction if the others have load/store instructions. Ceva-XC uses six-slot VLIW, and four slots can have SIMD instructions in parallel with a dual load/store.

For wider parallelism, Tensilica encourages developers to add cores. Ceva lets developers use multiple cores, too. But before crossing that bridge over troubled water, developers can configure a single Ceva-XC core with one, two, or four vector-processing units. Both companies can claim performance advantages, depending on the task. Ceva's emphasis on single-core performance reduces design complexity and simplifies programming.

NXP's CoolFlux BSP is a relatively conservative design with less parallelism than the fancy VLIW and SIMD technology in the ConnX BBE and Ceva-XC. CoolFlux SIMD instructions can execute only four operations at once. If a design needs more performance, NXP tells customers to use multiple cores, as Tensilica does. Another option is to use

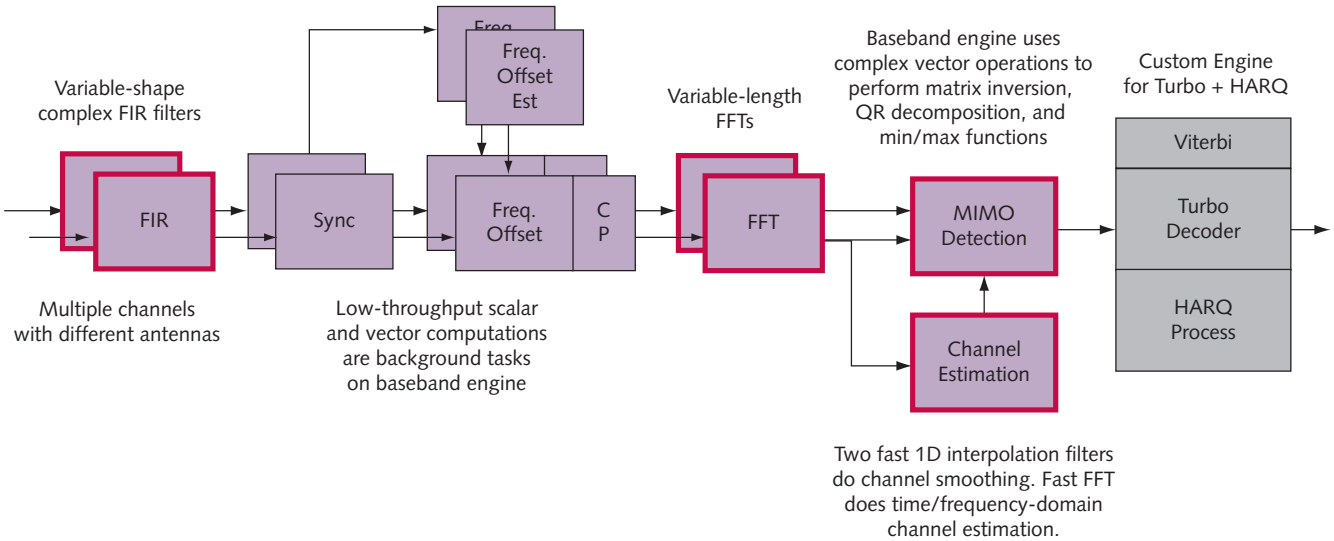


**Figure 7.** The radio for an LTE phone will need a combination of programmable signal processing and application-specific logic. In this conceptual design of the input chain, Tensilica expects ConnX BBE to handle all the tasks shown in purple. Blocks outlined in red are particularly compute-intensive. Gray blocks at the far right indicate tasks better handled with dedicated logic.

more hard-wired logic. However, CoolFlux lacks the built-in features for multicore integration and tightly coupled logic found in Tensilica's baseband engine.

The standout feature of the CoolFlux is its small size: only 65,000 gates when synthesized for maximum clock speed. In contrast, an area-optimized ConnX BBE core requires at least 250,000 gates, and a speed-optimized core will have about 400,000 gates. On the other hand, a CoolFlux design would need four or five cores to match the parallelism of the ConnX BBE or Ceva-XC. NXP's philosophy is that more cores are better than larger cores, because critical paths tend to be shorter.

Table 2 summarizes the features of these licensable baseband cores. NXP is boldly quoting power consumption and maximum worst-case clock frequency in a specific fabrication process (65nm-LP, standard voltage threshold). Thanks to its small, efficient core, the CoolFlux BSP's power consumption is admirably low, dropping to 31 microwatts per megahertz at 0.8V. Unfortunately, neither Tensilica nor Ceva has released enough data to compare these vital metrics. Tensilica says ConnX BBE can reach 400MHz in a 65nm-LP process or 500MHz in 65nm-GP. Ceva says the Ceva-XC core can exceed 400MHz in 65nm-LP and 650MHz in 65nm-GP.

Of course, all these companies will share more data with prospective customers under a nondisclosure agreement. Without detailed information about the synthesis parameters and fabrication processes, it's impossible to make apples-to-apples comparisons. In particular, a GP process is more suitable for chips designed for infrastructure equipment, whereas an LP process is more suitable for mobile applications—and these process variations aren't directly comparable. In addition, important parameters of these processes vary from one foundry to another.

## Signal Processing Is Everywhere

Tensilica is doubling down in a highly competitive market, but it's a clear growth market. Smartphones like the Apple

| Feature | Tensilica ConnX BBE | Ceva Ceva-XC | NXP CoolFlux BSP |
|---|---|---|---|
| **CPU / DSP Arch.** | Xtensa LX2 | Ceva-X DSP | CoolFlux DSP |
| **Configurable ISA** | Yes | Preconfigured options | — |
| **DSP Datapaths** | 16 bits (Range: 16–40 bits) | 16 bits (Range: 8–40 bits) | 24 bits (Range: 12–56 bits) |
| **CPU Instructions** | 16 or 24 bits | 16 or 32 bits | 16 bits (typical) |
| **DSP Instructions** | 3-issue VLIW | 6-issue VLIW | 32 bits (typical) |
| **Data-Memory Interface** | 256 bits (2 x 128 bits) | Up to 2,048 bits | 48 bits (2 x 2 x 12 bits or 2 x 24 bits) |
| **Maximum Throughput** | > 80 ops per cycle (18 bits) | Up to 400 ops per cycle (16 bits) | 20 ops per cycle (12 bits) |
| **MAC Throughput** | 16 (18x18-bits) per cycle | 64 (16x16-bits) per cycle | 4 (12x12-bits) per cycle<br>2 (24x24-bits) per cycle |
| **Complex FFT Throughput** | 4 per cycle (Radix-2 butterfly) | Up to 16 per cycle (Radix-2 butterfly) | 0.5 per cycle* (Radix-2 butterfly equivalent) |
| **FIR Throughput** | 4 x 18-bit complex taps per cycle | Up to 16 x 40-bit complex taps per cycle | 2 x 28-bit complex taps per cycle |
| **MIMO Instructions** | Yes | Yes | — |
| **Software Libraries** | FP, Turbo, Viterbi, AES, DES | FP, Transmitter, MLDE, Cordic | Math, Viterbi, OFDM, QAM, FSK, QPSK |
| **Core Frequency** | 500MHz (65nm-GP) | > 650MHz (65nm-GP) | 290MHz (65nm-LP SVT) |
| **Core Size** | 250K–400K gates (area–speed opt.) | n/a | 65K gates (speed optimized) |
| **Power Consumption (Dynamic)** | n/a | n/a | 31µW / MHz @ 0.8V<br>70µW / MHz @1.2V<br>(65nm-LP SVT) |
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**Table 2.** Feature comparison of the Tensilica ConnX Baseband Engine, Ceva-XC DSP, and NXP CoolFlux BSP. All are licensable, fully synthesizable DSP cores for baseband processing. Ceva is the market leader. The Ceva-XC was designed specifically for basebands, whereas ConnX BBE is a heavily customized version of Tensilica's configurable Xtensa LX2 processor, and the CoolFlux BSP descends from an audio DSP. *CoolFlux is oriented to radix-4 operations and can perform a radix-4 butterfly in eight cycles, equivalent to a radix-2 butterfly in two cycles. n/a: data not available. (Data sources: Tensilica, Ceva, NXP.)

iPhone, Palm Pre, and RIM Blackberry have energized the industry while creating more demand for cellular-network bandwidth. Voice calls, email, and text messaging were relatively easy applications to tackle. Web browsing, social networking, mobile video, and online gaming are another matter. Cellular networks and handsets are becoming much more sophisticated, placing heavier loads on baseband processors.

Separate baseband chips dominate in cellphones today. But as application processors and basebands become integrated in the same chip—or in the same multichip package—the demand for licensable DSP cores is bound to rise.

Tensilica has already wedged a foot in the baseband door by licensing the Xtensa LX2 processor to Fujitsu, NEC, Panasonic, and Blue Wonder Communications. Because ConnX BBE builds on Xtensa LX2, it's a logical choice for those companies' next-generation designs. And DoCoMo's vote of confidence doesn't hurt.

However, this first ConnX engine probably isn't the best solution Tensilica can devise. At its roots, it's a heavily customized general-purpose RISC processor. Although the baseline Xtensa LX2 core is a mere 15,000 gates in a baseband engine with 250,000 to 400,000 gates, it still outlines the framework of the architecture. Perhaps a future member of the ConnX family will introduce a more streamlined microarchitecture created specifically for baseband processing.

### Circumventing ARM

Tensilica's baseband strategy finds a niche for licensable processor cores not yet ruled by ARM. Although ARM is huge in cellphone application processors and baseband controllers—worldwide, ARM averages two cores per handset—its DSP credentials are not as strong. ARM is rumored to be working on a baseband coprocessor but hasn't announced it yet.

For now, ARM's challenge is maintaining its lead in application processors, which face obstacles of their own. They need more and more performance without busting the power budget, and Intel wants to muscle in with the x86—a fight that will keep ARM plenty busy.

As the action shifts away from desktop PCs, Intel is becoming interested in other aspects of cellular telephony as well. In June, Intel announced a relationship with Nokia that includes licensing Nokia's 3G wireless-modem technology for the x86. In 2003, Intel announced an XScale-centric strategy for software-defined radio. (See *MPR 6/9/03-01*, "Intel Maps Wireless Future.") In 2006, Intel changed course to an x86-centric strategy by selling most of its XScale business to Marvell. (See *MPR 7/31/06-01*, "Intel's Embedded Future.")

In basebands, Ceva is clearly the stiffest competition for Tensilica. However, if Tensilica can become a major player in basebands, that success would create new opportunities in other DSP applications, too. That's very important, because the DSP market is rapidly changing.

Sales of discrete DSP chips are falling fast. Nevertheless, signal processing remains a growth market, because more applications demand it. Signal processing is simply migrating from discrete chips to SoCs—the realm of licensable-IP cores. If Tensilica can capture some high-volume baseband design wins, perhaps it can ride this wave to the profitability and initial public offering that has eluded the company for 12 years.

### Price & Availability

Tensilica's new ConnX Broadband Engine will be available for general licensing in September. The licensing fee has not been publicly disclosed. The unnamed lead customer—a new Tensilica licensee—obtained early access to the core and taped out a design in June.

Two existing products have been renamed to join the new ConnX family. The Diamond Standard 545CK processor core is now called the ConnX 545CK DSP, and the Vectra LX DSP extensions are now called the ConnX Vectra DSP Engine. For more information:

- *www.tensilica.com/products/dsps/connx-baseband-engine.htm*
- *www.tensilica.com/products/dsps/545ck-new.htm*
- *www.tensilica.com/products/dsps/connx-vectra-dsp-engine.htm*