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Intel's New SoCs

Pre-Atom Integrated Chips Face Tough Competition

By Tom R. Halfhill {8/18/08-01}

The embedded-processor market resembles a wild costume party, with variety galore—from Little Bo Peep (8-bit MCUs) to the Incredible Hulk (massively parallel DSPs). Into this colorful riot wanders Intel, casually dressed by The Gap for a come-as-you-are party.

Intel's first x86-based SoCs, announced July 23, are attired less appropriately than Intel would like. For now, they combine a PC processor core, a PC north-bridge chip, a PC south-bridge chip, and (optionally) a cryptography-acceleration chip. Consequently, they are relatively large and power hungry when compared with competing SoCs. But they are also fast, highly integrated, and definitely better than a cobbled-together system using three or four separate Intel chips.

More important, they are merely a hint of things to come. Future products will substitute the new Atom x86 processor core for the Pentium M "Dothan" core that was handed down to Intel's SoC architects from the PC division. Atom is a smaller, lower-power core that will make Intel's x86 SoCs more competitive with chips based on the ARC, ARM, MIPS, Power, SPARC, Tensilica, and other RISC architectures. The Atom core wasn't finished until early this year, so it won't appear in SoCs until late 2009 or 2010. (See *MPR 4/7/08-01*, "Intel's Tiny Atom.")

Until then, the Dothan-based EP80579 (code-named Tolapai) is Intel's debut in the extremely competitive market for networking and communications chips. Counting different speed grades and integration options, the EP80579 is available in eight varieties, including two parts specified for industrial temperatures. And Intel is promising seven-year availability—a minimum requirement for some embedded-system developers. Additional x86-based SoCs, coming in 2009 or 2010, will target consumer electronics, mobile Internet devices (MID), and smartphones. (The consumer-electronics SoCs are code-named Canmore and Sodaville; the SoC for MIDs and smartphones is code-named Lincroft.)

Intel's biggest challenge isn't developing state-of-the-art SoCs. For that, the Silicon Valley giant already has everything it needs: processor cores, peripheral cores, engineering resources, the world's best high-volume fabrication technology, and ample manufacturing capacity. When necessary, Intel is even willing to license additional intellectual property (IP) from other sources.

No, the biggest challenge for Intel is convincing customers they need an x86-based SoC instead of a more established RISC-based chip. Competitors offer more choices, more processor cores, higher performance, lower power, smaller packages, longer availability, lower prices, and undivided attention on the embedded market. It's a far cry from the cloistered world of PC processors, where Intel rules supreme over two much smaller competitors.

Tolapai Unveiled: the EP80579

Previously known as Tolapai, the EP80579 is Intel's first highly integrated x86-based SoC. Although Intel has always produced "embedded" x86 processors, those chips are essentially hand-me-down PC processors, not purpose-built embedded designs. They have nowhere near the level of integration seen in the EP80579. The new chip has more in common with Intel's XScale devices, which were based on the StrongARM processor core acquired from Digital in 1997. Intel sold most of its XScale business to Marvell Technology Group in 2006. (See *MPR 7/31/06-01*, "Intel's Embedded Future.")

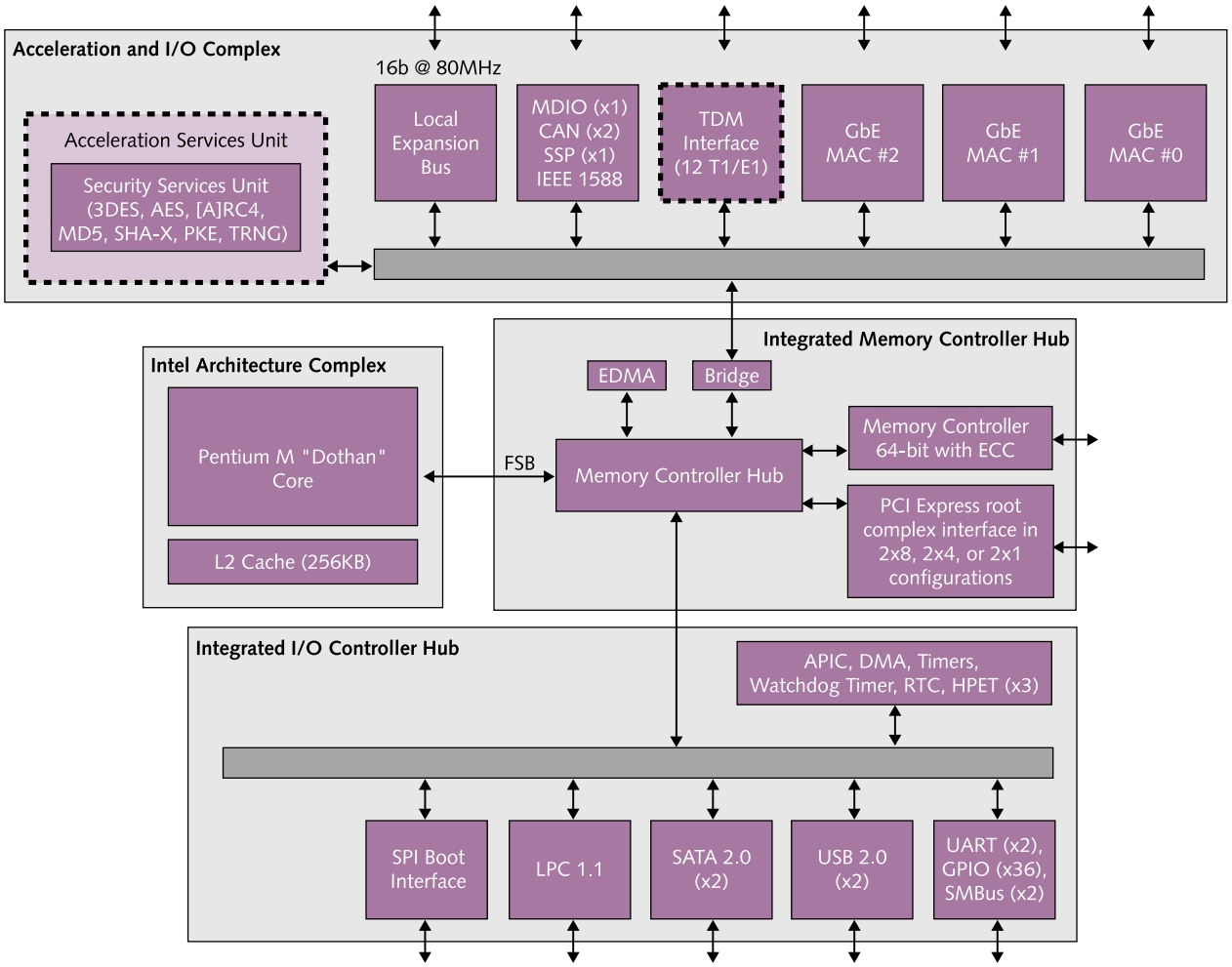

Figure 1. Intel EP80579 block diagram. In addition to having a Pentium M "Dothan" x86 processor core with 256KB of L2 cache, this SoC integrates the functions of PC north-bridge and south-bridge chips. Four of the eight parts in the family also integrate the equivalent of a security-acceleration chip. (The optional acceleration hardware is marked with dotted lines in this diagram.) Although the EP80579 has an impressive level of integration, Intel may prune future devices to optimize them for narrower applications. Migrating to the lower-power Atom processor core and 45nm CMOS process should reduce power consumption.

At that time, *Microprocessor Report* noted that Intel planned to revive the x86 as an embedded-processor architecture. To do that, Intel needed a lower-power x86 core. Atom is the result of that project. But chip designers need 18 to 24 months to wrap an SoC around a new processor core, so, for now, the EP80579 uses the tried-and-true Dothan core. There's nothing wrong with Dothan, except that it was designed to meet PC performance requirements, not embedded power-consumption requirements. Introduced in 2004, Dothan is the 90nm version of the original "Banias" Pentium M processor that debuted in 2003. (See *MPR 5/24/04-02*, "Dothan by the Numbers.")

Likewise, the EP80579 is fabricated in 90nm CMOS—two generations behind the 45nm process that Intel uses for its latest PC and server processors. By itself, 90nm fabrication isn't a handicap in the embedded market. Few, if any, competing chips are manufactured in newer processes, and some are still made in 0.13-micron processes. However, competing SoCs have smaller RISC cores designed for lower power consumption, and competing roadmaps anticipate 45nm fabrication by 2010. Intel's Atom-based SoCs will reach 45nm by then, which will set up a very interesting competition.

Meanwhile, the Dothan-based EP80579 holds down the fort. CPU clock frequencies range from 600MHz to 1.2GHz. Depending on the specifications of these parts—mainly clock speed and optional security features—Intel estimates the maximum power consumption at 11W to 21W. That power estimate is Intel's "thermal design power" (TDP), a worst-case measure that system designers must consider for cooling requirements. Intel hasn't estimated "typical" power consumption for the EP80579 family, but the TDPs are a few watts higher than maximum-power specifications for most competing chips.

Feature	Intel EP80579 EZ600C	Intel EP80579 EZ600CT	Intel EP80579 EZ004C	Intel EP80579 EZ009C	Intel EP80579 EB600C	Intel EP80579 ED004C	Intel EP80579 ED004CT	Intel EP80579 ED009C
Core Freq	600MHz	600MHz	1.066GHz	1.2GHz	600MHz	1.066GHz	1.066GHz	1.2GHz
Memory Freq	400MHz 533MHz 667MHz	400MHz 533MHz 667MHz	400MHz 533MHz 667MHz 800MHz	400MHz 533MHz 667MHz 800MHz	400MHz 533MHz 667MHz	400MHz 533MHz 667MHz 800MHz	400MHz 533MHz 667MHz 800MHz	400MHz 533MHz 667MHz 800MHz
QuickAssist	—	—	—	—	Yes	Yes	Yes	Yes
Temp Range	0° to 70°C	–40° to +85°C	0° to 70°C	0° to 70°C	0° to 70°C	0° to 70°C	–40° to +85°C	0° to 70°C
Power (TDP)	11W	11W	18W	19W	13W	20W	20W	21W
Price (1KU)	$40	n/a	n/a	$65	$54	n/a	n/a	$95

Table 1. Summary of distinguishing features among the eight parts in the Intel EP80579 family. Intel says all these chips will be available in quantity this quarter. Power consumption is Intel's thermal design power (TDP), a maximum rating. QuickAssist is Intel's brand name for specialized acceleration technology, in this case taking the form of optional security-acceleration hardware. Temperature ranges are for ambient air at the heatsink, not the junction temperature (T_j) that is commonly cited by other vendors. Intel hasn't published the T_j for these parts. (n/a: data not available.)

We'll make specific comparisons with those chips later. At this time, however, power consumption isn't the main story, because the future Atom core and two-generation process shrink will go a long way toward addressing that concern. More important for now is the level of integration, which determines how effectively the EP80579 stacks up against other SoCs.

PC Heritage Is Apparent

In some ways, the EP80579 is *too* highly integrated. It absorbs all the functions of a PC north-bridge chip (the Intel 915GME Memory Controller Hub) and a PC south-bridge chip (the Intel ICH6-M I/O Controller Hub). Consequently, it inherits a few features unneeded by some embedded systems for which it's intended. For instance, the EP80579 has two Serial ATA (SATA) interfaces for attaching hard-disk drives, when even one SATA interface might be considered luxurious. Such luxury isn't always desirable in the power- and cost-conscious embedded market. It's no surprise that the EP80579 is packaged in a flip-chip ball grid array (FCBGA) with 1,088 contacts—300 more than some competing SoCs.

In most respects, however, the EP80579 is well suited for networking and communications. It has three Gigabit Ethernet controllers, two USB 2.0 host controllers, a 64-bit DDR2 memory controller with ECC protection, a PCI Express controller supporting three configurations (1×8, 2×4, or 2×1 lanes), and two control-area network (CAN 2.0b) interfaces. And those are just the major features. Other accoutrements include a 16-bit local-expansion bus, a Serial Peripheral Interface (SPI) boot controller, a Synchronous Serial Port (SSP), a Low Pin Count (LPC 1.1) interface, two 16550-compatible UARTs, 36 general-purpose I/O (GPIO) ports, and two System Management Bus (SMBus) interfaces that can serve as I^2C interfaces. Figure 1 shows a block diagram of the EP80579.

Four parts in the eight-member EP80579 family have special hardware for accelerating the cryptographic functions associated with network security, a common feature in this class of device. All told, the characteristics that distinguish members of this family from each other are the optional accelerators, the clock frequency of the CPU core, the clock frequency of the DDR2 memory interface, and the temperature rating (commercial or industrial). Table 1 summarizes these differences.

The EP80579's optional QuickAssist hardware consists of programmable RISC processors with a proprietary Intel instruction set. Intel adapted these processors from the microengines in the IXP1200 network processor, introduced in 1999. (See *MPR 9/13/99-01*, "Intel Network Processor Targets Routers.")

Although the RISC microengines are programmable, they are transparent to software developers. Programmers tap their functions through an application-programming interface (API) that is part of Intel's QuickAssist technology. Actually, QuickAssist is an umbrella term describing multiple approaches to application acceleration. In the context of the EP80579, QuickAssist refers to the optional hardware for accelerating security functions and to the software drivers encapsulating the APIs. Intel will deliver different QuickAssist drivers for different types of embedded applications.

When a program makes a QuickAssist function call, the function executes much faster if the processor has QuickAssist hardware. Otherwise, the function executes on the x86 CPU. This concept is analogous to floating-point libraries that execute math functions on a CPU or FPU, depending on whether an FPU is present. In other words, QuickAssist allows programmers to write code that runs without modification on processors with or without QuickAssist hardware. Intel says the QuickAssist drivers for general embedded applications and security applications will be available in September. The QuickAssist driver for Internet Protocol telephony is scheduled for release in 4Q08.

Intel's Emphasis On Security

A Swiss Army knife like the EP80579 can perform all kinds of duties, mostly in client-side systems attached to networks.

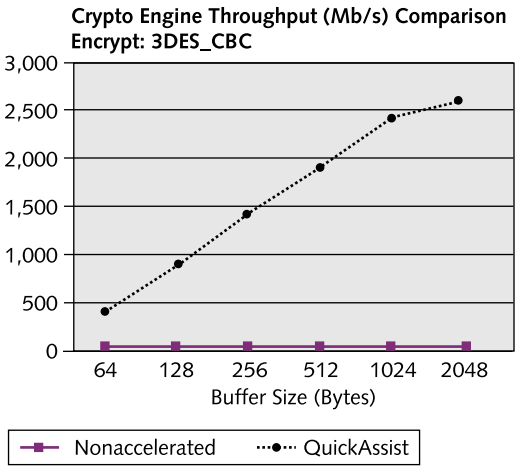

Figure 2. Low-level cryptography acceleration on the Intel EP80579 with QuickAssist. This chart measures the performance of Triple-DES Cipher Block Chaining (3DES-CBC). The flat line shows the algorithm's performance when running unaccelerated on the x86 CPU at 1.2GHz (prerelease silicon). The fast-rising line shows performance when the algorithm gets help from the EP80579's optional QuickAssist engine. Dramatic improvements like this are common when compute-intensive cryptography functions execute in optimized logic.

That Intel is working on a QuickAssist driver for Internet telephony is one clue to the company's intentions. Note, too, that EP80579 devices with QuickAssist support time-division multiplexing (TDM) over as many as 12 T1/E1-grade network connections—a potentially useful feature for voice over Internet Protocol (VoIP).

Another clue is found in Intel's marketing presentations and technical white papers, which discuss the EP80579's capabilities with regard to a unified threat-management (UTM) appliance. UTM appliances are networked systems or subsystems that combine deep-inspection packet processing with intrusion detection, malware scanning, spam filtering, and virtual private network (VPN) tunneling. Software capable of performing those tasks is available for PCs, but it runs on the CPU, relying on a general-purpose x86 processor for cryptography and other compute-intensive functions. Those functions can run much faster if the CPU hands them off to hard-wired logic or an optimized programmable engine, like the QuickAssist engine in the EP80579.

Among other things, the QuickAssist engine can accelerate Data Encryption Standard (DES) and Triple-DES (3DES) cryptography; Advanced Encryption Standard (AES) cryptography; Message Digest 5 (MD5); Rivest Cipher 4 (RC4); and multiple versions of the Secure Hash Algorithm (SHA). It also generates true random numbers, essential for public-key cryptography and other security tasks. Some of these functions are commonly used in higher-level security protocols, such as the Internet Protocol security (IPsec) standard.

Intel says that a single EP80579 chip with QuickAssist can replace a four-chip solution built with standard parts, reducing power consumption from 31W to 21W (a 34% savings) and reducing the board footprint from 32 square inches to 17 square inches (a 45% savings). But that's a straw-man argument, because the four-chip solution is an Intel Pentium M processor, an Intel 915GME north bridge, an Intel ICH6-M south bridge, and a discrete cryptography-acceleration chip attached to the south-bridge PCI interface. In reality, few engineers would build a UTM appliance that way, because integrated SoCs similar to the EP80579 are widely available from other vendors.

Boosting Performance With QuickAssist

Nevertheless, Intel's UTM example does demonstrate the dramatic performance improvement possible with an optimized SoC—whether that SoC is from Intel or another company. The graph in Figure 2 compares 3DES Cipher Block Chaining (3DES-CBC) on a prerelease EP80579 processor with and without QuickAssist acceleration. Without QuickAssist, the algorithm labors on the x86 CPU. Even at 1.2GHz, the processor can't encrypt the data fast enough to keep up with a 100Mb/s Fast Ethernet connection. With QuickAssist, the algorithm leaps to nearly 500Mb/s when operating on a small 64-byte buffer. It exceeds 2.5Gb/s when operating on a large 2KB buffer.

The comparison in Figure 2 is not necessarily a cherry-picked example. A little optimized logic goes a long way in cryptography, which is why security accelerators are a popular feature in networking and communications processors. Although Figure 2 measures the performance of a low-level cryptographic function, the high-level benefit is real, as Figure 3 shows. This graph compares the performance of a full IPsec stack running on a prerelease EP80579 processor with or without QuickAssist.

Frequent CPU interrupts generated by small packets account for the poorer throughput when handling packets smaller than 512 bytes. To remove that bottleneck, Intel plans to release software drivers that will allow the QuickAssist engine to accelerate other packet-processing tasks, not just cryptography. For now, those capabilities lie fallow.

Essentially, those future QuickAssist drivers will enable more separation between control-plane and data-plane processing on the EP80579. Packets not requiring deep inspection will bypass the x86 CPU and proceed directly to the QuickAssist engine. The engine will quickly check their headers and invoke various (programmable) policies, depending on the packet type. When deeper inspection is needed, the CPU will intervene. Intel's internal benchmarking with prerelease drivers indicates that huge improvements are possible with this "fast path" approach—improvements that will benefit large packets as well as small ones.

Competitors Enjoy a Head Start

Intel's EP80579 enters a crowded field. Similar standard parts are available from several major vendors, and the EP80579 also competes with custom ASICs that aren't sold on the open market but account for a big chunk of the networking

and communications business. (The same will be true when Intel introduces its first x86 SoCs for consumer electronics and smartphones.) Integrated SoCs with hardware acceleration for networking and communications have been available since the early 1990s, most notably from Broadcom, Motorola, and Motorola's spinoff company, Freescale Semiconductor.

For Intel, the PC heritage of the EP80579 is both an advantage and a disadvantage. The Dothan CPU core is powerful but less power efficient than an embedded-processor core should be. Future designs with Atom CPUs should fix that problem.

Integration is a larger concern. Because the EP80579 incorporates the functions of PC north-bridge and south-bridge chips, it's overburdened with PC-centric I/O controllers and interfaces. These features inflate the chip's power consumption, die size, and pin count. Someone could build a great little PC with integrated networking, security, and VoIP around the EP80579, but it's supposed to be an embedded SoC, not a PC processor or jack-of-all-trades. This wealth of features also makes the EP80579 difficult to compare with competing chips. Rival vendors have larger product lines, populated with devices that typically have fewer features but are available in greater variety, each targeting specific market segments.

One advantage of the EP80579 is that it's brand new, so it sports the very latest fashions in I/O interfaces. Most competing chips are a few years old, because embedded processors don't become obsolete as quickly as PC processors do. Consequently, the EP80579 has PCI Express, whereas some competing chips are still using PCI-X and PCI. Likewise, the EP80579 has SATA and USB 2.0, allowing easy attachment of mass storage and peripherals. The catch is that many networking chips don't need mass storage or USB peripherals, because they're simply way stations for packets. The EP80579 is hard to classify, because it has elements of a packet processor, storage processor, security processor, and telephony processor.

Rival Chips Use Less Power

For packet processing, Broadcom's BCM1280 is a powerful competitor, even though it's four years old and Broadcom hasn't refreshed this product line recently. The BCM1280 has two MIPS64-compatible processor cores, four Gigabit Ethernet controllers, two 64-bit SDRAM interfaces (configurable as four 32-bit interfaces), and three high-speed serial interfaces configurable as HyperTransport or SPI-4 pathways. The SiByte-designed processor cores can reach 1.2GHz, matching the clock speed and probably the throughput of the EP80579. On the downside, the BCM1280 lacks special hardware for cryptography acceleration, though it does accelerate some packet-processing functions. And it has even more pins than the EP80579 does, partly because it's designed to enable multiprocessor configurations. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

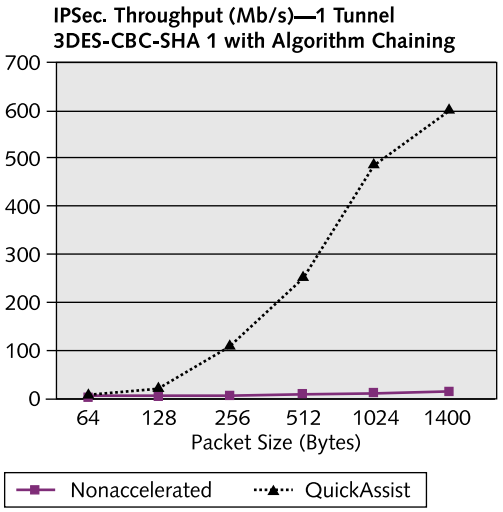

Figure 3. IPsec acceleration on the Intel EP80579 with QuickAssist. In this comparison, an open-source IPsec stack is running on a 1.2GHz EP80579 processor (prerelease silicon). Without QuickAssist, the x86 CPU struggles toward 50Mb/s, even with large 1,400-byte packets. With QuickAssist enabled, the EP80579 securely processes the packets much faster, reaching 600Mb/s with large packets.

Cavium Networks will be especially tough competition for Intel, because its rapidly expanding product line was designed from the ground up for networking and communications. There's a Cavium part for almost every purpose, and some chips have as many as 16 MIPS-compatible processor cores. Cavium has always emphasized application-specific acceleration for cryptography, data compression, decompression, pattern matching, and general packet processing. One of Cavium's newest product families is the Octeon Plus 52xx, which has been sampling since March and begins volume production in 4Q08. (For general background on Cavium's Octeon processors—not specifically the Octeon Plus 52xx—see *MPR 7/16/07-01*, "Cavium Stalks Storage," and *MPR 2/6/06-01*, "Cavium Expands Octeon Family.")

With dual or quad MIPS-compatible 64-bit processor cores, each clocked at 500MHz to 900MHz, Cavium's Octeon Plus 52xx chips should easily outrun Intel's EP80579—especially when boosted with their extensive hardware accelerators. Indeed, Cavium says that IPsec throughput on a quad-core CN5230 running at 800MHz reaches 2.1Gb/s with 64-byte packets, and 5.1Gb/s with 512-byte packets. That performance is 20 times faster than Intel's preliminary results in Figure 3, using a 1.2GHz EP80579. As new designs, Octeon Plus 52xx chips have up-to-date I/O interfaces, including multiple PCI Express and USB 2.0 controllers. Their four Gigabit Ethernet interfaces can be reconfigured as a single 10Gb/s Ethernet port. The on-chip memory controller supports DDR2 at effective speeds up to 800MHz, with ECC. The 729-contact BGA package has 359 fewer pins than Intel's SoCs, and maximum power consumption is about 35% lower.

Feature	Broadcom BCM1280	Cavium Octeon Plus CN52xx	Freescale PowerQUICC III MPC8544E	Freescale PowerQUICC III MPC8548E	Intel "Tolapai" EP80579
CPU Arch.	MIPS64	MIPS64	Power	Power	x86
CPU Core	SiByte SB-1 (2 cores)	cnMIPS64 Plus (2 to 4 cores)	e500 (1 core)	e500 (1 core)	Dothan (1 core)
Arch. Width	64 bits	64 bits	32 bits	32 bits	32 bits
Core Freq.	800MHz–1.2GHz	500–900MHz	667MHz–1.06GHz	800MHz–1.5GHz	600MHz–1.2GHz
L1 Cache (I / D)	32K / 32K	32K / 16K	32K / 32K	32K / 32K	32K / 32K
L2 Cache	1MB	512K	256K	512K	256K
Integrated Memory Controller	32/64-bit DDR/DDR2 400–800MHz ECC	32/64-bit DDR2 400–800MHz ECC	64-bit DDR/DDR2 400–533MHz ECC	64-bit DDR/DDR2 400–667MHz ECC	32/64-bit DDR2 400–800MHz ECC
PCI PCI-X	64-bit PCI 64-bit PCI-X	—	32-bit PCI 2.2	64-bit PCI-X 2 x 32-bit PCI	—
PCI Express	—	1x4, 2x2, or 2x1	2x4 and 1x1	1x8 PCIe or 1x4 PCIe and 4x Serial RapidIO	1x8, 2x4, or 2x1
Ethernet MAC	4 x GbE	4 x GbE	2 x GbE	4 x GbE	3 x GbE
USB	—	2 x USB 2.0	—	—	2 x USB 2.0
Serial ATA	—	—	—	—	2 x SATA 2.0
Ctrl-Area Net	—	—	—	—	2 x CAN 2.0b
Time-Division Multiplex I/F	—	—	—	—	Optional Up to 12 T1/E1
Crypto Accel.	—	Yes	Yes (E model)	Yes (E model)	Optional
Miscellaneous Interfaces & Features	3 x HyperTransport or SPI-4.2, SMBus, PCMCIA, UART	UART, GPIO, CRC, XOR, TCP, packet accel.	DUART, GPIO, I^2C, XOR accel.	DUART, GPIO, I^2C, XOR accel.	MDIO, SSP, UART, SMBus, IEEE-1588, LPC 1.1, SPI boot
IC Process	90nm CMOS	90nm CMOS	90nm SOI	90nm SOI	90nm CMOS
Package	1,936-ball BGA	729-ball BGA	783-ball FC-PBGA	783-ball FC-PBGA	1,088-ball FCBGA
Temp. Range (Max)	0° to +105°C	–40° to +85°C	–40° to +105°C	0° to +105°C	–40° to +85°C (600MHz & 1.066GHz)
Power Consumption*	17W (max) @ 1.0GHz	7–13W (max)	2.6–3.6W (typ) 7.15–7.5W (max)	4.6–13.6W (typ) 8.1–18.6W (max)	11W–21W (max)
Production	2005	4Q08	2007	2007	3Q08
Price (Quantity)	n/a	$43–$98 (1KU)	$68.59 (10KU)	$110 (10KU)	$40–$95 (1KU)

Table 2. Comparison of similar networking and communications processors from Broadcom, Cavium, Freescale, and Intel. This comparison is rather broad, because the Intel EP80579 is less narrowly targeted at specific market segments than are other SoCs. Better matchups are possible when the specific application is known, because Intel's competitors have larger product lines with more variety than is found in the initial eight members of the EP80579 family. (*Power consumption estimated by vendors. n/a: data not available.)

Two potential competitors from Freescale are the PowerQUICC III MPC8544 and MPC8548. Each has a Power e500 processor core with clock speeds reaching 1.06GHz and 1.5GHz, respectively. Both devices are new enough (introduced last year) to have PCI Express. The MPC8544 has two Gigabit Ethernet controllers, and the MPC8548 has four, compared with three on the EP80579. Both have special hardware for accelerating packet-processing functions and pattern matching, plus optional acceleration for cryptography—salient features of PowerQUICC chips for many years.

Both of these PowerQUICC III chips use significantly less power than the EP80579 and have about 300 fewer pins, reducing their footprints on system boards. And in 2010, near the time when Intel's Atom-based SoCs will appear, Freescale plans to ship the first of its new QorIQ communications processors. (See *MPR 7/7/08-01*, "Freescale's Multicore Makeover.")

Table 2 compares these rival chips with the Intel EP80579. This table is a mere sampling, not anything close to a comprehensive list. Depending on the specific application, many other chips from Broadcom, Cavium, and Freescale (and several additional companies) might be better alternatives.

Debating x86 Compatibility

Ultimately, our analysis of Intel's x86-based SoCs ends with the same question posed by our analysis of Intel's Atom processor: Does x86 compatibility matter in the embedded market? A great many companies can make SoCs—and they already do. But Intel is pretty much the only company that can make x86-based SoCs in this class. AMD is too wounded to offer much beyond its ancient Geode processors. The Centaur subsidiary of VIA Technologies is too small to launch a broad product line of x86 chips with high integration.

Intel's argument in favor of the x86 makes some sense for subnotebook computers ("netbooks") and the MIDs that Intel is heavily promoting. If those portable computing

platforms run desktop-class operating systems like Windows and Linux, along with some desktop-class software, then x86 compatibility saves the trouble of porting desktop-PC code to RISC architectures. Intel often cites plug-ins for web browsers as an example. However, this argument rapidly loses water when applied to networking and communications. A router or UTM appliance hardly needs to run Internet Explorer and Adobe Flash.

Indeed, the software-compatibility argument for the x86 seems inverted in the embedded world, where most application code is written for ARM, MIPS, Power, and other RISC architectures. Off the desktop and outside the server closet, the x86 has no significant advantages in operating systems, middleware, or software-development tools. Traditionally, CISC yields better code density than RISC, but most embedded RISC architectures have subsets of 16-bit instructions that are even more compact than the x86's variable-length instructions.

Intel could have gained a slight advantage by stripping down the x86 architecture for the embedded market, much as Motorola streamlined the 68K to make ColdFire. Instead, Intel chose to maintain full x86 compatibility, without compromises. As a result, Intel's x86 cores will struggle to match the small size and low power consumption of their RISC rivals.

Another factor is that almost all RISC architectures are licensable, whereas the x86 emphatically is not. As long as this imbalance persists, Intel will always be one company competing against hundreds of RISC licensees, which will strain even Intel's vast resources. Without licensable processor cores, the x86 will make no inroads into the custom ASICs and FPGAs that are so vital to embedded developers. The unlicensable x86 gives customers no control over custom integration, production volume, pricing, or long-term availability. When Intel discontinues a part, some customers will be stranded, because there are no alternative suppliers for x86 SoCs.

All things considered, the x86 is entering the SoC market without compelling architectural advantages and with some handicaps. Its biggest potential advantage is technological, not architectural. If Intel assigns high priority to its SoC business, the company's world-class fabrication technology should bless these chips with the smallest, fastest transistors on the smallest, most efficient dies, economically manufactured in high volumes. Intel's competitors are either fabless or rely on alliances for manufacturing, and they will probably trail Intel's technology progress by a year or more.

Of course, superior fabrication technology didn't make Intel's XScale processors successful. However, we suspect that Intel was half-hearted about the not-invented-here ARM architecture. With the x86 in play, Intel has much more at stake. As more personal computing moves off the desktop and onto mobile platforms, Intel must establish the x86 as a viable architecture in that fast-growing market. Otherwise, the x86 will be relegated to immobile computers, which are looking more and more like yesterday's news.

Price & Availability

All eight of Intel's EP80579 SoCs are scheduled for volume production this quarter (3Q08). For parts without QuickAssist technology, 1,000-unit prices range from $40 to $65 (600MHz to 1.2GHz). For parts with QuickAssist, 1,000-unit prices range from $54 to $95 (600MHz to 1.2GHz). Intel plans to ship the first QuickAssist software drivers in September, followed by additional drivers in 4Q08 and 2009. For more information about Intel's EP80579, visit *www.intel.com/design/intarch/ep80579*.

- For more information about Broadcom's BCM1280: *www.broadcom.com/products/Enterprise-Networking/Communications-Processors/BCM1280*
- For more information about Cavium's Octeon Plus 52xx processors: *www.caviumnetworks.com/OCTEON-Plus_CN52XX.html*
- For more information about Freescale's PowerQUICC III: *www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=02VS0lDFTQJk19*