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READYIP BOOSTS FPGAS

Synplicity Tools Offer Packaged Soft-IP for FPGA Development

By Tom R. Halfhill {6/16/08-01}

Chip designs aren't carved in stone. It's worse—they're carved in silicon. And the engineers wielding the chisels might labor for years on a brilliant design that fails miserably after its first pass from the fab. A few costly re-spins later, the revised silicon may actually work, may hit the original performance targets, and may still be competitive in the market. Or maybe not.

For several years now, *Microprocessor Report* has covered the trend toward implementing and deploying SoC designs in the programmable logic of FPGAs instead of in the fixed logic of ASICs. In the past, programmable-logic devices were commonly viewed as prototype platforms, not as final products. Multiple factors are driving the trend toward programmable logic: the rising costs of fabricating ASICs, the falling prices of FPGAs, the growing capacities of programmable-logic fabrics, the need to meet shorter time-to-market deadlines, and the rapid obsolescence of electronic products.

A major obstacle has been the limited variety of synthesizable intellectual property (soft IP) licensed for commercial deployment in FPGAs. Although ASIC designers can choose from dozens of licensable embedded-processor cores, FPGA developers have only a few processors available to them. Furthermore, some processor-IP vendors restrict their cores to devices from only one FPGA vendor. Peripheral IP for FPGAs is a little less limited but still isn't as abundant as the peripheral IP available for ASIC designs.

One reason for this obstacle is that producing an SoC in programmable logic is economical only for lower-volume or higher-priced embedded systems, so the market isn't compelling enough for some soft-IP vendors—yet. Things are slowly changing in favor of FPGAs. Another reason is that soft-IP vendors fear losing control of their valuable property when it's distributed in programmable logic. Theft is a serious threat to companies earning their livelihoods by licensing soft IP.

FPGA developers received a big boost in April when Synplicity unveiled its ReadyIP initiative. Synplicity is an FPGA development-tool vendor recently acquired by Synopsys, and ReadyIP could open the floodgates. It allows soft-IP vendors to package their cores in a standardized format, so FPGA developers can easily integrate the IP using system-level design tools. The Synplicity tools work with existing FPGA tools to generate the final layout. Optionally, soft-IP vendors can protect their ReadyIP cores with encryption that still lets developers evaluate a design before purchasing a full license. And ReadyIP isn't specific to any particular brand of FPGAs, so it works with devices from market leaders Altera and Xilinx, as well as with devices from smaller vendors like Actel and Lattice Semiconductor.

Tensilica Takes the Plunge

So enticing is ReadyIP that Tensilica is offering its first processor core for FPGA deployment. Tensilica's Diamond Standard 106Micro 32-bit processor, introduced last year for conventional ASIC design flows, is now sanctioned for FPGAs—and it's free. Licensing the processor costs nothing for volumes under 10,000 units.

ARM—by far the leading processor-IP vendor—is throwing its crucial support behind ReadyIP, too. ARM is offering its Cortex-M1, the company's first processor core designed and optimized for FPGAs. (See *MPR 3/19/07-01*, "ARM Blesses FPGAs.")

Another ReadyIP affiliate is CAST, which is making several peripheral cores (but not processors) available through

the ReadyIP program. CAST peripherals include an AMBA system library, PCI Express endpoint controllers, High-Speed USB controllers, a 10–100Mb/s Ethernet controller, various memory controllers, and accelerators for JPEG image compression and decompression.

For additional soft IP, developers can turn to Gaisler Research, which licenses the SPARC V8-compatible LEON3 processor core and related peripheral IP in the extensive GRLIB library. Source code for GRLIB peripherals is available under a GNU General Public License. The IP includes AMBA bus controllers, memory controllers, DMA controllers, a programmable UART, and a 10–100Mb/s Ethernet controller. All the cores from CAST and Gaisler are silicon-proven components that have been available for years and are now sanctioned for FPGA development under the ReadyIP program.

More is coming. In addition to recruiting other third-party vendors, Synopsys says it may adapt the soft IP in its vast DesignWare library to work with ReadyIP. Such a move could provide the extra push needed to make ReadyIP virtually an industry standard for implementing SoCs in programmable logic. All told, ReadyIP is the best news for FPGA developers in years.

Optional Encryption Protects IP

Soft-IP vendors needn't modify their processors or peripheral cores for the ReadyIP program, but they must add some metadata that describes the high-level I/O interfaces to system-level design tools. The metadata format is IP-XACT, an open XML-based format promoted by the Spirit Consortium. IP-XACT isn't specific to ReadyIP—Synplicity merely adopted it as a convenient metadata format that's already gaining industry support.

IP-XACT can describe soft IP written in various hardware-design languages, including Verilog, VHDL, SystemC, and SystemVerilog. It can also describe software components written in C and C++. If an IP vendor hasn't already defined the metadata for a particular core or component, developers can do it themselves, using widely available tools. In addition, developers can use these tools to define the metadata for soft IP developed internally.

By itself, IP-XACT provides no encryption to protect IP from theft. Some soft-IP vendors don't care. For instance, Gaisler Research provides the LEON3 processor core and the GRLIB peripheral IP as unencrypted VHDL or Verilog source code. (A few blocks—such as LEON3's optional FPU—are supplied as unencrypted VHDL or Verilog netlists.) Developers can download the cores, synthesize the source code, implement the design in an FPGA, and test the design under actual conditions. The LEON3 is verified to work with Synplicity's synthesis tools and with the Synplicity High-Performance ASIC Prototyping System (HAPS).

Other soft-IP vendors are protecting their cores in various ways. A strength of the ReadyIP program is that it allows IP vendors to choose any degree of protection they want. For example, Tensilica encrypts the Diamond 106Micro processor core but not some ancillary components, such as an AHB-Lite bus bridge, a tap controller, local memories, and the top-level interconnect. Developers can synthesize the 106Micro with these components, test the design in an FPGA, and deploy the design in the same device.

ARM is a little more cautious. ARM encrypts the Cortex-M1 processor as Tensilica does and permits logic synthesis for evaluation purposes, but the design tools disclose the timing information only. To test the Cortex-M1 under actual conditions, developers must purchase a license from ARM at regular prices.

Depending on the performance requirements of a design, the differences among these various levels of protection may or may not matter. Obviously, developers can evaluate a timing-critical design more thoroughly by using IP that's fully implemented in a device. Otherwise, developers must rely on the performance estimates of the design tools for evaluation before purchasing a license.

The Synplicity ReadyIP tools use an encryption scheme known as OpenIP. In 2005, Cadence Design Systems donated an encryption scheme to the IEEE, which adopted it as the IEEE 1364-2005 specification. In 2006, Synplicity (before its acquisition by Synopsys) launched the OpenIP initiative, which proposed a nonproprietary scheme for soft-IP encryption and digital-rights management. OpenIP is based on both technologies. An IEEE working group (IEEE P1735) is refining this specification. It's an open spec that conforms with U.S. government export controls and is largely transparent to SoC developers using the encrypted IP. The encryption scheme is flexible, so soft-IP vendors can choose which information about their cores to protect or expose.

ReadyIP Tools for System-Level Design

For now, to use ReadyIP, developers must buy Synplicity design tools—either Synplify Pro or Synplify Premier. The Pro version can synthesize netlists and costs $22,000 to $50,000, depending on the terms of the particular license. The Premier version can synthesize netlists and generate optimized placements for specific types of FPGAs. It costs $49,000 to $75,000, depending on the license.

Neither tool replaces the FPGA vendor's proprietary tools for generating the final physical layout. With Synplify Pro, the FPGA vendor's tools do the final place and route. With Synplify Premier, the FPGA vendor's tools do the routing only. The Synplify tools are based on the same Synplicity FPGA-synthesis tools already used by thousands of developers.

In their ReadyIP incarnations, both Synplify Pro and Synplify Premier have an IP browser that lists all the soft IP available through the ReadyIP program. Developers can read documentation about the IP, decide what they want, and download evaluation versions (or, in some cases, fully capable versions) of the cores.

Another tool included with Synplify Pro and Synplify Premier is the ReadyIP System Designer. It's an Eclipse-based

environment that lets developers create an SoC by integrating all the soft IP they have obtained. System Designer connects the I/O interfaces of the cores and generates the RTL files needed for logic synthesis. Figure 1 illustrates the ReadyIP design flow.

IP-XACT metadata is strictly for the convenience of developers and system-level design tools. The underlying RTL or software code is unmodified, so it performs normally when implemented in an FPGA. Encrypted soft-IP is automatically decrypted before final physical placement in the FPGA fabric, so it performs normally, too. There is no difference in performance when using soft IP obtained through the ReadyIP program instead of the same IP obtained in the usual ways.

Because the IP-XACT metadata format and the OpenIP encryption scheme are open specifications, other vendors can create design tools that compete with Synplicity's tools. For instance, a competitor could offer a different System Designer for IP integration. In fact, similar tools for integrating IP-XACT files already exist. And because the Synplicity System Designer is based on Eclipse, it's open for extension. Likewise, Synplify Pro and Synplify Premier are potentially interchangeable parts in the ReadyIP design flow. Therefore, ReadyIP could become an industrywide vendor-independent standard for designing FPGA-based SoCs.

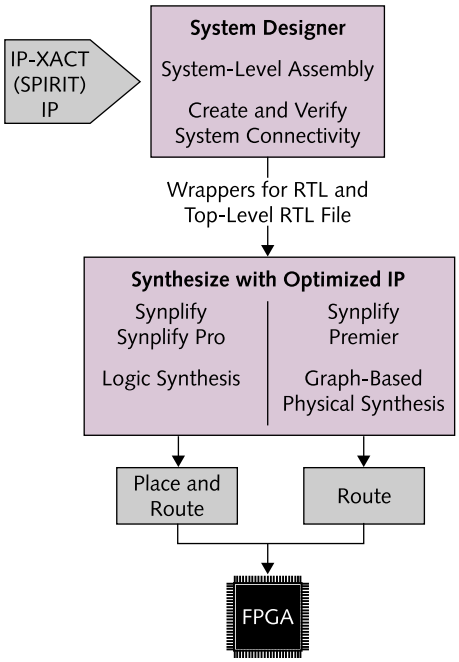

Figure 1. ReadyIP design flow. To create SoCs with ReadyIP, developers use special Synplicity design tools—either Synplify Pro or Synplify Premier—plus System Designer, an Eclipse-based IP-integration environment. All soft-IP interfaces must be described by the IP-XACT open metadata format. System Designer can integrate free IP, commercial IP, and in-house proprietary IP.

Growing Demand for CPUs in FPGAs

Before launching ReadyIP, Synplicity conducted an anonymous survey of developers and gathered some interesting data. The survey found growing demand for processor cores in FPGAs, confirming the anecdotal evidence. More than 40% of FPGA projects are using some kind of processor core—although that figure includes projects using FPGAs for prototyping only, not for deployment.

According to the Synplicity survey, the most popular processors in FPGAs are based on the Power Architecture. This result is surprising at first glance, because the Power processor cores from Freescale Semiconductor and IBM normally aren't licensed for commercial distribution in FPGAs. Since 2000, however, Xilinx has been selling some high-end FPGAs with integrated PowerPC 405 hard cores, which run much faster than soft cores synthesized in a programmable-logic fabric. The popularity of these devices among the developers that Synplicity surveyed may reflect Synplicity's high-end user base.

Market leader ARM might be expected to have a big presence in FPGAs, but ARM didn't begin licensing a synthesizable processor for FPGA deployment (the aforementioned Cortex-M1) until last year. Also, the Cortex-M1 doesn't support the 32-bit ARM instruction-set architecture, which may deter some developers. Although the Cortex-M1 is upwardly compatible with that architecture, it runs only the subsets of 16-bit ARM Thumb and Thumb-2 instructions. That feature is great for code density but less desirable for developers that already have 32-bit ARM code.

Not surprisingly, two other popular CPU architectures in FPGAs are MicroBlaze (from Xilinx) and Nios (from Altera). MicroBlaze is an FPGA-only 32-bit processor. (See *MPR 11/13/07-01*, "MicroBlaze v7 Gets an MMU.") Nios is a 32-bit competitor intended primarily for FPGAs, but developers can also use it with structured ASICs and standard-cell ASICs. (See *MPR 12/17/07-02*, "Altera Aims for ASICs.") In a report published last year, market researchers at Gartner found that the Nios II is the industry's favorite synthesizable 32-bit processor in recent design starts. Altera has shipped more than 20,000 Nios II development kits to more than 5,000 customers.

Tensilica is the newcomer to this game. After standing on the sidelines for years, Tensilica has decided that ReadyIP is the right vehicle for bringing the configurable Xtensa CPU architecture to FPGAs. Until now, Tensilica allowed developers to use FPGAs for prototyping, but typically not for deployment. (ARC International and MIPS Technologies are similarly wary of FPGAs.) Even so, at this time, Tensilica is offering only the preconfigured Diamond Standard 106Micro processor through the ReadyIP program. It is Tensilica's smallest core, intended mainly for microcontroller applications.

Developers can implement and distribute the 106Micro in as many as 10,000 FPGAs without paying an up-front licensing fee or chip royalties. For many applications that substitute an FPGA for an ASIC, 10,000 units is a

Feature	Altera Nios II/f v8.0	ARM Cortex-M1	Freescale ColdFire-V1	Gaisler LEON3	Tensilica 106Micro	Xilinx MicroBlaze v7
Architecture	Nios II	ARMv6-M	ColdFire-V1	SPARC V8	Xtensa LX	MicroBlaze
Primary FPGA Targets	Cyclone, Stratix	Any FPGA (Optimized for Actel, Altera, Xilinx)	Cyclone III or any FPGA	Any FPGA	Any FPGA	Virtex-5 Spartan-3
Structured ASIC	HardCopy II	HardCopy II	Any process	Any process	Any process	—
Standard-Cell ASIC	Any process	Cortex-M3 compatible	Any process	Any process	Any process	—
Configurable ISA	Yes	—	—	—	Yes	—
Pipeline Depth	6 stages	3 stages	4 stages	7 stages	5 stages	5 stages
I-Cache	0–64K	—	—	0–1MB	—	0–64K
D-Cache	0–64K	—	—	0–1MB	—	0–64K
Local Memory	0–4 0.5K–64K	0 or 2 1K–1024K	—	0 or 2 Configurable	2 (I + D) Configurable	0 or 2 256K
32-Bit Multiplier	Optional	Two options	Yes	Yes	Yes	Optional
32-Bit Divider	Optional	—	Optional	Yes	—	Optional
Barrel Shifter	Optional	Yes	Yes	Yes	Yes	Optional
FPU	Optional 32 bits	—	—	Optional 32 / 64 bits	—	Optional 32 bits
Branch Predict	Dynamic	—	Static	—	—	—
Privilege Levels	2	1	2	2	1	1 or 2
Coprocessor Interface	Avalon	AMBA-3 AHB-Lite	—	AMBA 2.0 AHB	—	FSL
On-Chip Interconnect	Avalon	AMBA-3 AHB-Lite	AHB-Lite or Avalon	AMBA 2.0 AHB	Xtensa PIF (AMBA bridges)	CoreConnect PLB v4.6
Memory Management	Optional MPU or MMU	—	—	Optional MMU	MPU	Optional MMU or MPU
Translation Lookaside Buffer (TLB)	—	—	—	Configurable	—	Optional 8-entry I + D 64-entry unified
FPGA Core Freq (Max)	265MHz*	>200MHz	80MHz†	Up to 140MHz	n/a	220MHz
FPGA Integer Performance (Max)	300 Dmips*	0.8 Dmips per MHz	1.05 Dmips per MHz	1.0 Dmips per MHz	n/a	240 Dmips
FPGA FP Performance (Max)	n/a	—	n/a	1.0 Mflops / MHz	—	50 Mflops
FPGA Logic Cells	1,100 ALUTs*	1,800 (Base config)	5,000–6,000	~3,500** (Base config)	n/a	960–1,700
ASIC Core Freq (Max)	n/a	—	150MHz (130nm)	400MHz (130nm)	1.22Dmips / MHz (400MHz 90nm)	—
Introduction	2004 Upgrade 2Q08	4Q07	3Q08	2004	2007	2001 Upgrade 4Q07
FPGA Price	$495	<$100,000 (ARM) Free (Actel)	Free‡	€20,000 with GRLIB	<10K units: free >10K units: $1/chip	$495

Table 1. Comparison of 32-bit synthesizable processors approved by their vendors for deployment in FPGAs. This table keeps growing, as more vendors are willing to license their cores for commercial distribution in FPGAs and not just for prototyping ASIC designs. Freescale's ColdFire-V1 and Tensilica's Diamond 106Micro are the latest additions. ARC International and MIPS Technologies are still avoiding this market for now. *Nios II performance when synthesized in an Altera Stratix III FPGA. †ColdFire-V1 clock-speed target is 100MHz by the time of introduction. **Gaisler's estimate for a LEON3 synthesized in an Altera Stratix II or Xilinx Virtex-4 FPGA. ‡The ColdFire-V1 is license- and royalty-free when implemented in an Altera Cyclone III device; for other FPGAs and ASIC designs, the licensing fee is $10,000 plus royalties. (n/a: data not available.)

generous ceiling. Beyond 10,000 units, developers will owe Tensilica $1 per chip. That's a princely royalty—much higher than Tensilica usually charges for its processors. But embedded systems based on FPGAs tend to be higher-priced specialty items, not mass-market consumer products, so $1 per chip shouldn't be a significant cost. The only additional cost is for Tensilica's development tools, which include a C/C++ compiler, linker, assembler, debugger, instruction-set simulator, and performance-profiling tools. Developers can evaluate the tools for free, and licenses cost $1,000 per seat per year.

Differences Among CPUs for FPGAs

Table 1 lists the 32-bit synthesizable processor cores sanctioned for commercial distribution in programmable-logic devices. A similar table appeared in our previously cited December 2007 article about the Nios II, but this one adds Tensilica's Diamond Standard 106Micro processor and Freescale Semiconductor's ColdFire-V1 processor. Tensilica entered this market segment on April 2 and Freescale joined the party on June 9. Although Freescale hasn't joined the Synplicity ReadyIP program, Freescale's debut in this market segment is notable for two reasons: it brings a processor

Freescale Offers ColdFire-V1 for FPGAs

Freescale Semiconductor has joined the growing list of companies allowing their processor cores to be commercially distributed in FPGAs. Freescale's ColdFire-V1—a synthesizable 32-bit embedded processor derived from the Motorola 68K architecture—is now sanctioned for use with Altera's Cyclone III and other programmable-logic devices. Freescale and Altera announced the news on June 9.

Although Freescale isn't participating in the Synplicity ReadyIP program, the release of the ColdFire-V1 for FPGA distribution is another sign that processor-IP vendors are responding to design challenges facing developers. Until now, Freescale licensed the ColdFire-V1 for ASIC projects only. (See *MPR 8/28/06-02*, "Connecting the Continuum.")

Better yet, Freescale is licensing the Cyclone III variant of the ColdFire-V1 for free. There are no up-front licensing fees and no royalties, no matter what the volume. Multicore projects are free, too, and the processor includes Freescale's single-wire debug module. To implement and deploy the ColdFire-V1 in other FPGAs (or in ASICs), the licensing fee is $10,000, plus chip royalties.

The ColdFire-V1 becomes the only free commercial processor approved for deployment in FPGAs. ARM's Cortex-M1 is license- and royalty-free when preintegrated in some Actel FPGAs, but, obviously, some pass-through cost is built into the chips. Tensilica is freely licensing its Diamond Standard 106Micro processor for FPGAs, but volumes exceeding 10,000 units incur a $1 per chip royalty. The open-source LEON3 processor from Gaisler Research is free to educational users, but commercial developers must buy a €20,000 license for an FPGA project. Even the low-ball Altera Nios II and Xilinx MicroBlaze processors cost $495.

What's the catch with the ColdFire-V1? Tech support. Freescale provides free support, but only for matters relating directly to the processor, such as questions about the instruction-set architecture. Altera provides the usual tech support with its FPGA design tools, such as SOPC Builder and Quartus II. But for help with implementation problems, developers must purchase tech support from IPextreme, the independent company to which Freescale outsources all its IP licensing. IPextreme licenses the full line of ColdFire-V1 cores and has the technical expertise to package and support the cores. IPextreme has a website called the Core Store from which developers can obtain the ColdFire-V1 (as well as additional soft IP) and buy 10-hour tech-support packages for $2,500. (See *MPR 2/11/08-01*, "Buy SoC IP Like MP3s.")

Another catch is that the free version of the ColdFire-V1 is for Altera's Cyclone III only. Not that there's anything wrong with Cyclone III—it is Altera's lowest-priced, lowest-power line of FPGAs. Cyclone III devices are the only low-cost FPGAs currently fabricated at 65nm. But for now, the free version of the ColdFire-V1 isn't compatible with Altera's higher-performance Stratix line or with FPGAs from other vendors. For $10,000, the Core Store sells another variation of the ColdFire-V1 that's compatible with virtually any FPGA and with ASIC design flows.

Despite their smaller capacities, most Cyclone III devices have plenty of room for the ColdFire-V1. Freescale estimates the processor will occupy 5,000 to 6,000 logic elements in the programmable-logic fabric. Cyclone III devices have 5,000 to 120,000 logic elements, so all but the smallest chips will be suitable. Altera says the processor will fit easily into a Cyclone III costing less than $5, with room to spare for some peripheral IP. Cyclone III devices are available with up to 4Mb of on-chip memory and as many as 288 dedicated DSP multipliers.

Freescale is aiming for a maximum clock speed of 100MHz when the Cyclone III version of the ColdFire-V1 hits the market in 3Q08. At this time, however, a more realistic clock frequency is 65–80MHz. Unlike Altera's Nios II, ARM's Cortex-M1, and Xilinx's MicroBlaze, the ColdFire-V1 wasn't originally designed with FPGA fabrics in mind.

The ColdFire-V1 will work with Altera's SOPC Builder, a system-level design tool for integrating soft IP in SoC designs. SOPC Builder is a more established tool than Synplicity's new ReadyIP System Designer. In addition to working with the ColdFire-V1, SOPC Builder is compatible with Altera's Nios II, ARM's Cortex-M1, and more than 50 peripheral-IP blocks that are optimized for FPGAs and are royalty free.

Just because Freescale is offering the ColdFire-V1 for free doesn't mean the company isn't worried about IP theft. Developers will receive the processor as an encrypted netlist presynthesized for SOPC Builder, and it won't be available in China. The rest of the world can begin using the ColdFire-V1 in FPGAs in 3Q08.

based on the Motorola 68K (68000) architecture to FPGAs, and the ColdFire-V1 is free when implemented in Altera Cyclone III devices. (See the sidebar, "Freescale Offers ColdFire-V1 for FPGAs.")

Note that the ARM Cortex-M1, Gaisler Research LEON3, and Tensilica Diamond 106Micro are the only processor cores currently available through the Synplicity ReadyIP program. They work with FPGAs from Actel, Altera, Lattice, and Xilinx. MicroBlaze is compatible only with Xilinx devices, and the Nios II is compatible only with Altera devices. The ColdFire-V1 can work in any FPGA, but only the Cyclone III version is free and is tuned for better performance in a specific programmable-logic fabric. Other versions of the ColdFire-V1 cost $10,000 to license, plus chip royalties.

Only the ARM Cortex-M1 and Gaisler LEON3 are optimized for better performance in programmable-logic

Price & Availability

ReadyIP design tools and soft-IP cores are available now. Synplicity, a recently acquired business unit of Synopsys, sells two versions of its ReadyIP design-automation tools: Synplify Pro and Synplify Premier. Depending on licensing terms, Synplify Pro costs $22,000 to $50,000, and Synplify Premier costs $49,000 to $75,000. Both versions include the ReadyIP System Designer, a system-level tool for integrating soft IP. These tools can target FPGAs from Actel, Altera, Lattice, and Xilinx.

Several soft-IP cores are available through the ReadyIP program, and more are coming. Initial 32-bit processor cores are the ARM Cortex-M1, Gaisler Research LEON3, and Tensilica Diamond Standard 106Micro. An ARM Cortex-M1 RTL license costs less than $100,000 for Actel, Altera, or Xilinx FPGAs. The Cortex-M1 is free with some Actel devices. The Gaisler LEON3 processor is free to educational users; for commercial FPGA projects, a license costs €20,000, which includes the GRLIB peripheral-IP library. Tensilica's Diamond 106Micro processor is free for FPGA deployments under 10,000 units and costs $1 per chip thereafter. Tensilica's development tools cost $1,000 per seat per year. CAST sells numerous peripheral-IP cores at various prices. All soft IP offered through the ReadyIP program is available for free evaluation.

Outside the ReadyIP program, Freescale Semiconductor will offer multiple versions of the ColdFire-V1 processor through the IPextreme Core Store. There are no up-front fees or royalties when licensing the ColdFire-V1 for Altera Cyclone III devices. For other FPGAs and ASICs, the ColdFire-V1 license is $10,000 plus chip royalties. Freescale says the Cyclone III version of the ColdFire-V1 will be ready in 3Q08.

For more information:

- ReadyIP: *www.synplicity.com/partners/readyip*
- Altera: *www.altera.com/corporate/news_room/releases/products/nr-sopc_builder.html*
- ARM: *www.arm.com/products/CPUs/ARM_CortexM1.html*
- CAST: *www.cast-inc.com/synplicity*
- Gaisler Research: *www.gaisler.com/leonmain.html*
- Tensilica: *www.tensilica.com/diamond/di_106micro.htm*
- Freescale Semiconductor: *www.freescale.com/files/pr/coldfirelicensing.html*
- IPextreme: *www.ip-extreme.com/corestore*

fabrics from multiple FPGA vendors. Fabrics vary in structure from one vendor to another, and those variables affect both the size and speed of a synthesized processor core. ARM offers slightly different synthesizable models of the Cortex-M1 for the FPGAs from Actel, Altera, and Xilinx. A synthesis option for Gaisler's LEON3 processor lets developers optimize the core for either standard-cell or programmable-logic implementations. When targeting FPGAs, the LEON3 uses modified I/O pads, memory cells, clock generators, pipeline stages, register files, multipliers, adders, and other structures. The LEON3 is configurable, and developers can even tinker with the open VDHL source code if they wish. For educational users, the LEON3 processor and GRLIB peripherals are free. Commercial users pay €20,000 for an FPGA implementation. In either case, LEON3 software-development tools are free.

Tensilica hasn't optimized its processor core for programmable logic. At this point, Tensilica is testing the FPGA waters, so it doesn't make sense to rework the processor for specific fabrics. MicroBlaze is optimized for Xilinx fabrics, and Nios II is optimized for Altera fabrics, but Xilinx and Altera forbid developers to use their processors in FPGAs from other vendors. Freescale is making minor modifications to the ColdFire-V1 to improve performance in Cyclone III devices, but it's not a major overhaul. Freescale is reluctant to invest too much effort in a giveaway product and worries that extensive modifications could affect the processor's software compatibility with the 68K-derived instruction-set architecture.

As more SoC developers turn to FPGAs as an alternative to ASICs, *MPR* expects more CPU vendors to relax their licensing restrictions and optimize their cores for programmable logic. Custom chips are becoming economical only for the highest-volume products, and the volume crossover point at which FPGAs are more economical gets lower every year. If Synplicity's ReadyIP program succeeds in standardizing the packaging, protection, and integration of soft IP for FPGAs, it will accelerate a trend that already seems inexorable. ◇