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TRANSMETA'S SECOND LIFE

$250 Million Patent Windfall From Intel Creates Opportunities

By Tom R. Halfhill {12/26/07-01}

Once given up for dead, Transmeta is getting a second chance. Thanks to a $250 million settlement from Intel in a patent-infringement lawsuit, Transmeta is looking forward to a new future as an intellectual-property (IP) provider. But the company says it has no plans to resume making microprocessors.

In October, industry watchers were surprised when Intel settled a patent lawsuit that Transmeta had filed only a year before. Usually, patent squabbles take years to resolve, even when settled out of court. Transmeta had sued Intel in U.S. District Court in October 2006, alleging that Intel had infringed ten of Transmeta's microprocessor-related patents. (Later, Transmeta amended its complaint to name an eleventh patent.) Within weeks, Intel fired back with a countersuit, alleging that Transmeta had infringed seven of Intel's patents. The case began to resemble an epic AMD-Intel feud that might drag on for a decade.

Instead, one year after Transmeta's opening barrage, Intel settled. Intel agreed to pay Transmeta $150 million within 90 days of the agreement plus $20 million a year for five years afterward—$250 million in all. In addition, Intel received a license for the patents and gave Transmeta a covenant-not-to-sue for Transmeta's low-power technology-licensing business.

However, the fight hasn't entirely ended. Before the settlement, Intel had asked the U.S. Patent and Trademark Office to reexamine Transmeta's patents. The reexamination—which may take years—is continuing, despite the settlement. If the reexamination invalidates some or all of Transmeta's patent claims, there may yet be another surprise in this saga.

Meanwhile, the $250 million windfall is nothing less than a second lease on life for Transmeta. Shriveled by layoffs and forced to kill its innovative Crusoe and Efficeon microprocessors, Transmeta was looking doomed. The 12-year-old company has dwindled to about 40 people, including contractors. Even the business functions have been outsourced, leaving a small group of (mostly hardware) engineers to work on power-saving technologies suitable for licensing to other parties. During its heyday in the early 2000s, Transmeta employed hundreds of people and seriously challenged Intel with low-power x86-compatible processors. (See *MPR 1/24/2000-05*, "Transmeta Unveils Crusoe," and *MPR 2/14/00-01*, "Transmeta Breaks x86 Low-Power Barrier.")

Now, suddenly, Transmeta is flush with cash. The company is essentially debt-free and has a guaranteed five-year revenue stream of $20 million a year from the settlement alone. The big question is what Transmeta will do with the money. To find out, *Microprocessor Report* interviewed John Heinlein, vice president of business development and marketing. Heinlein, who joined Transmeta in June 1997, isn't just a talking suit. He has a B.S. in computer engineering from Carnegie Mellon University and a Ph.D. and M.S. in electrical engineering from Stanford University. He has held several positions at Transmeta, including engineering positions, and knows the company's technology.

In addition, *MPR* has reviewed the eleven patents named in Transmeta's lawsuit. Although Transmeta says it doesn't plan to use the patents offensively, clearly they are valuable property. If nothing else, they will be useful defensively in the years to come—assuming they survive the reexaminations.

(Full disclosure: The inventor named on four of the eleven patents in Transmeta's lawsuit is Rich Belgard, an *MPR* contributing editor who writes our "Patent Watch" feature. Belgard is also a longtime member of the *MPR* editorial board. Transmeta acquired these four patents from Belgard in 2001. Belgard reviewed this article but did not otherwise contribute to it.)

Plan A: Beat Intel

At least five years ago, Transmeta realized that competing with Intel for x86-compatible microprocessors was tougher than anticipated. Stung by Transmeta's bold challenge, Intel struck back with a low-power x86 core of its own, quietly developed by a then-obscure Intel engineering group in Israel. Code-named Banias, later dubbed Pentium M, Intel's new microarchitecture was a sharp departure from the hyperpipelined, high-clock-speed NetBurst microarchitecture in the Pentium 4. In notebook computers, Banias negated the advantages of Transmeta's low-power Crusoe processors. In desktop computers and servers, Banias was more suitable for the new wave of multicore x86 designs. (See *MPR 11/25/02-01*, "Intel Spills the Beans About Banias.")

Transmeta began exploring other options. One response was the Crusoe SE (Special Embedded) family, intended for embedded systems needing x86 compatibility. (See *MPR 1/13/03-01*, "Transmeta Charges the Embedded Market.") Within months, Intel began pushing Pentium M in the same direction. (See *MPR 5/12/03-01*, "Intel's Pentium M Gets Embedded.") As *MPR* noted when Transmeta first unveiled Crusoe in 1999, Intel regards the x86 as home turf and doesn't gladly suffer interlopers. And Intel has much greater engineering resources, not to mention marketing muscle and long-established business relationships.

Undeterred, Transmeta forged ahead with a new family of low-power x86-compatible processors named Efficeon. (See *MPR 10/27/03-01*, "Transmeta Gets More Efficeon.") Transmeta hoped its second-generation design would regain an advantage over Intel's low-power x86 chips. Plans called for Efficeon to carry Transmeta all the way to the 65nm process node. (See *MPR 10/18/04-01*, "Transmeta Extends Efficeon Roadmap.")

Unfortunately for Transmeta, Efficeon stalled in the market. Despite some early successes with Crusoe, Transmeta couldn't win enough designs to reach the production volumes required to sustain a company trying to compete with an industry giant. Meanwhile, spurred by AMD's competition as well as by Transmeta's, a reinvigorated Intel fought back even harder. Earlier this year, Intel announced its improved Core 2 microarchitecture, which surpasses the power/performance efficiency of Pentium M. (See *MPR 4/30/07-01*, "Intel Goes on the Offensive.") By that time, battered by layoffs and cutbacks, Transmeta realized it needed a new strategy.

Plan B: License LongRun2

Two good things survived Transmeta's travails with Intel: Long Run and LongRun2. LongRun is Transmeta's original technology for dynamically adjusting a microprocessor's voltage and clock frequency to reduce power consumption. Instead of blindly running at full speed all the time, the processor can respond to different software workloads by throttling back to a lower clock rate and voltage. Power savings can be dramatic. Today, many processors use similar techniques.

LongRun2 improves on LongRun by implementing lower-level power management. Whereas LongRun can vary only the processor's clock frequency and core voltage in relatively large steps, LongRun2 can vary the threshold voltage (Vt) of the transistors themselves. At lower threshold voltages, transistors switch more quickly but leak more current. Conversely, at higher threshold voltages, transistors leak less current but switch more slowly.

Chip designers can choose to apply LongRun2 statically or dynamically. Static adjustments are easier, but dynamic adjustments are more flexible, because they can alter the threshold voltages at run time in response to changing conditions. If desired, LongRun2 can adjust the threshold voltage hundreds of times per second. A key advantage of LongRun2 is that it works with most existing processor designs, circuit layouts, cell libraries, and CMOS fabrication processes. Transmeta introduced LongRun2 in Efficeon processors in 2003. (See *MPR 10/27/03-01*, "Transmeta Gets More Efficeon.")

In 2005, Transmeta began making the transition from a fabless semiconductor company to an IP-licensing company. (See *MPR 5/2/05-01*, "The Transformation of Transmeta.") Today, LongRun2 remains Transmeta's most valuable licensable IP. In 2005 and 2006, Transmeta licensed LongRun2 to Fujitsu, NEC Electronics, Sony, and Toshiba. Transmeta is actively seeking additional licensees.

Transmeta's John Heinlein told *MPR* that LongRun2 is the foundation of a licensable-IP portfolio that the revived company hopes to build upon, using the settlement money from Intel. Transmeta's first goal is to make LongRun2 easier to license and use. (Originally, LongRun2 was developed only for Transmeta's own processors.) Heinlein expects demand to rise as chip developers move to smaller fabrication processes, because current leakage is becoming a larger problem.

Another application of LongRun2 is managing the variations in leakage among different dies manufactured on the same wafer line. Whether chip designers apply LongRun2 statically or dynamically, either locally or throughout the chip, it can compensate for leakage variations in ways that other techniques (including the original LongRun) cannot. As a result of this fine tuning, more chips fall within the target performance specifications, tightening the distribution of parts coming off the production line.

Plan C: Develop More IP

LongRun2 is clever technology, but it's not enough to sustain a whole company for long. Transmeta now has plenty of

money to invest. What's next? Heinlein says the company is "reviewing all its options." Meanwhile, the plan is to continue focusing on licensable IP. One option almost completely off the table is reviving the microprocessor-manufacturing business. However, Transmeta doesn't rule out licensing its microprocessor technology in some form.

At first glance, it would seem that converting the company's existing technology into licensable IP is a logical step. Efficeon is one example of that technology. In theory, Transmeta could license the low-power core to chip developers, just as ARM and other processor-IP companies license their CPU cores. Even though Transmeta had little success finding customers for Efficeon, the core might be useful in some ASICs and SoCs that need x86 compatibility.

However, it's unlikely that Transmeta will license Efficeon as an IP core in the same way ARM does. For one thing, Transmeta didn't design Efficeon (or Crusoe) as a licensable core, so it doesn't exist as a standalone, synthesizable, process-portable model that's ready for integration. Second, Efficeon isn't truly x86 compatible—it has a proprietary VLIW architecture that requires Transmeta's code-morphing software to achieve x86 compatibility. Third, Intel is known to be developing a new low-power x86 microarchitecture (Silverthorne) for the embedded market, and the last thing Transmeta needs is another processor showdown with Intel. Fourth, the processor-IP business is already crowded with stiff competition, including industry leader ARM, ARC International, MIPS Technologies, and Tensilica.

Another possible source of licensable IP is the aforementioned code-morphing software, which is actually a sophisticated x86 emulator and dynamic binary compiler. As with Efficeon, however, Transmeta didn't design this technology as a standalone product suitable for licensing. It's highly optimized for Transmeta's proprietary VLIW architecture. In theory, Transmeta could adapt the software for other CPU architectures, but the programmers who developed it are no longer with Transmeta. And again, there is existing competition from companies like Transitive. (See *MPR 8/8/05-01*, "Transitive's Tech Frees ISA Dependence.")

The disappointing conclusion is that Transmeta's most innovative technology—the CPU hardware and code-morphing software that its engineers spent 10 years developing and refining—is largely unsuitable for IP licensing, at least in their present forms. Instead, Transmeta hopes to build an IP business on its last remaining core competency—low-level power management, as exemplified by LongRun and LongRun2.

Whether Transmeta's plan is realistic for a small company unconnected with a foundry or physical-IP provider remains to be seen. Certainly, Transmeta now has the financial resources to expand in almost any direction it wants. Any significant expansion will require hiring more talent, because the company's engineering staff has been whittled down to near-maintenance levels. But another company that appears to be successfully making the transition from a fabless-semiconductor business model to IP licensing is Intrinsity, whose Fast14 logic is showing up in new processor cores from AMCC and ARM. (See *MPR 9/24/07-02*, "Intrinsity Turns a Corner.")

Aces in the Hole: The Patents

Although Transmeta's CPU architecture, microprocessors, and code-morphing software aren't very suitable for IP licensing, the patents surrounding those technologies are definitely valuable. Otherwise, Intel wouldn't have settled Transmeta's lawsuit so quickly and so lavishly. However, Heinlein told *MPR* that Transmeta won't become a "patent troll" that aggressively threatens to sue companies unless they license the portfolio. So far, Transmeta hasn't filed a patent-infringement lawsuit since October 2006.

Last July, before Intel settled, AMD invested $7.5 million in Transmeta in return for preferred stock, thereby becoming Transmeta's largest investor. The two companies have a long history of technology collaboration and continue to work together. AMD has some licenses to Transmeta's patents that neither company wishes to publicly disclose at this time. Their relationship is so close that AMD once planned to sell Efficeon chips under the AMD brand, and rumors flew that AMD hoped to acquire Transmeta. An acquisition looks unlikely now, in view of AMD's recent financial difficulties and the $250 million newly added to Transmeta's value. Nevertheless, it's possible that Transmeta's power-management technology will appear in future AMD processors.

Although AMD and Intel are in the clear, other microprocessor companies may be worried about Transmeta's patents, despite Heinlein's assurance that Transmeta won't become a patent troll. Transmeta certainly has the right to sue infringers or negotiate licenses with them. Therefore, it's worth reviewing the patents in question. In this article, *MPR* will focus on the 11 U.S. patents named in the action against Intel. Transmeta has additional patents in the U.S. and elsewhere.

Patents for Multiple Register Sets

Patent 5,493,687: "RISC Microprocessor Architecture Implementing Multiple Typed Register Sets," filed July 8, 1991, issued February 20, 1996. Originally issued to Seiko Epson and later acquired by Transmeta, this patent describes multiple identical banks of registers in a microprocessor. Instead of saving and restoring the registers' contents during each context switch, the processor can simply reference a different bank of registers assigned to each context. In addition, the '687 patent describes general-purpose registers for multiple data types (e.g., integer or floating-point values) instead of dedicated registers for each data type, as Figure 1 shows.

Transmeta's lawsuit alleged that Intel infringed the '687 patent in the P6, Pentium 4, Pentium M, Core, and Core 2 microprocessor families. Although Transmeta's complaint doesn't describe the alleged infringement in detail,

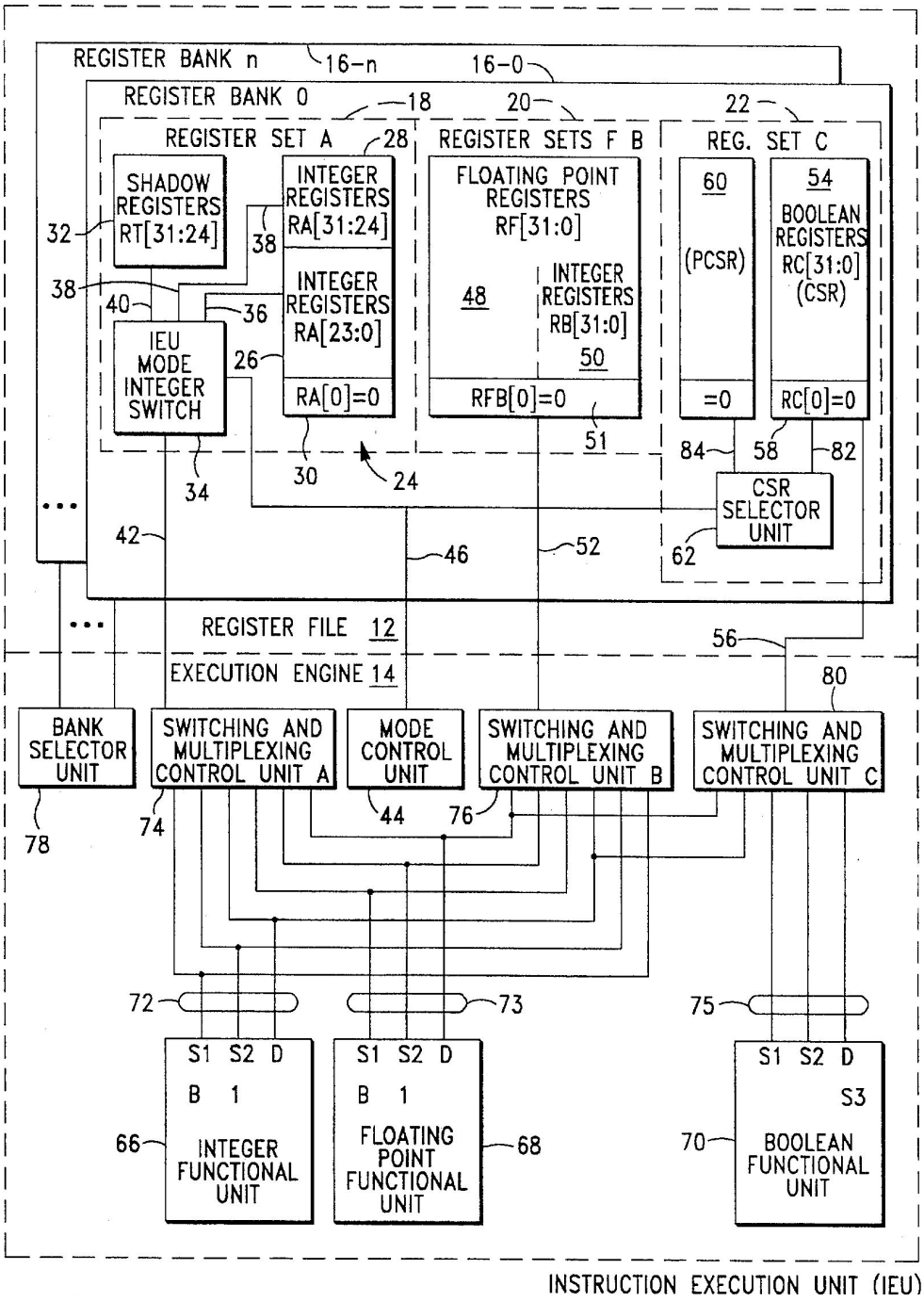

Figure 1. This figure, from Transmeta's '687 patent, illustrates a technique commonly used in microprocessors with hardware-level multithreading—multiple register banks, switchable for each thread context. The bottom part of the figure illustrates a technique less commonly seen—different function units using the same registers for different datatypes.

Intel's Hyper-Threading technology relies in part on multiple register banks—as do many other microprocessors that provide hardware support for core multithreading or fast context switching at the operating-system level.

Patent 5,838,986: "RISC Microprocessor Architecture Implementing Multiple Typed Register Sets," filed September 25, 1997, issued November 17, 1998. Originally issued to Seiko Epson and later acquired by Transmeta, this patent is a continuation of the '687 patent described above. A continuation can have new claims if the original patent specification (the written description and figures) supports the new claims. The advantage of filing a continuation instead of a

wholly new patent is that a continuation inherits the earlier filing date of the original patent. Transmeta's complaint alleged that Intel infringed the '986 continuation patent in the P6, Pentium 4, Pentium M, Core, and Core 2 microprocessor families.

Patent 6,044,449: "RISC Microprocessor Architecture Implementing Multiple Typed Register Sets," filed November 10, 1998, issued March 28, 2000. Originally issued to Seiko Epson and later acquired by Transmeta, this patent is a continuation of the '986 patent, which was a continuation of the '687 patent. Transmeta's complaint alleged that Intel infringed the '449 patent in the P6, Pentium 4, Pentium M, Core, and Core 2 microprocessor families.

All three patents in this group appear to describe a solution for fast context switching widely used in the industry. By equipping a microprocessor with multiple, identical register files, each context (software process) can maintain its working set of data on chip. During a context switch, there's no need to copy the contents of the registers to external memory and then reload the registers with the new context's data that was previously stored in memory. Instead, the processor simply changes a pointer to select a different bank of registers as the new working register set.

Some processors use this technique to support fast context switching at the operating-system level. Other processors use multiple register banks for hardware-level multithreading. In the latter case, instructions from multiple contexts can occupy different stages of the instruction pipeline at the same time. Mixing instructions in the pipeline saves additional clock cycles, because the processor doesn't have to flush the pipeline for each context switch. A hardware-multithreaded processor can switch contexts on every clock cycle, if necessary, simply by toggling among multiple register banks referenced by the instructions. To the operating system, a single-core multithreaded processor may appear to be a multicore processor.

Notice that Transmeta acquired all three of these patents from Seiko Epson, and that the earliest filing date on the patents is July 8, 1991. That date precedes the introduction of multiple register files in some microprocessors from other companies. It would be prudent for those companies to do further research on the prior art.

Patents for Instruction Scheduling

Patent 5,737,624: "Superscalar RISC Instruction Scheduling," filed January 31, 1996, issued April 7, 1998. Originally issued to Seiko Epson and later acquired by Transmeta, this patent describes a register-renaming system for out-of-order execution, plus circuits for identifying and managing any data dependencies among the instructions.

Transmeta's complaint alleged that Intel infringed the '624 patent in the P6, Pentium M, Core, and Core 2 microprocessor families. Of course, all out-of-order processors necessarily have some system for identifying and managing data dependencies. Rename registers and dependency-check circuits are commonplace mechanisms. The '624 patent is a lengthy one, and it's unclear how broadly it applies to out-of-order processors from other companies.

Patent 5,974,526: "Superscalar RISC Instruction Scheduling," filed December 15, 1997, issued October 26, 1999. Originally issued to Seiko and later acquired by Transmeta, this patent is a continuation of the patent application later issued as the '624 patent described above. Transmeta's complaint alleged that Intel infringed the '526 patent in the P6, Pentium M, Core, and Core 2 microprocessor families.

Patent 6,289,433: "Superscalar RISC Instruction Scheduling," filed June 10, 1999, issued September 11, 2001. Issued to Transmeta, this patent is a continuation of the patent application that became the '526 patent described above. Transmeta's complaint alleged that Intel infringed the '433 patent in the P6, Pentium M, Core, and Core 2 microprocessor families.

Like the previous group of patents on multiple register sets, these three patents on rename registers appear to describe a technique widely used in microprocessors from many companies. The basic concept is that a processor has a superset of registers beyond the working set defined by the instruction-set architecture. When the processor begins executing instructions out of order, it moves any associated operands into the extra registers. If an out-of-order instruction passes the dependency checks—and isn't aborted by some other event, like an exception—then the processor renames the extra registers to make them part of the working set of architectural registers.

Transmeta acquired two of these three patents from Seiko Epson. The third patent ('433), originally issued to Transmeta, is a continuation of the others. The earliest filing date is January 31, 1996. Other companies were working on the same concept of register renaming at about the same time, so the strength of these patents is unclear.

Patents for Memory Addressing

Patent 5,895,503: "Address Translation Method and Mechanism Using Physical Address Information Including During a Segmentation Process," filed June 2, 1995, issued April 20, 1999. This patent, naming Rich Belgard as the inventor, describes an improved address-translation method and mechanism for memory management. It can map virtual memory addresses into a linear address space, and it can store information about real-memory pages in segment registers or a special cache. Transmeta's complaint alleged that Intel infringed the '503 patent in Pentium 4 processors.

Patent 6,226,733: "Address Translation Mechanism and Method in a Computer System," filed August 4, 1997, issued May 1, 2001. Naming Belgard as the inventor, this patent is a continuation of the patent application that became the '503 patent described above. Transmeta's complaint alleged that Intel infringed the '733 patent in the Pentium 4 family.

Patent 6,430,668: "Speculative Address Translation for Processor Using Segmentation and Optical [sic] Paging," filed January 10, 2001, issued August 6, 2002. Naming Belgard as

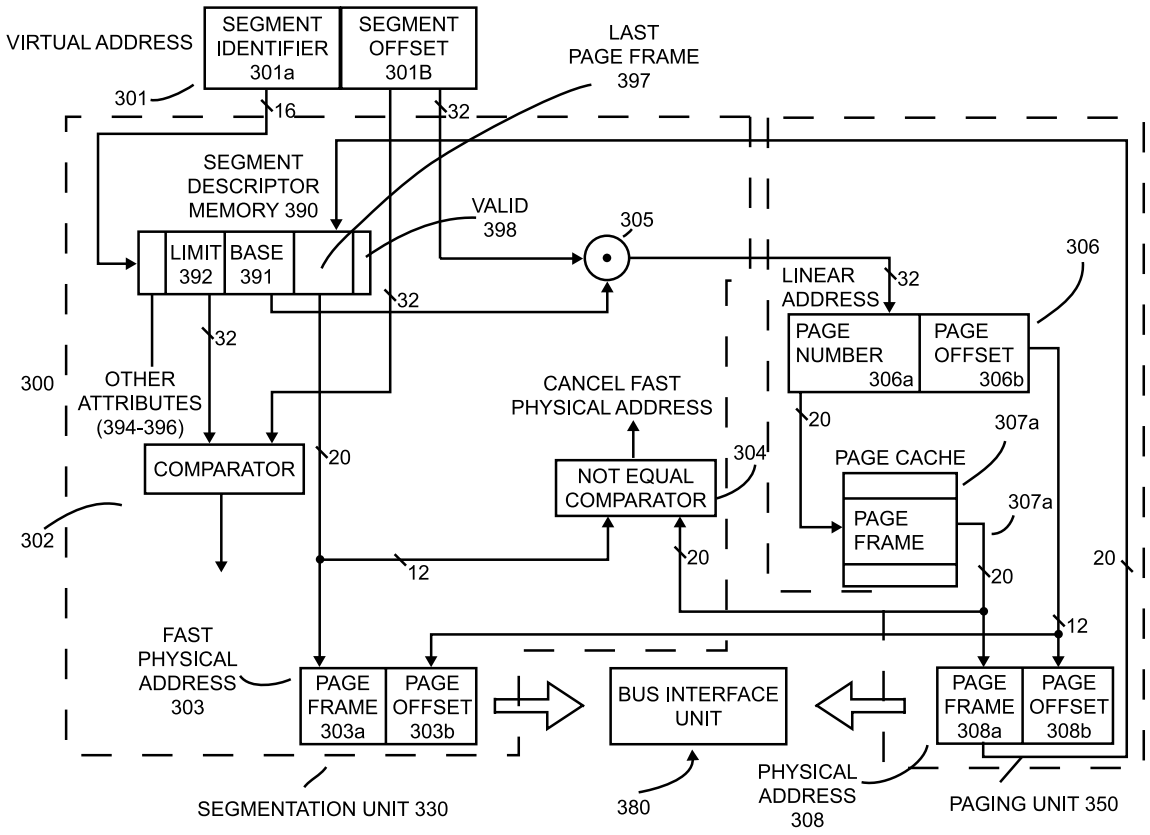

Figure 2. This figure, from Transmeta's '733 patent, illustrates a method for speculatively calculating memory addresses in a microprocessor that has both memory paging and memory segmentation. Although it's not necessarily specific to any particular CPU architecture, this patent is most applicable to the x86.

the inventor, this patent is a continuation of the patent applications that became the '503 and '733 patents described above. It's also a continuation of an application filed on August 4, 1997, later issued as patent 5,960,466 on September 28, 1999. Transmeta's complaint alleged that Intel infringed the '668 patent in Pentium 4 processors. (Note: When the patent office issued the '668 patent, the title inadvertently substituted the word "optical" for "optional." There is no optical technology involved.)

Patent 6,813,699: "Speculative Address Translation for Processor Using Segmentation and Optional Paging," filed June 10, 2002, issued November 2, 2004. Naming Belgard as the inventor, this patent is a continuation of the application that became the '668 patent described above. Transmeta's complaint alleged that Intel infringed the '699 patent in Pentium 4 processors.

All four of Belgard's patents relate to a speculative translation lookaside buffer (TLB) or speculatively addressed memory with independent segmentation and paging mechanisms. Although these patents aren't specific to the Intel x86 architecture, they describe technology that improves the efficiency of the x86's infamously convoluted memory addressing. The x86 is one of the few CPU architectures with independent segmentation and paging mechanisms—a holdover from the architecture's origins in the 1970s and of later attempts to improve the memory addressing.

In the 1980s, Intel designed the 386 processor to be compatible with the 286 processor, which had memory segmentation but not paging. Intel tacked paging onto the result address after segmentation. However, this solution requires the processor to complete the segmentation process before applying paging. Usually, the page address of reference n is the same as the page address for reference n–1, so it's possible to guess that it refers to the same page and start the reference. Simultaneously, it's possible to apply the paging, then check if the speculative address was correct. If so, the processor could save a few clock cycles for all those memory references. If the speculative address was wrong, the processor could abort the memory reference and reissue it correctly. Belgard's patents describe an apparatus and methods for performing these operations (see Figure 2), and Transmeta found them sufficiently interesting to justify their acquisition in 2001.

A Key Patent for Power Management

Perhaps the most important patent named in Transmeta's lawsuit is 7,100,061, "Adaptive Power Control," filed January

18, 2000, issued August 29, 2006. Issued to Transmeta, this patent describes a method for dynamically changing the clock frequency and voltage of a microprocessor in response to different operating conditions, including different software workloads. It is the foundation of Transmeta's LongRun power-management technology.

The '061 patent describes many scenarios for dynamic voltage/frequency control, such as stepping the voltage first, then the clock frequency, or stepping the clock frequency first, then the voltage. (See Figure 3.) The processor may continue executing the workload at the new voltage and frequency or enter a lower-power sleep state or halt state. The patent describes numerous technical details, including a lookup table of paired voltage-frequency levels that the processor may reference when making these adjustments.

LongRun was a key factor in the low power consumption of Crusoe and Efficeon processors. (Another factor was their compact VLIW architecture, which shifted much of the logic normally required for x86 compatibility into the code-morphing software.) Although the '061 patent is broad in scope, several claims narrowly describe specific aspects of LongRun, such as the voltage-frequency lookup tables. (For more details about Transmeta's power-management technology, see the sidebar "Transmeta Explains LongRun" in *MPR 7/10/00-02*, "Top PC Vendors Adopt Crusoe," which expands on the explanation in *MPR 2/14/00-01*, "Transmeta Breaks x86 Low-Power Barrier.")

Note that Transmeta filed the '061 patent application the day before Crusoe's dramatic public debut on January 19, 2000. Less than two months after the patent was issued in August 2006, Transmeta filed its lawsuit against Intel (October 11, 2006). Transmeta's complaint alleged that Intel infringed the '061 patent by using Enhanced SpeedStep Technology in Pentium 4, Pentium M, Core, and Core 2 processors. Of all the allegations in Transmeta's lawsuit, this one was the most specific.

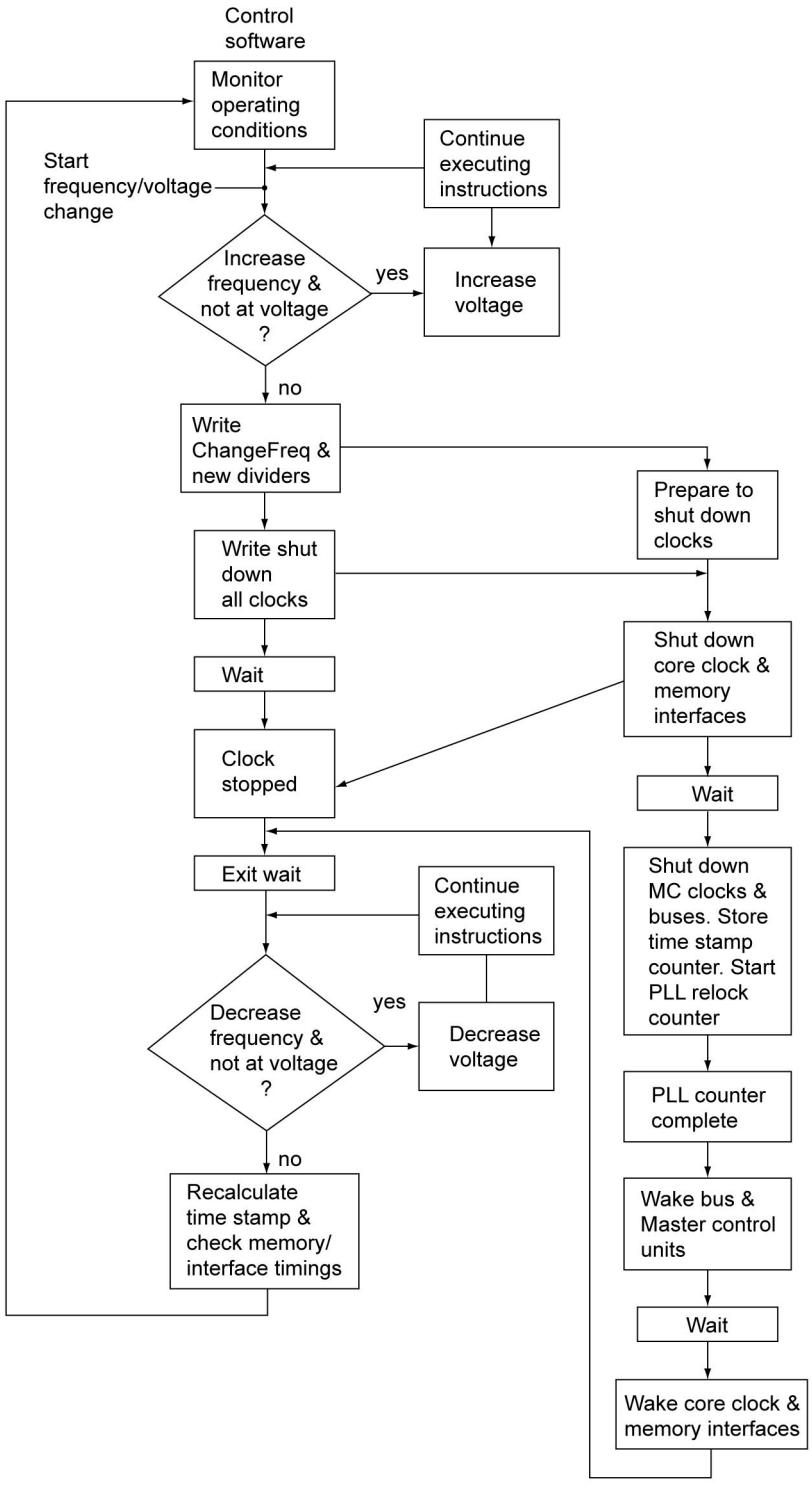

Figure 3. This figure, from Transmeta's '061 patent, is a flow chart describing one way of dynamically adjusting the clock frequency and voltage of a microprocessor to save power. This key patent is the foundation of Transmeta's LongRun technology.

As its name implies, Intel's Enhanced SpeedStep Technology was an improvement over the original SpeedStep, which was Intel's first response to LongRun. The original SpeedStep wasn't nearly as sophisticated as LongRun. Instead of changing the processor's voltage and clock frequency dynamically in response to different workloads, SpeedStep merely lowered the voltage and frequency when a notebook computer was unplugged and switched to battery power. (Critics called it "SlowStep.") Apparently, Transmeta

For More Information

For more information about Transmeta, visit www.transmeta.com. Below is a chronological summary of Transmeta-related articles published in *MPR* since 1998. Many additional *MPR* articles have discussed Transmeta in relation to other microprocessor companies.

- *MPR 12/7/98-02*, "Transmeta Exposed"
- *MPR 12/28/98-01*, "x86 Competition Thriving"
- *MPR 1/24/2000-05*, "Transmeta Unveils Crusoe"
- *MPR 2/14/00-01*, "Transmeta Breaks x86 Low-Power Barrier"
- *MPR 7/3/00-02*, "Intel Strikes Back at Transmeta"
- *MPR 7/10/00-02*, "Top PC Vendors Adopt Crusoe"
- *MPR 8/28/00-04*, "Transmeta Files for IPO; Wins Sony"
- *MPR 11/6/00-01*, "Intel's Cool New Mobile Roadmap"
- *MPR 2/5/01-01*, "Transmeta Forecast for 2001"
- *MPR 2/22/01-04*, "Best Mobile PC Processor of 2000"
- *MPR 7/2/01-01*, "Crusoe Gets Skinny With TM5800"
- *MPR 7/30/01-05*, "Transmeta 2Q01 Results Fall Short"
- *MPR 10/15/01-01*, "Transmeta Tips the TM6000"
- *MPR 2/11/02-01*, "2001 PC Survivor Challenge"
- *MPR 1/6/03-02*, "Transmeta Shows New TM8000 Astro"
- *MPR 1/13/03-01*, "Transmeta Charges the Embedded Market"
- *MPR 1/21/03-01*, "Analog and CPU Wizards Reduce Digital Power"
- *MPR 8/23/03-05*, "Transmeta Settles On Efficeon"
- *MPR 10/27/03-01*, "Transmeta Gets More Efficeon"
- *MPR 12/15/03-02*, "Award Nominees Announced"
- *MPR 2/9/04-03*, "Mobile Processors Move Forward"
- *MPR 2/9/04-19*, "Better, Faster, Cheaper: Take All Three"
- *MPR 10/18/04-01*, "Transmeta Extends Efficeon Roadmap"
- *MPR 5/2/05-01*, "The Transformation of Transmeta"

considered the original SpeedStep beneath consideration, because the complaint doesn't mention it.

Enhanced SpeedStep vs. LongRun

In contrast, Enhanced SpeedStep works more like LongRun does—but not quite. Whereas LongRun can dynamically change both the processor's clock frequency and voltage over a wide range of levels, Enhanced SpeedStep has only two voltage levels (called "total dynamic power operating modes"), and it can dynamically change the clock frequency only within the scope of those modes. Within those limitations, the clock speed can vary under software control at run time, partly in keeping with the user's power-management preferences. Typically, in notebook computers, Enhanced SpeedStep defines one voltage level for AC power ("maximum performance mode") and a second voltage level for DC power ("battery-optimized mode").

Enhanced SpeedStep first appeared in Intel's Pentium III-M mobile processors (based on the Tualatin die) in October 2001. In maximum performance mode, the fastest version of this processor could vary its clock speed from 866MHz to 1.13GHz at 1.4V. In battery-optimized mode, the voltage dropped to 1.15V, and the clock speed could vary from 667MHz to 800MHz. Enhanced SpeedStep is definitely an improvement over the original SpeedStep, but it still isn't as good as LongRun. The relationship between clock frequency and power consumption is linear, whereas voltage is a squared term in the power equation (Power = CSV2f). Superior voltage flexibility makes LongRun a more effective power-management technology.

Nevertheless, Transmeta evidently thought Enhanced SpeedStep was a little too close to the technology described in the '061 patent, so the lawsuit alleged infringement. Intel's out-of-court settlement does not acknowledge infringement of this patent or any others named in Transmeta's complaint, but it does give Intel a license to the patents. So for Intel, at least, the question is moot. Indeed, Intel can use LongRun or derivative technology in future microprocessors. Perhaps we will see an Enhanced Enhanced SpeedStep.

For other companies using some form of voltage/frequency scaling to save power, the legal air isn't quite so clear. *MPR* is not aware of any microprocessors using this technique before Transmeta revealed LongRun in 2000. Of course, doing something first strengthens the position of any patent. Note that for the purposes of evaluating prior art, the U.S. Patent and Trademark Office generally assumes a date of "conception and reduction to practice" as one year before the filing date. In this case, Transmeta filed the '061 patent on January 18, 2000, so the prior art would have to date before January 18, 1999. *MPR* thinks it would be prudent for other companies using voltage/frequency scaling to research the prior art in view of this priority date.

Once Burned, Twice Shy

Here's how we began our February 2000 report on Transmeta's debut of Crusoe: "Like moths drawn to a flame, semiconductor startups seem to find the bright but dangerous glow of the x86 market irresistible. Never mind that companies as resourceful as AMD, Centaur, Cyrix, IBM, National Semiconductor, and Rise have all charred their wings in the fires of competition with Intel. More than 120 million x86 chips were sold in the profitable PC market last year, casting off a warmth that lures newly hatched companies from the darkness. The latest newcomer to emerge from its cocoon is Transmeta."

At the time, Transmeta didn't like our funereal summary of the x86 market, nor our worry that code-morphing software would penalize Crusoe's performance, nor our warning that competing directly with Intel's x86 processors

was a risky gambit. Unfortunately for Transmeta, our concerns were valid. After burning through nearly $700 million in 12 years, and getting burned in the process, Transmeta will probably choose its future competitors a little more carefully.

However, we don't blame Transmeta for challenging Intel, just as we don't blame AMD for continuing to compete against Intel. Events of recent years have shown that Intel is formidable, but not infallible. It's just that competing directly with Intel in the x86 market demands resources greater than most startups can muster. Even AMD has trouble keeping up.

Developing and licensing lower-level IP is a good start for the reborn Transmeta. Downtown streets in San Francisco are named not for the Gold Rush miners of 1849 but for the savvy businessmen who sold tools and supplies to the miners. Those merchants made money whether the miners struck gold or not. Perhaps Transmeta can find a niche by licensing clever technology that helps other companies make successful processors. Crusoe and Efficeon embodied some innovative ideas, and we won't be surprised if some of those ideas resurface in the future.

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