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ALTERA AIMS FOR ASICS

Altera and Synopsys Offer Nios II Processor for Standard-Cell Designs

By Tom R. Halfhill {12/17/07-02}

Altera's Nios II embedded-processor core is now a triple-threat contender. Thanks to a partnership with Synopsys, developers can license the 32-bit synthesizable processor for standard-cell implementations in ASICs as well as for FPGAs and structured ASICs.

Previously, Nios II was restricted to Altera's FPGAs and HardCopy II structured ASICs, although Altera occasionally made special arrangements with favored customers. Now, anyone can license Nios II for a standard-cell design flow using industry-standard design tools, including the popular electronic-design automation (EDA) tools from Synopsys.

The Altera-Synopsys deal creates new opportunities for Nios II developers. They can test and deploy a small-volume design in an FPGA first, then migrate the design to a structured ASIC or standard-cell ASIC if sales exceed expectations. Developers can also move a design from an FPGA to an ASIC to improve performance. By sticking with the same processor core for these various implementations, developers can preserve their engineering investments in SoC design, application-specific logic, and software.

Synopsys brings additional goodies to the party. Nios II becomes part of the Synopsys DesignWare Star IP (intellectual property) portfolio, which includes CPU and DSP cores from other allied companies. The Synopsys DesignWare portfolio offers additional IP directly from Synopsys, including synthesizable peripheral components and mixed-signal physical-interface (PHY) blocks. Furthermore, Synopsys is packaging the Nios II core in the same manner as other DesignWare IP, ensuring tight integration with Synopsys EDA tools. By relying on Synopsys for ASIC IP licensing and EDA expertise, Altera remains focused on its traditional FPGA business while creating new options for Nios II customers. Synopsys says the standard-cell Verilog model for Nios II will be available in 1Q08.

Juggling Price and Performance

Altera introduced the Nios 32-bit processor for FPGAs in 2000 and significantly improved the architecture with Nios II in 2004. (See *MPR 6/28/04-02*, "Altera's New CPU for FPGAs.") Since then, Altera has shipped more than 20,000 Nios II development kits to more than 5,000 companies, making it the most popular soft processor core for FPGA integration, according to a recent Gartner/Dataquest report. Altera says that all top-20 consumer-electronics manufacturers use Nios II. It's also popular with engineering students and hobbyists, thanks to a royalty-free $495 FPGA license.

Nios II is actually a family of configurable processor cores: Nios II/f (fast), Nios II/s (standard), and Nios II/e (economy). All are variations of the same basic core. For standard-cell implementations, Synopsys will offer only the top-of-the-line Nios II/f, which includes caches, a hardware divider, dynamic branch prediction, and a slightly deeper pipeline than other Nios II cores. Developers can configure the size of the instruction and data caches (0KB–64KB each), the number and size of tightly coupled memories (0 to 4 TCMs, 512 bytes to 64KB each), and the number of interrupt ports (up to 32). Depending on the configuration, a standard-cell implementation of the Nios II/f will range in size from about 65,000 to 85,000 gates, excluding memories. That's larger than an ARM7 but smaller than an ARM9.

One obvious reason for moving an SoC design from an FPGA to an ASIC is to reduce costs in high-volume applications. The least expensive Altera FPGAs with enough programmable gates to accommodate a Nios II core are Cyclone III parts, costing about $4 in large volumes (at least 100,000 units). In small volumes, those parts may cost several times as much. On the other hand, the nonrecurring engineering (NRE) costs for developing an ASIC can reach $1 million or more, depending on the size of the chip, the target fabrication process, and the number of spins required to debug the design. The crossover point when an ASIC becomes cheaper than an FPGA is different for every project, but the curve always tilts in favor of ASICs as volumes rise.

Unfortunately, Altera and Synopsys haven't finalized an important parameter that would help plot that curve: the Nios II/f licensing fee for an ASIC implementation. The aforementioned $495 Nios II license is strictly for FPGA implementations. Altera and Synopsys say the ASIC fee will be significantly higher than $495, but they haven't yet decided how much higher. They expect to announce the licensing fee when the standard-cell Nios II ships next quarter. Until then, we can only speculate. Licenses for similar ARM processors can cost millions of dollars, depending on the terms, but it's doubtful that Synopsys will ask that much money for the Nios II/f. Even so, figure on adding at least two zeros to the FPGA licensing fee.

In addition to reducing costs, another big reason for migrating an SoC design from FPGAs to ASICs is performance. Due to the inherent limitations of programmable logic, a standard-cell implementation will easily outrun an FPGA implementation of the same design. Programmable-logic devices can't match the clock speeds of ASICs in similar fabrication processes, and the standard-cell version of a design should be smaller, too. One counterargument is that FPGA manufacturers are quick to adopt the latest fabrication technologies, whereas ASIC developers often use older, slower processes to save money. However, even if a developer implements a design in a fabrication process that's one or two generations behind the latest FPGAs, the ASIC may still outperform a programmable-logic implementation.

Unfortunately, Altera and Synopsys aren't quoting an important parameter that would help developers calculate the performance improvement: Nios II's maximum clock frequency in standard logic. Nor can Altera or Synopsys estimate Nios II's power consumption, an even more critical specification for an embedded processor. Apparently, the Verilog model isn't far enough along for accurate characterization.

Nevertheless, Altera offers one estimate of throughput, as measured by Dhrystone mips. Figure 1 illustrates the performance gap between ASICs and FPGAs. Altera estimates that a standard-cell Nios II/f processor fabricated in a 90nm CMOS process will deliver about 67% better throughput than the same core implemented in Altera's best Stratix III FPGAs, which TSMC fabricates in a leading-edge 65nm CMOS process. The standard-cell implementation looks even better when compared with Altera's lower-priced Cyclone III FPGAs. And it's twice as fast as a structured-ASIC implementation (Altera's HardCopy II option).

Altera says it remains committed to its HardCopy II program, which allows developers to rapidly port a Nios II design from programmable logic to a structured ASIC. Although structured ASICs haven't fulfilled their early promise, they're still a viable option, and HardCopy II gives developers another set of price/performance trade-offs. One advantage of converting an FPGA-based design to a structured ASIC is that the chips will be pin compatible, so developers can replace the FPGA without redesigning the board. (See our two-part series in *MPR 7/2/07-01* and *MPR 7/9/07-01*, "Structured ASICs: Dead or Alive?")

Nios II Integrates With Synopsys Tools

Synopsys is the ideal partner for this venture because it has the EDA tools and IP that developers will need for their ASIC designs. The Synopsys DesignWare IP portfolio includes peripheral IP (DDR2, Ethernet, PCI Express, SATA, USB, etc.), on-chip interconnects (AMBA AHB, AMBA-3 AXI, OCP, etc.), platform IP, verification suites, and system-level models. All this IP is integrated with Synopsys design tools. Synopsys will deliver the Nios II/f as a synthesizable Verilog model in a Synopsys coreKit wrapper for the coreConsultant tool. Additional deliverables include RTL verification suites, an instruction-set simulator, and synthesis scripts.

Some current Nios II users integrate multiple instances of the processor to create multicore SoCs. In FPGAs, there's no cost penalty for multicore integration, because the $495 FPGA license covers single- and multicore designs. Alas, the rules are different for standard-cell implementations. Altera and Synopsys say multicore ASICs will require a more expensive license, but the price is undetermined. The companies do say that the per-core price of a multicore license will be less than the price for a single-core design. In other words, a dual-core license won't cost twice as much as a single-core license.

There are reasons for Altera and Synopsys to set higher prices for standard-cell implementations of Nios II. For one thing, ASIC developers will probably need more technical support than FPGA developers do. (That said, Altera provides good support to FPGA developers buying large volumes of devices.) Another reason for the higher pricing is that Altera originally conceived Nios II as a way to spur sales of FPGAs; an ASIC implementation doesn't boost Altera's main line of business.

In addition, there's probably a third reason for Altera and Synopsys to ask a higher price for the standard-cell Nios II: to avoid poisoning relations with ARM. Drastically underselling ARM's processors could damage ARM's primary line of business by luring more developers into using Nios II. Altera is more interested in selling FPGAs than in competing with ARM as a processor-IP vendor.

Until recently, Altera's $495 license for using Nios II in FPGAs didn't represent direct competition with ARM,

because ARM forbade its licensees from deploying ARM-based designs in FPGAs. (Prototyping an ARM-based design in an FPGA has always been allowed.) However, ARM recently introduced the Cortex-M1, its first processor core designed and optimized for FPGA deployment. (See *MPR 3/19/07-01*, "ARM Blesses FPGAs.") Altera welcomed the Cortex-M1 as an opportunity to sell more FPGAs and worked closely with ARM to optimize the processor for Cyclone III devices. Although the $495 license for using Nios II in an FPGA is essentially grandfathered, Altera and Synopsys probably don't want to antagonize ARM by underpricing the standard-cell Nios II license by a similar degree (three orders of magnitude). Altera can make more money selling FPGAs than it can by licensing processor cores.

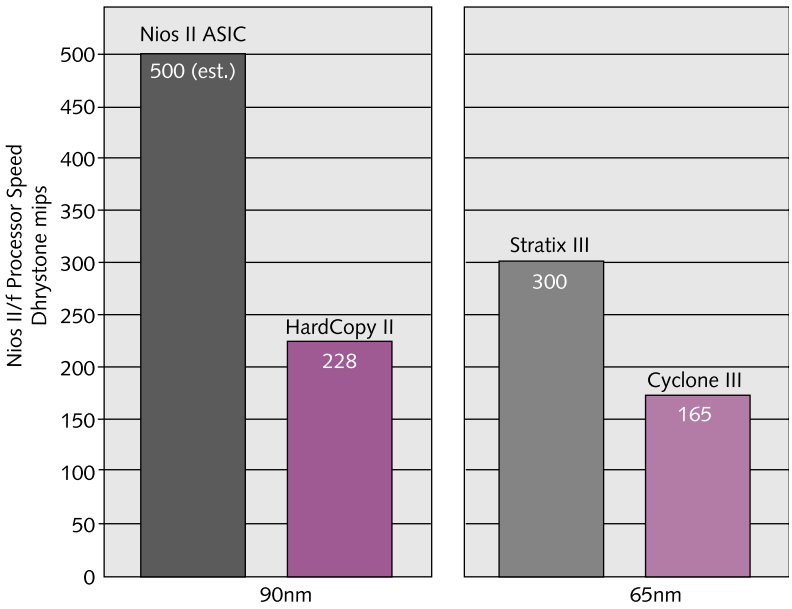

Figure 1. Altera's estimated performance of the Nios II/f processor when implemented as a standard-cell ASIC, as a structured ASIC, and in programmable logic. Even when manufactured in a process technology a full generation behind the best FPGAs, the standard-cell implementation should run significantly faster. (Data source: Altera.)

Surveying the Competition

Nios II hasn't markedly changed since 2004, but it was a good processor to begin with and remains competitive with other 32-bit embedded-processor cores in its class. Altera's main rival, Xilinx, recently gained an advantage by introducing an optional memory-management unit for its MicroBlaze processor core. (See *MPR 11/13/07-01*, "MicroBlaze v7 Gets an MMU.") One advantage that Nios II retains over MicroBlaze is a customizable instruction-set architecture (ISA), which allows developers to create application-specific extensions. In addition, Altera has steadily improved the development tools surrounding Nios II. Those tools include an IP-integration environment called SOPC (System On Programmable Chip) Builder and the C-to-Hardware (C2H) Acceleration Compiler. Of course, the new migration path from FPGAs to ASICs is another plus for Nios II.

In many ways, ARM's Cortex-M1 suffers when compared with the Nios II/f. Altera's processor has instruction/data caches, a 32-bit divider, dynamic branch prediction, an optional FPU, two privilege levels, a configurable ISA, more flexibility with TCMs, and a deeper pipeline. Despite these extras, the Nios II/f is more compact than the Cortex-M1.

On the other hand, the ARM architecture is practically the industry standard. ARM licensees can implement the Cortex-M1 in FPGAs from virtually any vendor, whereas the FPGA version of the Nios II is restricted to Altera FPGAs. (Likewise, Xilinx restricts its MicroBlaze processor to Xilinx FPGAs.) ARM, like Altera, offers an easy path to ASICs—though not quite in the same way. The Cortex-M1 is for FPGAs only, but developers can upgrade to a more capable (and software-compatible) ARM processor, such as the Cortex-M3. It's even possible to dodge the higher price of a Cortex-M1 license by purchasing FPGAs from Actel, which sells devices that include an ARM sublicense in the price of the chip.

Table 1 summarizes the features of some 32-bit synthesizable embedded-processor cores sanctioned for deployment in FPGAs. (Other processor-IP vendors—such as ARC International, MIPS Technologies, and Tensilica—don't encourage FPGA implementations and haven't optimized their cores for programmable logic.) This table includes the latest performance specifications for the Nios II/f in Altera's top-of-the-line Stratix III devices, which was omitted from our recent report on MicroBlaze v7.

An unexpectedly strong competitor for Nios II is the Gaisler Research LEON3, a SPARC-compatible embedded-processor core with the same implementation flexibility as Altera's processor. Gaisler will license the LEON3 for deployment in FPGAs, structured ASICs, or standard-cell ASICs. Unlike Nios II, the LEON3 has an optional MMU and industry-standard AMBA AHB I/O interfaces. (The Nios II's Avalon interface is Altera's own interface technology.) In FPGAs, however, the LEON3 is significantly larger and slower than the Nios II/f, probably because it hasn't been finely tuned for programmable logic. In standard cells, the LEON3 can reach 400MHz in a 0.13-micron process. (As mentioned above, Altera and Synopsys haven't yet estimated Nios II's maximum clock speed in standard cells.)

LEON3's VHDL source code is freely available for research and education through a GNU Public License (GPL). For commercial use in FPGAs, Gaisler licenses the processor for €20,000 (about $29,500). For commercial use in ASICs, Gaisler licenses the LEON3 processor for €35,000 (about $51,700). Note that both the GPL and commercial

Feature	Altera Nios II/f v7.2	ARM Cortex-M1	Gaisler LEON3	Xilinx MicroBlaze v7.0
Architecture	Nios II	**ARMv6-M**	SPARC V8	MicroBlaze
Primary FPGA Targets	Cyclone, Stratix	**Fusion, ProASIC3, Stratix, Virtex-4/5, Cyclone, Spartan**	Any FPGA	Virtex-5 Spartan-3
Structured ASIC	HardCopy II	—	Any process	—
Standard-Cell ASIC	Any process	—	Any process	—
Configurable ISA	Yes	—	—	—
Pipeline Depth	6 stages	**3 stages**	7 stages	5 stages
I-Cache	0–64K	—	0–1MB	0–64K
D-Cache	0–64K	—	0–1MB	0–64K
Local Memory	0–4 512 bytes–64KB each	**0 or 2 1K–1024K each**	0 or 2 Configurable	0 or 2 256K each
32-Bit Multiplier	Optional	**Two options**	Yes	Optional
32-Bit Divider	Optional	—	Yes	Optional
Barrel Shifter	Optional	**Yes**	Yes	Optional
FPU	Optional 32 bits	—	Optional 32 / 64 bits	Optional 32 bits
Branch Predict	Dynamic	—	—	—
Privilege Levels	2	**1**	2	1 or 2
Coprocessor Interface	Avalon	**AMBA-Lite**	AMBA 2.0 AHB	FSL
On-Chip Interconnect	Avalon	**AMBA-Lite**	AMBA 2.0 AHB	CoreConnect PLB v4.6
Memory Management	—	—	Optional SPARC-Reference MMU	Optional MMU or MPU
Translation Lookaside Buffer (TLB)	—	—	Configurable	Optional 8-entry I + D 64-entry unified
FPGA Core Freq (Max)	265MHz*	**Up to 72MHz † >170MHz ‡**	Up to 125MHz in FPGAs	220MHz
FPGA Integer Performance (Max)	300 Dmips*	**0.8 Dmips / MHz**	1.0 Dmips / MHz	240 Dmips
FPGA FP Performance (Max)	n/a	—	1.0 Mflops / MHz	50 Mflops
FPGA Logic Cells	1,100 ALUTs*	**4,300+ LUT3 tiles (~1,900 LUT4 cells)**	~3,500** (Base config)	960–1,700
ASIC Core Freq (Max)	n/a	—	400MHz (130nm)	—
Introduction	2004 (Upgraded 4Q07)	**4Q07**	2004	2001 (Upgraded 4Q07)
Price	ASIC: n/a FPGA: $495	FPGA: <$100,000 (ARM) FPGA: Free (Actel)	ASIC: $51,700 FPGA: $29,500	FPGA: $495

Table 1. Feature comparison of synthesizable 32-bit embedded-processor cores marketed for deployment in programmable-logic devices. Altera offers two additional versions of Nios II (the Nios II/s and Nios II/e), but the Nios II/f is the fastest, fully featured version—and the only one Synopsys will license for a standard-cell design flow. Altera and Synopsys plan to announce the Nios II/f ASIC licensing fee when the standard-cell version ships in 1Q08. *Performance when synthesized in an Altera Stratix III FPGA. †Estimate for synthesis in an Actel ProASIC3 or Fusion FPGA. ‡Estimate for synthesis in a Xilinx Virtex-5 FPGA. **Estimate for synthesis in an Altera Stratix II or Xilinx Virtex-4 FPGA. (n/a: data not available.)

licenses include not only the LEON3 processor core, but also the Gaisler Research Library (GRLIB)—an impressive collection of peripheral IP. GRLIB includes memory controllers (SRAM, SDRAM, DDR1, DDR2, and PROM) as well as popular interface controllers (USB 2.0, Gigabit Ethernet, UARTs, and more). Equivalent third-party IP for other processors could cost hundreds of thousands of dollars.

An Upwardly Mobile FPGA Processor

Altera's goal is to provide developers with a migration path that spans all the common options for implementing chip designs: FPGAs, structured ASICs, and standard-cell ASICs. Altera appears wholly uninterested in becoming a leading processor-IP vendor. Instead, Altera wants to build on Nios II's success in FPGAs and remove an obstacle that might deter developers from starting a design with Nios II.

Just because Altera originally designed Nios II for FPGAs doesn't mean developers can't consider the processor as their first choice for an ASIC. Nios II's features are competitive with those of similar 32-bit soft-processor cores, and Nios II will almost certainly be less expensive to license than most other cores. Under the Synopsys umbrella, the Nios II/f will mesh

with lots of additional peripheral IP. And Synopsys design tools are first rate.

However, several factors make Nios II more suitable for FPGA-based designs that might someday blossom into ASICs, not as the first choice for ASICs. First, it's unclear how effectively Nios II will be optimized for standard cells. Neither Altera nor Synopsys has publicly estimated the processor's maximum clock speed or power consumption in conventional logic—critical parameters that matter a lot to developers. Its size (65,000–85,000 gates) is a small clue to power consumption, but gate counts don't describe the degree of clock gating and other power-saving techniques widely used today in embedded-processor cores.

Another factor against Nios II is that it has less third-party support than some competing architectures do. Market leader ARM enjoys the widest support. ARC, MIPS, and Tensilica have large ecosystems, too. Gaisler's SPARC-compatible LEON3 is enthusiastically supported by the open-source community. Nios II isn't exactly an orphan—over the past several years, it has attracted much support as well. However, to find the best selection of peripheral IP, operating systems, middleware, development tools, educational materials, and engineering experience, most ASIC developers will look to ARM or other CPU architectures.

Nevertheless, Nios II is a compelling choice for developers introducing a design in an FPGA. If sales do take off like a rocket—or if end users demand (and are willing to pay for) more performance than programmable logic can deliver—there's always the option of spinning an ASIC without doing a major redesign. For some developers, that option will be attractive enough to compensate for Nios II's shortcomings.

Price & Availability

Synopsys plans to ship the synthesizable Verilog model of Altera's Nios II/f processor in 1Q08. The processor core will be optimized for standard-cell design flows in industry-standard EDA tools and will become part of the Synopsys DesignWare Star IP library. Synopsys will deliver the Nios II/f in a Synopsys coreKit wrapper for the coreConsultant tool. Additional deliverables will include RTL verification suites, an instruction-set simulator, and synthesis scripts. Altera and Synopsys plan to announce the ASIC licensing fee when the processor ships in 1Q08. Altera will continue licensing all Nios II-family processors for FPGAs and HardCopy II structured ASICs. The FPGA license is $495. For more information, visit:

- *www.altera.com/corporate/news_room/releases/*
- *products/nr-synopsys_nios.html*