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MIPS 74K PERFORMANCE UPDATE

MIPS Releases Power/Performance Estimates for New Processor Core

By Tom R. Halfhill {6/4/07-01}

At the recent Microprocessor Forum in San Jose, MIPS Technologies released power-consumption estimates and performance benchmarks for the new MIPS32 74K embedded-processor core. These preliminary numbers show the 74K running neck and neck with ARM's Cortex-A8, another 32-bit processor core that uses two-way superscalar pipelining to deliver high performance at relatively low power levels.

Microprocessor Report covered the MIPS 74K in detail shortly after its May 21 debut, but we overlooked some power-consumption estimates. (See *MPR 5/29/07-01*, "MIPS 74K Goes Superscalar.") In her Microprocessor Forum presentation, MIPS Engineering Director Vidya Rajagopalan showed the latest data for a 74Kc processor core synthesized for TSMC's 65nm GP process, using TSMC's standard-cell library and low-VT (threshold-voltage) transistors. The 74Kc processor is a 74K-family core without an FPU.

For these tests, MIPS configured the 74Kc with 32KB L1 instruction and data caches and synthesized two instances of the processor—one optimized for maximum speed, the other optimized for minimum die area. Note that these are only two of many possible variations. As with any synthesizable processor, the results can vary widely, depending on the target fabrication process, design-automation tools, synthesis scripts, cell libraries, core configurations, and other factors. Nevertheless, the two data points that MIPS provides are useful guidelines for developers. Table 1 summarizes the data.

One observation is that even when the 74Kc is synthesized to conserve silicon, it can still reach a high clock speed

Specification	MIPS Technologies 74Kc	MIPS Technologies 74Kc
Synthesis Optimization	Speed	Die Area
Target IC Process	TSMC 65nm GP	TSMC 65nm GP
Cell Library (Logic)	TSMC standard, low V_T	TSMC standard, low V_T
Cell Library (Memory)	Dolphin, standard V_T	Dolphin, standard V_T
L1 Caches (I/D)	32K / 32K	32K / 32K
Clock Frequency (wc)	1.04GHz	830MHz
Die Area (Core)	1.7mm^2	1.3mm^2
Die Area (Total)	2.5mm^2	2.1mm^2
Dynamic Power (Core)	0.53mW / MHz* 551mW @ 1.04GHz*	0.44mW / MHz* 365mW @ 830MHz*
Dynamic Power (Total)	0.76mW / MHz (790mW @ 1.04GHz)	0.63mW / MHz (523mW @ 830MHz)
Leakage Power (Total)	34mW	25mW
Dhrystone 2.1	1.8 Dmips / MHz (1,872 Dmips @ 1.04GHz)	1.8 Dmips / MHz (1,494 Dmips @ 830MHz)

Table 1. Estimated MIPS 74Kc power consumption and performance. When synthesized for maximum speed, the 74Kc runs 25% faster than an identically configured core synthesized for minimum die area. The speedy core is 20–30% larger and uses about 20% more dynamic power. MIPS measured power consumption while running Dhrystone 2.1, which fits entirely into the 32K L1 cache, eliminating I/O power from consideration. (*MPR estimate; other estimates are from MIPS.)

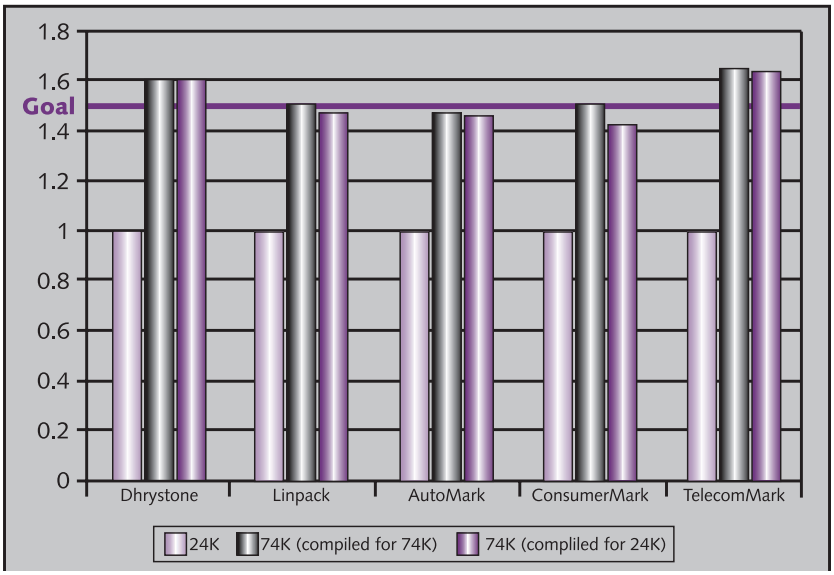

Figure 1. MIPS 74K vs. MIPS 24K performance. At Microprocessor Forum, MIPS showed relative scores from three EEMBC benchmark suites, in addition to Dhrystone 2.1 and Linpack results. Overall, the MIPS 74K meets its goal of delivering 1.5 times the throughput for about 1.5 times the power and die area.

(830MHz) in this moderately fast fabrication process. When synthesized for speed, the 74Kc breaks the 1.0GHz barrier, an impressive achievement for a fully synthesizable embedded-processor core. ARM's Cortex-A8 can also exceed 1.0GHz, but it relies on some prehardened elements. (See our two-part coverage in *MPR 10/25/05-02* and *MPR 11/14/05-01*, "Cortex-A8: High Speed, Low Power.") A fully synthesizable model of the Cortex-A8 would be harder pressed to go beyond 1.0GHz, although ARM licensee Texas Instruments says it's feasible. (See *MPR 7/24/06-01*, "The F1: TI's 65nm Cortex-A8.")

Power Consumption Is Reasonable

As we expected, the MIPS 74K isn't a low-power embedded processor when compared with less capable 32-bit cores. Inevitably, the additional logic required for the 74K's deep superpipelining, dual-issue superscalar pipes, and out-of-order execution takes its toll. Even when fabricated in an advanced 65nm process, the 74K will consume at least one order of magnitude more power than a 32-bit processor in the ARM7, ARM9, or MIPS 4K class. But for embedded applications requiring high throughput, the MIPS 74K is capable of delivering better performance than most other synthesizable processor cores.

For the 74Kc configuration described above, MIPS estimates total dynamic power consumption at 0.76mW per megahertz when the processor is synthesized for maximum speed. When the processor is synthesized for minimum die area, power consumption drops to 0.63mW per megahertz. At their worst-case maximum clock frequencies, those numbers translate into 790mW at 1.04GHz and 523mW at 830MHz. If we exclude the 32KB caches, MPR estimates dynamic power consumption for the cores alone at 0.53mW per megahertz (optimized for speed) and 0.44mW per megahertz (optimized for area).

The MIPS estimates for the 74Kc are quite close to ARM's estimates for a Cortex-A8 core when synthesized for speed in a 65nm process: 0.5mW per megahertz. Naturally, it's almost impossible to make apples-to-apples power-consumption comparisons among synthesizable cores, especially when actual silicon implementations aren't yet available for testing. However, it appears that the MIPS 74K and ARM Cortex-A8 will have similar power-consumption characteristics.

ARM claims the Cortex-A8 delivers 2.0Dmips per megahertz, versus 1.8Dmips per megahertz that MIPS claims for the 74K. That's a small enough difference to ignore, especially with a benchmark test as moth-eaten as Dhrystone. To provide a better estimate of throughput, MIPS surprised us with EEMBC and Linpack benchmark scores based on RTL running in an FPGA. Figure 1 shows the EEMBC, Linpack, and Dhrystone results that MIPS revealed at Microprocessor Forum.

To demonstrate that the 74K's out-of-order superscalar pipelining is good at running existing code, MIPS ran these benchmarks using code compiled for the 24K as well as code optimized for the 74K. The recompiled code runs a little faster, but the differences are marginal. These results tend to confirm the principle that out-of-order processors are less sensitive to instruction ordering than in-order processors are. However, the results may also reflect the relative immaturity of compilers for the 74K—performance may improve further over time. In any event, MIPS says it's important for the 74K to run existing binaries well, because many developers use third-party function libraries that may not be recompiled for the new processor for a while.

Strong Single-Core Performance

At Microprocessor Forum, some critics questioned the introduction of a powerful, complex, single-core processor at a time when multicore designs are the wave of the future. MIPS responded that it has nothing against multicore designs—plenty of MIPS customers have created multicore chips—but that a powerful single-core solution is still best for some embedded applications. It makes sense to exhaust the possibilities of speeding up a single-core processor before resorting to multiple cores. Furthermore, a single-core processor is easier to program than a multicore processor. Although the first point is debatable, no one argues with the second.

MIPS also hinted that a multicore-friendly 74K processor wouldn't be a totally unexpected future development, although it's not on the MIPS public roadmap. MIPS has said that a hardware-multithreaded version of the 74K, similar to

the 34K, is in the works. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.")

MPR agrees with MIPS that there's a place for powerful single-core embedded processors—especially while software-development solutions for multicore designs remain immature. The MIPS 74K is strong competition for the ARM Cortex-A8 and other high-performance synthesizable processors.

Price & Availability

The MIPS32 74Kc and 74Kf 32-bit processor cores are available for licensing now. The 74Kc is the integer-only version, and the 74Kf has a 32/64-bit FPU. Both have the MIPS CorExtend technology, which allows customers to configure the cores and add their own extensions. MIPS doesn't publicly disclose license fees. For more information, visit:
www.mips.com/products/cores/32-bit_cores/MIPS32_74K_Family.php