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MAKING CHIPS FROM THIN AIR

IBM's New 'Air-Gap' Technology Uses Vacuums for Low-k Dielectrics

By Tom R. Halfhill {5/21/07-01}

Vacuum tubes vanished from computers decades ago, but now vacuums are making a surprising comeback. IBM is introducing a new semiconductor-fabrication technique that creates "air gaps"—actually, tiny vacuum cavities—to replace the conventional insulation around copper wiring in integrated circuits. The preliminary results are even better than with the latest low-*k* solid dielectrics.

IBM announced its air-gap technology on May 3, stirring up the usual confused coverage in the mainstream media and even in the trade press. Some reporters seized upon IBM's statement that the technique uses "self-assembly nanotechnology" to claim that the chips practically build themselves. Actually, the "self-assembly" technique applies to only one part of the manufacturing process, and it doesn't really assemble anything. IBM was describing a new liquid material that rearranges its structure after deposition, allowing subsequent fabrication steps to create nanoscale holes, which in turn help create the vacuum cavities. In fact, the "self-assembly" confusion detracts from IBM's most impressive accomplishment: devising a method of leaving tiny gaps between wires without significantly altering the rest of the fabrication process.

IBM commonly refers to the vacuums as air gaps, slots, or cavities. They have a lower dielectric constant (*k*)—the most critical insulating property for wiring—than conventional solid dielectrics do. Lower-*k* dielectrics reduce the capacitive coupling between adjacent wires, thereby improving current flow, especially in long runs of parallel wires. IBM says air gaps can reduce the resistance-capacitance (RC) delay by as much as 35%. Circuit designers can leverage lower capacitance in various ways. They can increase the chip's clock frequency, reduce the chip's power consumption, or choose some combination of those improvements.

Air-gap technology will help designers keep circuit scaling on its historical track. As circuits keep shrinking, the wires in the metal layers are squeezed closer together. Some state-of-the-art microprocessors have more than 20 miles of wiring. But rising RC delay slows signal propagation and forces circuits to run at higher currents. IBM's air gaps—scheduled for mass production in 2009—should allow circuits to continue shrinking, as they have been for decades. There is some concern that the Swiss-cheese chips won't be as physically strong as those with solid dielectrics, but IBM says its preliminary tests for reliability have been successful so far.

Litho vs. Nano for Different Layers

Normally, the wire traces in a chip's metal layers are etched into solid dielectric materials, such as silicon carbon oxyhydride (SiCOH) or fluorine-doped silicon oxide (SiOF). SiCOH is effective for the tightest-pitch wiring in the lower metal layers—those closest to the polysilicon layer containing the transistors. The topmost level of metal requires a much thicker layer of SiOF to strengthen the mechanical interface between the die and the package. Even before announcing the air-gap technology, IBM claimed to have the best dielectrics in the industry. IBM's conventional low-k materials have a dielectric constant of 2.7 in 65nm CMOS and 2.4 in 45nm CMOS. Due to the additional resistance of the higher-k SiCN cap layer, the total effective dielectric constants (k_{eff}) are slightly higher: 3.0 in 65nm CMOS and 2.7 in 45nm CMOS. The best possible dielectric constant is that of a vacuum: 1.0.

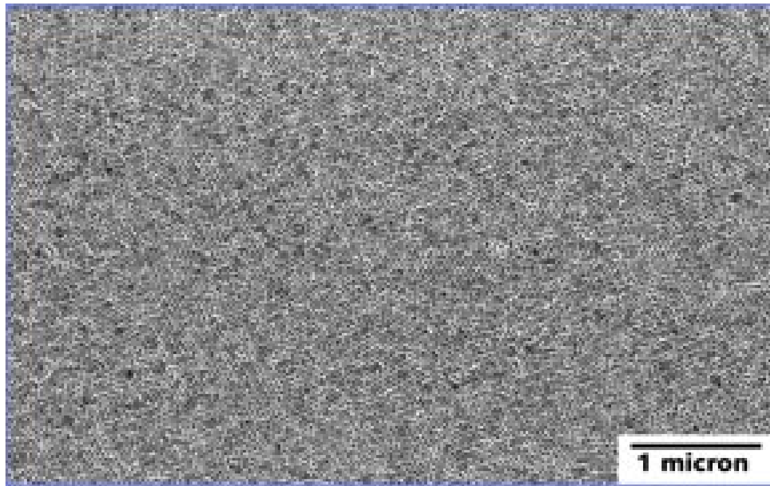

Figure 1. This photograph, taken with an electron-beam microscope, shows the lattice-like atomic structure that emerges after IBM deposits its polymer material on a copper-metal layer. The polymer isn't crystalline but "self-assembles" this pattern as it cures. IBM compares this process to common processes in nature, such as the accretion of tooth enamel, the growth of seashells, and the formation of snowflakes. In later fabrication steps, IBM etches nanoscale holes through this material. The holes eventually result in tiny gaps in the solid dielectric. After special steps to dissolve the partitions between the holes, the result is a cavity in the solid dielectric between the wires.

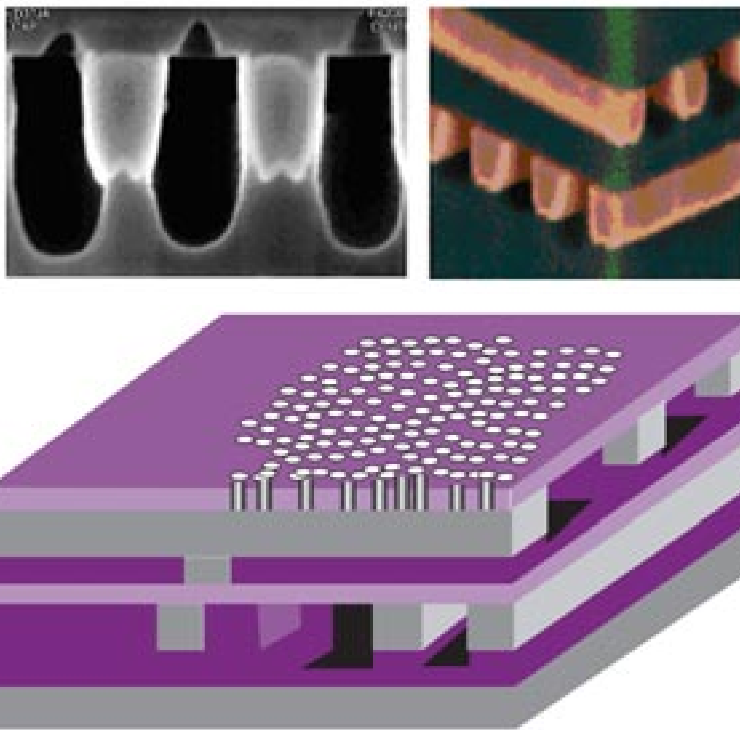

Figure 2. The drawing at the bottom of this figure illustrates the nanoscale holes that allow acids to create gaps in the solid dielectric material. Above are actual photographs of the tiny cavities (which resemble dental x-rays of tooth decay) and their appearance as gaps in the solid dielectrics of the metal layers.

Engineers are constantly seeking lower-*k* dielectrics that are also compatible with existing fabrication processes. Unfortunately, low-*k* solid dielectrics become weaker mechanically and electrically as their dielectric constants decrease. These side effects reduce the viability of new solid dielectrics. Vacuum cavities have been used before in a limited way, but only in exotic fabrication processes more expensive than CMOS.

The challenge for IBM was figuring out how to leave physical gaps around the wires without harming the copper or creating voids that lack structural integrity and thermal conductivity. The critical dimension of the gaps is only half the minimum spacing between the wires. This goal is especially difficult to achieve in the lowest metal layers, which have the tightest wiring pitches. In addition, the extra fabrication steps for creating the gaps should be compatible with the rest of the CMOS manufacturing process, to minimize the impact on design rules and fab lines.

IBM's solution is to create the gaps using two very different fabrication techniques. The simpler technique uses conventional optical lithography and is appropriate for the higher metal layers with the largest pitches. Unfortunately, this technique was inadequate for the lower metal layers with the smallest pitches. Optical lithography simply lacks the resolution to create small enough cavities. Therefore, IBM had to invent an unconventional technique for those layers—the "self-assembly nanotechnology" mentioned above.

For the middle and upper metal layers, IBM uses conventional lithography in a familiar series of fabrication steps. The process starts with a conventional layer of copper wiring and a conventional insulator, then adds a few low-cost steps to create the gaps. Before depositing the next layer of insulation, IBM pinches off and seals the gaps. IBM devised a way to expand the gaps underneath the small openings in the standard copper cap layer so that the pinching happens rapidly, without refilling the gaps. Because all these steps take place in a carefully controlled vacuum chamber—a common aspect of any chip-fabrication process—the sealed gaps retain vacuums.

It's Like Growing Teeth

The lowest metal layers will get a very different treatment. First, as usual, IBM fabricates a standard layer of copper wiring in a solid low-*k* dielectric (in this case, SiCOH). Next, a standard cap of SiCN (silicon carbon nitride) covers that layer. But this step is followed by a layer of special polymer material that IBM has not disclosed. IBM deposits

this material as a liquid film. As it cures, it automatically rearranges its atomic structure to form a lattice-like pattern. IBM says the material is not crystalline, but its final lattice structure resembles that of a crystal, as Figure 1 shows.

After the polymer material cures, a plasma etches trillions of nanoscale holes through it, deliberately damaging the SiCOH beneath. (Each hole is about 20nm in diameter.) Next, acid removes the damaged SiCOH through the holes, leaving behind contiguous gaps in the remaining dielectric. Normal fabrication steps seal off the gaps with a conventional interlevel dielectric. These steps happen in a vacuum chamber, leaving vacuums in the cavities. Figure 2 illustrates this process.

Ideally, the vacuum cavities would perfectly shield the wires, achieving a dielectric constant of 1.0. However, a significant amount of solid dielectric remains above and below the wiring for mechanical and thermal integrity. This raises the total effective dielectric constant to 2.0—still a big improvement over a solid dielectric. The remaining solid materials maintain the structural integrity of the voids and conduct heat away from the wires, down into the silicon substrate and out of the chip. Without the solid dielectric, the gaps might be too weak to support the metal wires, and the gaps would trap more heat.

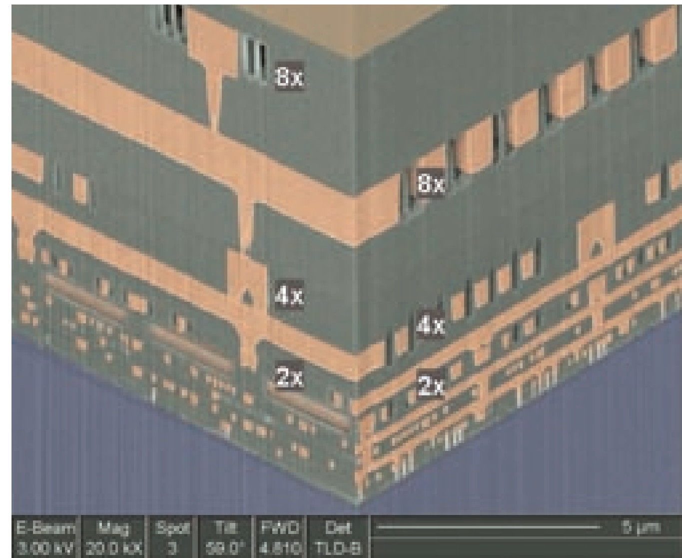

Figure 3. This electron-beam micrograph shows an oblique view of the metal layers in a chip fabricated with IBM's new air-gap technology. The lowest metal layers, nearest to the polysilicon layer containing the transistors, are the thinnest and have the tightest-pitch wiring. IBM must fabricate the gaps in those "1×" layers by etching nanoscale holes through the lattice-like atomic structure of a special material.

Figure 3 shows an oblique view of the metal layers, illustrating the different thicknesses of the layers. This particular chip has 10 layers of metal (not all visible), common for high-performance microprocessors such as IBM's POWER5 and POWER6. Some of the tiny air gaps are visible in this view.

Figure 4 is a closeup view of the final result. The air gaps, again resembling x-rays of tooth decay, vary in size, depending on their metal layer and whether they were created by conventional lithography or IBM's self-assembly nanotechnology. Note that in addition to sealing the cavities, IBM hermetically seals the entire die inside the chip package—common practice, in any case. Sealing is necessary to protect the die from humidity and other ruinous effects of atmospheric contamination, whether or not the chip has air gaps.

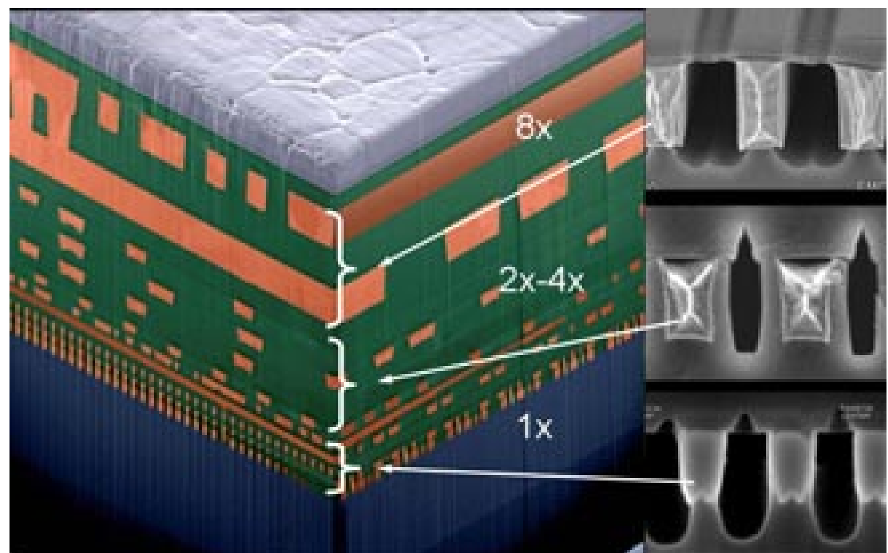

Figure 4. Additional electron-beam micrographs provide startling closeups of the tiny vacuum cavities, which by themselves have a dielectric constant near the ideal of k=1.0. However, notice that some conventionally solid dielectric material (either SiCOH or SiOF, depending on the metal layer) remains behind. Although the residual solid insulation raises the effective dielectric constant to 2.0, it's necessary to provide physical support for these minuscule structures and to help conduct heat away from the copper wires.

Applying Air-Gap Technology to Real Chips

Air gaps aren't a theoretical or far-future technology. IBM plans to ship air-gap processors in 2009, when its fab in East Fishkill, New York, ramps up production in 32nm CMOS. Already, IBM has fabricated fully functional air-gap test chips in its 65nm CMOS process. *MPR* observed a working system with a POWER6 processor manufactured using air-gap technology. Because the technology is not yet in production and testing is still under way, IBM isn't releasing much specific information. According to IBM's preliminary data, air gaps can reduce capacitive coupling by 35%, improve ring oscillation, and reduce the chip's overall power consumption.

IBM says its air-gap test chips are undergoing rigorous testing for performance and reliability. Tests include accelerated

Price & Availability

IBM plans to ship the first commercial chips with air gaps in 2009, when its fab in East Fishkill, New York, begins mass production in 32nm CMOS. IBM hasn't announced which chips will be the first to use air gaps, but the technology's advantages for high performance suggest that POWER6 server processors are a likely candidate. Already, IBM has demonstrated a working system with an air-gap POWER6 test chip. IBM hasn't publicly estimated the additional manufacturing cost of chips with air gaps. For more information about the technology, visit this page on IBM's website:

- *www-03.ibm.com/press/us/en/presskit/21463.wss*

aging in ovens plus other stresses to determine if air gaps impair the chip's physical characteristics. Preliminary results indicate the chips may meet the necessary specifications. Automotive systems are perhaps the most challenging, because of high temperatures in engine compartments and dashboards. (Interestingly, the G-force tests for IBM's mainframe processors are much more stringent than those for aerospace applications.)

Even if air-gap technology isn't suitable for all applications, it won't interfere with IBM's plans. Air gaps won't be an integral part of the fabrication process; they are optional. This is an important aspect of IBM's accomplishment. Because the additional fabrication steps don't require changes in existing steps or tooling, IBM can manufacture chips with or without air gaps in the same basic CMOS process. Air-gap chips will simply take a short detour, then return to the regular process line.

IBM Isn't the Only Beneficiary

Another key point is that air-gap technology, like all IBM fabrication technology, is available to IBM's research alliance partners. Currently, those partners are AMD, Freescale Semiconductor, Sony, and Toshiba. AMD already benefits from IBM's state-of-the-art silicon-on-insulator (SOI) technology and other innovations. Air-gap technology will help keep AMD competitive with Intel, whose resources in process technology vastly outrank AMD's. Freescale may benefit, too, especially if air gaps are suitable for the automotive and industrial processors that are a mainstay of its product lines. Of course, air-gap technology will be available to IBM's foundry customers, as well.

The air-gap project is a relatively small endeavor for IBM, but it draws on many different IBM resources. IBM Research started the project in 2004 at the T.J. Watson Research Center in Yorktown Heights, New York. As the project grew, it needed additional resources from Almaden Research Center in San Jose, California, and the Albany Nanotechnology Center in Albany, New York. For a demonstration of a test chip made in a realistic manufacturing environment, the project used development resources at the Semiconductor R&D Center in East Fishkill, New York; IBM Microelectronics in Essex Junction, Vermont; and the Austin Design Center in Austin, Texas. The project is supervised by Daniel C. Edelstein, an IBM Fellow and manager of IBM's Back-End of Line (BEOL) Technology Strategy. Edelstein also led IBM's introductions of copper wiring in 1997 and copper with low-*k* solid dielectrics in 2004.

Air gaps are a significant addition to other advanced fabrication techniques, such as copper wiring, SOI, strained silicon, high-*k*/metal-gate transistors, and liquid-immersion lithography. The days of judging a process node solely by its geometry are over. A 45nm process isn't necessarily better than a 65nm process when other factors come into play, especially for certain types of designs. CPU architects and circuit designers must pay closer attention to the target process if they want to squeeze out maximum performance, whether they measure performance by die cost, throughput, power, or energy efficiency. IBM's air gaps add yet another factor to this equation. ◇

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