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MICROPROCESSOR REPORT

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PREVIEW: MICROPROCESSOR FORUM 2007

Intel Headlines Conference on Multicore, Video, Graphics, and Low Power

By Tom R. Halfhill {5/14/07-01}

With three keynote addresses, 20 technical presentations, and a full-day seminar on power efficiency—plus our traditional Tuesday-evening expo and party—**Microprocessor Forum** will celebrate its 19th anniversary this year. Dozens of companies are participating as presenters or sponsors. This event will be the only Microprocessor Forum in the U.S. in 2007, moving from its usual time in the fall to May 21–23 in San Jose, California. The only other scheduled forum is **Microprocessor Forum Japan**, on June 19–20 in Tokyo. Several factors, most notably the scheduling of other industry conferences, persuaded In-Stat to move the long-running fall forum to the spring this year.

Otherwise, it's the same Microprocessor Forum that annually attracts hundreds of engineers, technical business managers, venture capitalists, reporters, and other attendees. It will be held at the Doubletree Hotel in San Jose (Silicon Valley). Separate admissions are available for the one-day seminar, two-day conference, and evening expo, as well as package tickets to multiple events. (For web links and registration information, see the "For More Information" box accompanying this article.)

Companies delivering technical presentations at the conference this year include AMD, Applied Micro Circuits Corporation (AMCC), ARM, Freescale Semiconductor, Intel, IPFlex, MEARS Technologies, MIPS Technologies, Nvidia, Parimics, Qualcomm, Renesas Technology, Stream Processors, Stretch, and Tensilica. Sponsors include ARC International, EDN, Freescale, Intel, MIPS, and Qualcomm.

Technical Seminar on Power Efficiency

Microprocessor Forum begins on Monday, May 21, with an optional all-day technical seminar, "Power-Efficient Performance for Multimedia Applications," chaired by Max Baron, a principal analyst for In-Stat and *Microprocessor Report*. The interactive seminar opens with Baron's presentation, a status update on low-power technology and multimedia.

Next comes the seminar's deep tutorial section, which includes 11 technical presentations from different experts. Three tutorials will address the influence of new semiconductor processes and chip-level integration on design decisions. Two

PHOTO: MPR

At last year's Microprocessor Forum, Intel's Dileep Bhandarkar delivered a well-received presentation on future power-management technology. Microprocessor Forum is the longest-running independent technical conference on all aspects of microprocessors.

tutorials will give examples of new architectural configurations. Another tutorial will examine different methods for measuring power efficiency.

Four tutorials will provide the latest information about software-development tools, applications, and system software. Finally, the last tutorial will be an overview of semiconductor physics relevant to chip developers. Participating companies are Calypto, Infineon, IPextreme, Marvell, MEARS, Mistletoe, PTR Group, Tensilica, and Texas Instruments.

MPF Conference: Day 1

The two-day conference begins at 9 a.m. on Tuesday, May 22, with a 45-minute keynote address by Mark T. Bohr, an Intel Senior Fellow and the director of **Intel's Technology and Manufacturing Group**, Process Architecture and Integration. Bohr's keynote will review Intel's high-*k* and metal-gate transistor technologies and their effects on the future of the semiconductor industry. (See *MPR 2/26/07-04*, "*MPR* Innovation Award: High-*k*.")

After his keynote, Bohr will chair a special session, "Advances in Computer Technology," featuring three technical papers by **Intel**. The first is "45nm Next-Generation Intel Core Microarchitecture (Penryn)," by Steve Fischer, a senior principal engineer at Intel. Fischer will discuss major features in the new core design, such as advanced power management, performance improvements, and SSE4 instruction-set extensions. These features will appear in an upcoming family of multicore x86 processors code-named Penryn. Intel will manufacture these chips in a new 45nm fabrication process using the high-*k* and metal-gate technology that Bohr describes in his keynote address. (See *MPR 4/30/07-01*, "Intel Goes on the Offensive.")

Intel's second technical presentation is "Multicore: The Dawning of the Era of Tera," by Jim Held, an Intel Fellow and director of Intel's Tera-Scale Computing Research Program. This program is a worldwide research effort to create new designs with tens to hundreds of cores. Held will discuss Intel's experimental TeraFLOPS research processor (TRP), which has 80 processor cores in a terabit-per-second on-chip interconnect fabric. (See *MPR 4/9/07-01*, "Low-Key Intel 80-Core Intro: The Tip of the Iceberg.")

The third technical presentation from **Intel** is "Reinventing Multicore Cache & Memory: Architecture, Performance, and QoS," by Ravi Iyer, a principal research scientist at Intel. Iyer will analyze multiple-workload scenarios for servers and clients, emphasizing cache and memory scalability, performance, and quality-of-service (QoS) issues. In particular, Iyer will discuss the opportunities and challenges for multicore cache/memory hierarchies in the decade after 2010.

PHOTO: MPR

A Wi-Fi network allows conference attendees to download the latest versions of technical presentations and other materials. In-Stat will also make the materials available on USB flash drives.

Session 2: Power-Reduction Technologies

Following Intel's presentations is the second Tuesday session, "Power-Reduction Technologies," chaired by Jim McGregor, In-Stat's director of research. This will be a relatively short session, with two presentations.

AMD will present "Striking the Balance: Managing Performance and Power Efficiency in Next-Generation Mobile Platforms," by Maurice Steinman, AMD Fellow. Steinman will introduce a new power-management technique that frees the processor from relying on the operating system to coordinate energy consumption.

MEARS Technologies follows with "New Semiconductor Technology Enhances Drive Current, Lowers Leakage," by Robert J. Mears, president and chief technology officer. Mears will describe a new technique for device scaling in chip-fabrication processes smaller than 45nm. This technique enables higher drive currents and reduces gate leakage by inserting a high-mobility epitaxial replacement layer in the silicon channel. It requires no new steps in the fabrication process.

After lunch, *MPR*'s Jim McGregor will chair a discussion panel, "Trends in General-Purpose Processors," featuring the speakers from AMD, Intel, and MEARS who appeared in the morning sessions. This 45-minute panel discussion will include an audience question-and-answer period.

Session 3: Processors on the Move

Tuesday's third session, "Processors on the Move," begins with a 45-minute keynote address by Hideaki Ishihara, senior manager of the Intellectual Property Research and Development Center, IC Engineering Department 1, at **Denso Corporation**. Denso is Toyota's first-tier supplier of automotive electronics. Ishihara's keynote will review the status of automotive processors and discuss their future requirements. Three technical presentations will follow.

Freescale will present "Automotive-Qualified Multicore Microprocessors for Telematics and Industrial-Control Systems," by Jeff Maguire, Freescale's chief architect. Maguire will unveil two new SoCs for automotive telematics. These devices are also suitable for networked industrial-control and

security/surveillance systems, networked patient-monitoring systems, videogames, home media gateways, and set-top boxes.

Parimics comes next with "A Processor Chipset for Real-Time Image Analysis," by Axel Kloth, chief technology officer and vice president of engineering. Kloth will introduce the architecture, design, and implementation of a new chipset designed for image analysis in automotive and other mobile applications.

Renesas wraps up the Tuesday-afternoon session with "SH-Navi2V: A Car Navigation Processor Employing a 38.4-GOPS Image-Recognition Engine," by Toru Baji, manager of Automotive Application Engineering Department 2 at Renesas. This presentation was co-authored by Yoshiyuki Matsumoto, senior engineer of the Car Information System Design Department at Renesas, and Shoji Muramatsu of the **Hitachi Research Lab**. Renesas will disclose technical details of its new car-navigation processor, which has a superscalar SH-4A core and a parallel-processing image-recognition engine.

In keeping with tradition, the first conference day concludes with the Microprocessor Forum Expo and Vendor Showcase in the ballroom from 5 p.m. to 8 p.m. This year's exhibitors include ARC, ARM, Atmel, Berkeley Design Technology Inc. (BDTI), Calypto, Cast, CEVA, Chroma, Codeplay, Green Hills Software, Intel, Intellasys, Intrinsity, MIPS, Obsidian, Shuttle, Sonics, Target Compiler Technologies, Tensilica, Trango Systems, VaST, Virtutech, and Warthman Associates. The expo has lots of food and an open bar. Separate tickets for this event are $95; admission is included with the conference and seminar packages.

PHOTO: MPR

The traditional Tuesday-night Expo and Demo Showcase gives attendees a chance to huddle with industry celebrities while enjoying food and drink.

MPF Conference: Day 2

The second day of the conference begins at 9 a.m. Wednesday with a 45-minute keynote address by Eisuke Miki, president and CEO of **DoCoMo Communications Laboratories USA**. Miki will review the status of Super 3G and 4G cellphone technologies, discussing the tests and experiments carried out to date. Miki will also describe future requirements for cellphone processors from the viewpoint of service providers. Migrating to 4G will provide as much as 1.0Gb/s of data bandwidth, which will be valuable for mobile PCs as well as for cellphones.

After Miki's keynote, *MPR*'s Max Baron will chair the first Wednesday session of technical presentations, "Video and Graphics Multicore Architectures." Four companies will appear in this session before lunch.

IPFlex will present "A Dual-Core Dynamically Reconfigurable Engine Employs 955 Parallel-Processing Elements," by Tomoyoshi Sato, IPFlex's vice president and chief technology officer. This will be the first public disclosure of IPFlex's new high-performance processor, which has parallel-processing capabilities difficult to obtain with conventional ASICs. Sato's presentation will provide technical details about the parallel-processing features and describe some example applications. (See U.S. patent 6,904,514, issued June 7, 2005.)

Nvidia then presents "CUDA Software and GPU Parallel Computing Architecture," by John Nickolls, Nvidia's director of architecture. This will be the first detailed public disclosure of Nvidia's massively multithreaded computing architecture and CUDA (Compute Unified Device Architecture) software for GPU computing. Nickolls will describe a scalable parallel architecture that delivers high throughput for data-intensive processing.

Stream Processors follows with "Making Parallel Processing Simple—Storm-1: A Massively Parallel C-Programmable 112GMACS Stream Processor," by Bill Dally, the company's co-founder, chairman, and chief scientist (and a professor at Stanford University). Dally will announce the SP16HP-G220, the new flagship of the Storm-1 processor family. The SP16HP-G220 can perform up to 112 billion multiply-accumulate (MAC) operations per second on 16-bit operands, or 440 billion operations per second with 8-bit data.

Stretch wraps up the Wednesday morning session with "A Software-Configurable Processor Architecture for Video Security," by Robert K. Beachler, vice president of product planning. This will be the first public disclosure of Stretch's second-generation software-configurable processor architecture, which is optimized for video surveillance. Beachler will describe a new signal-processing architecture designed specifically to meet the performance demands of high-resolution, intelligent, network-based security applications. (See *MPR 4/26/04-01*, "Stretching Performance.")

Session 5: Embedded Processors and Cores

After lunch, the afternoon presentations begin with a session chaired by *MPR* Senior Analyst Tom R. Halfhill, "Embedded Processors and Cores." This session has four technical presentations by three companies.

AMCC will present "Titan: A Low-Power, High-Performance Core Based on the Power Architecture," by Joe Chang, AMCC's chief architect. This presentation was co-authored by

Steve Horne, the founder of **Intrinsity** and the director of research technology at that company. For the first time, AMCC will publicly disclose details of its new Titan superscalar microarchitecture, which supports multicore designs and uses Intrinsity's Fast14 logic. (See *MPR 1/10/05-02*, "Intrinsity Takes Its IP on the Road.") Although AMCC's 32-bit processor doesn't appear on official Power Architecture roadmaps, *MPR* revealed some information about it last fall. (See *MPR 11/27/06-01*, "Power.org's United Roadmap.")

ARM will present "A New ARM Processor for Synthesis on FPGA," by Ian Devereux, director of technology at ARM's Processor Division. This presentation will provide additional technical details about the Cortex-M1, ARM's first embedded-processor core designed for synthesis and deployment in programmable-logic devices. (See *MPR 3/19/07-01*, "ARM Blesses FPGAs.")

ARM will deliver a second presentation in this session entitled "ARMv7 Architecture Receives Multiprocessor Extensions," by John Goodacre, ARM's program manager for multiprocessing. This presentation will be the first public disclosure of new extensions to the ARMv7 instruction-set architecture. Future ARM multiprocessor designs will be based on these extensions, which improve data security and the maintenance of caches and the translation-lookaside buffer (TLB). Goodacre will also discuss the requirements for multiprocessor systems and review existing hardware and software implementations.

MIPS Technologies finishes this session with "Design for Performance in a Synthesizable Area-Efficient Processor," by Vidya Rajagopalan, director of engineering at MIPS. Rajagopalan will introduce a next-generation family of single-threaded processor cores—the first MIPS processors based on a new microarchitecture optimized for performance, area efficiency, and low power consumption.

Session 6: Application-Specific Platforms

The final session of Microprocessor Forum 2007, "Application-Specific Platforms," is chaired by *MPR*'s Max Baron. This session has three technical presentations by two companies.

PHOTO: MPR

Behind the scenes at Microprocessor Forum. Backstage, our crack audio/video technicians ensure glitch-free presentations…most of the time.

For More Information

Microprocessor Forum 2007 will be held on May 21–23 at the Doubletree Hotel in San Jose, California. The all-day seminar, "Power-Efficient Performance for Multimedia Applications," is on Monday, May 21. The conference sessions are on Tuesday and Wednesday, May 22–23. The Expo and Demo Showcase begins at 5 p.m. Tuesday. Separate admissions are available for the seminar, conference, and expo, as well as package admissions for multiple events. Group discounts and special student tickets are also available. This will be the only Microprocessor Forum held in the U.S. this year. For more information about attending the forum, please contact Elaine Potter (epotter@reedbusiness.com, 480-483-4441). Please note that this preview article is based on preliminary scheduling information; there may be last-minute changes.

General information about Microprocessor Forum 2007:
www.instat.com/mpf/07/
Conference schedule:
www.instat.com/mpf/07/conference.htm
All-day seminar:
www.instat.com/mpf/07/seminar.htm
Expo and Demo Showcase:
www.instat.com/mpf/07/showcase.htm
Online registration:
www.instat.com/mpf/07/register.htm
Microprocessor Forum Japan will be held on June 19–20 at the Izumi Garden Gallery in Tokyo.
Microprocessor Forum Japan (English):
www.ednjapan.com/content/mpf2007/index_english.htm

Qualcomm begins the session with "Scorpion Processor Core for Mobile Applications," by Thomas Sartorius, senior director of technology and principal architect. Sartorius will introduce a power-efficient 1.0GHz ARMv7-compatible superscalar processor with a 128-bit SIMD engine. This high-performance processor is designed for a broad range of mobile applications, including portable game players and communications devices.

Qualcomm will deliver another presentation, "Snapdragon: High-Performance Mobile Platform," by Mark Schaffer, principal engineer and architect. The Snapdragon platform is designed to bridge the gap between high-performance PCs and low-power mobile handsets. Snapdragon uses Qualcomm's Scorpion—the new high-performance processor described in the previous presentation—as well as multimedia accelerators and a high-performance DSP.

Tensilica ends this session with "A Dual-Core Video Decoder/Encoder," by Dennis Moolenaar, a member of the technical staff at Tensilica. Moolenaar will reveal the implementation details of its Diamond Standard 388VDO Video

Engine—a preconfigured video processor that has two Tensilica Xtensa LX embedded-processor cores. This design uses Tensilica's unique Flexible-Length Instruction eXtensions (FLIX) and Tensilica Instruction Extension (TIE) ports and queues. (See *MPR 11/28/05-01*, "Tensilica Previews Video Engine.")

Technical presentations and other forum materials will be available to attendees over a special Wi-Fi network in the conference ballroom. In addition, these materials will be available on USB flash-memory drives.