Reed Electronics Group

MICROPROCESSOR REPORT

www.MPRonline.com

THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

FREESCALE LICENSES POWER CORES

Power Architecture e200 Processor Cores Available for IP Licensing

By Tom R. Halfhill {4/2/07-01}

For the first time, Freescale Semiconductor is making some of its Power Architecture embedded-processor cores generally available as licensable intellectual property (IP). Until now, only IBM has broadly licensed Power cores to chip developers. Freescale's move strengthens the Power Architecture as an alternative to widely licensed embedded-processor cores from ARM and others.

The first Freescale cores released for licensing are four members of the 32-bit Power e200 family. All are fully synthesizable and portable to virtually any digital IC process. Freescale is using IPextreme, a Silicon Valley-based company, to negotiate licenses with customers, deliver the IP, and provide technical support. (See the sidebar, "Freescale Outsources Licensing to IPextreme.")

Microprocessor Report has been expecting Freescale and IBM to license their Power cores more openly. The most recent hints came in November 2006, when the Power.org consortium released its strategic roadmaps for future development. (See *MPR 11/27/06-01*, "Power.org's United Roadmap.") IBM began openly licensing its 32-bit Power 405 and Power 440 cores in 2003. Last fall, IBM introduced three new licensable Power cores: the 460S, 464-H90, and 464FP-H90. (See the sidebar, "IBM's New Licensable Power Cores," in the previously cited article.) The 464-H90 and 464FP-H90 cores are prehardened for manufacturing at an IBM fab or IBM-approved foundry, such as Chartered Semiconductor or Samsung, but IBM's other cores are available in synthesizable formats and are portable to virtually any fabrication process or foundry.

Likewise, Freescale will allow Power e200 licensees to manufacture their chips at any foundry. Not that there's anything wrong with IBM's fabs or those of its foundry partners—indeed, they offer some of the best semiconductor manufacturing in the world. But other foundries may offer lower prices, and many customers like the freedom to fabricate their chips anywhere. Freescale's new licensing initiative puts the Power Architecture on a more competitive footing against other processor-IP companies, such as ARM, ARC International, MIPS Technologies, and Tensilica.

However, there's one important difference between the licensing businesses of IBM and Freescale. In addition to licensing Power processor cores, IBM can grant architectural licenses to favored customers. An architectural license allows the customer to design a completely new processor core that's compatible with the Power Architecture. One example is P.A. Semi, which created its PA6T processor core for the new PWRficient family of low-power, high-performance multicore processors. (See *MPR 10/25/05-01*, "P.A. Semi: New Blood for Power.") Another architectural licensee is Applied Micro Circuits Corp. (AMCC), which plans to announce an interesting new Power core at this year's Microprocessor Forum in San Jose, California (May 21–23). Freescale, itself an architectural licensee, cannot grant architectural licenses but can license its own Power cores to others.

Power e200 Comes in Four Flavors

Until now, Freescale has licensed a Power Architecture core to only one other company: STMicroelectronics. However, that's a special partnership, not a typical IP licensing deal. Freescale and STMicro are jointly designing e200-based chips that each company will bring to market separately.

These still-unannounced chips are primarily intended for automobiles, a key market for both companies. The joint designs will provide customers with two supply sources and a common hardware/software development platform.

The Power e200 is a respectable 32-bit embedded-processor core introduced in 2004. Although it's three years old, it's still very competitive for automotive controllers, avionics, industrial systems, consumer electronics, and other embedded applications. It was a logical choice for the Freescale/STMicro development project, and it's a worthy debutante for Freescale's new licensing initiative. Freescale says that since 2004, it has sold more than $1 billion worth of e200-based microcontrollers to the automotive industry alone. Last year, according to Freescale, more than one million e200-based chips were sold.

Freescale is offering four different versions of the e200, all as synthesizable Verilog-2 models. Figure 1 shows a block diagram of the highest-end variant, the e200z6. This core is the foundation for some highly integrated standard parts from Freescale, such as the MPC5567 microcontroller.

The other e200 variants available for licensing are the e200z0, e200z1, and e200z3. The most notable difference between these cores and the higher-end e200z6 is the depth of their instruction pipelines—they have only four stages, whereas the e200z6 has seven. With its deeper pipeline, the e200z6 can run at nearly twice the clock frequency of its siblings when fabricated in the same IC process. Other important differences among these cores are the cache, FPU, MMU, and SIMD/DSP extensions, which are missing from some of the lower-end variants.

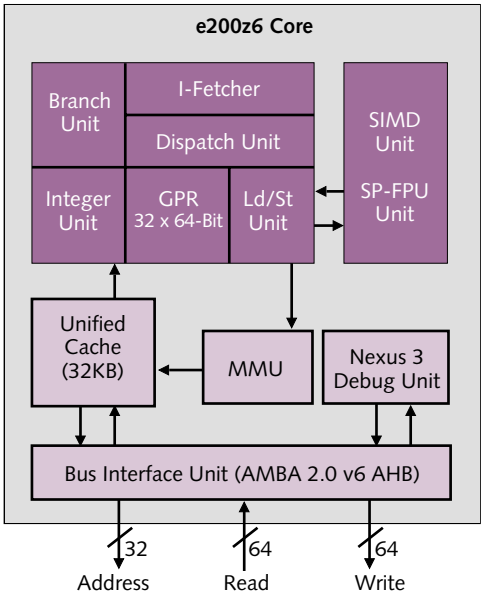

Figure 1. Power e200z6 block diagram. This 32-bit processor core is the highest-end example of the four e200 cores that Freescale is licensing as synthesizable IP. Notable features are a unified cache, single-precision FPU, an MMU to support virtual-memory operating systems, SIMD/DSP extensions, Variable-Length Encoding (VLE) extensions, and an AMBA 2.0 high-speed bus interface. Other e200 variants omit or downsize some of these features to reduce the core's area and power consumption.

Significantly, one feature all four cores share is Variable-Length Encoding (VLE), which supplements the standard 32-bit instruction set with 16-bit-long instructions. Programmers can freely mix 16- and 32-bit instructions together to reduce code size in memory-challenged embedded systems. Freescale says VLE can reduce code size by up to 30%. Table 1 summarizes the features of all four Power e200 cores licensed by Freescale.

VLE was introduced in 2005 by Motorola, Freescale's former parent company. It was a unilateral introduction, not a product of the former PowerPC alliance between Motorola and IBM. Motorola created VLE to address the shortcomings of IBM's CodePack and another code-compression method from Motorola that was used in some early PowerPC automotive controllers. (See *MPR 10/26/98-05*, "PowerPC Adopts Code Compression.") Both those methods improved code density by compressing 32-bit instructions at compile time and decompressing them at run time. However, those methods required a special on-chip decompression unit and weren't popular with developers.

In concept, VLE works more like the 16-bit subsets of the ARC, ARM, MIPS, and Tensilica architectures, which are widely embraced by developers. However, VLE is a self-standing denser encoding of the standard 32-bit integer instruction set—so complete that the Power e200z0 core supports nothing but VLE instructions. After Freescale and IBM joined forces again in the Power.org consortium, they made VLE part of the latest instruction-set architecture (ISA) definition, Power ISA 2.03. (See *MPR 8/21/06-01*, "The New Power Architecture.")

Powerful SIMD/DSP Extensions

In addition to VLE, the e200z3 and e200z6 cores have the Signal Processing Engine (SPE), another Freescale invention. Freescale introduced SPE in 2001 as an auxiliary processing unit for its PowerPC processors. (See *MPR 7/16/01-01*, "Speedier Book E Encore," and *MPR 8/12/02-01*, "Motorola's Embedded PowerPC Story.") SPE is a tightly coupled coprocessor that adds 222 new DSP instructions and single-instruction multiple-data (SIMD) operations. By stretching the standard 32-bit general-purpose registers to 64 bits, Freescale enables SPE instructions to perform single-cycle vector operations on two 32-bit operands in a single register. (Standard 32-bit instructions ignore the upper half of these extended registers.)

SPE is found only in Freescale's e200 and e500 cores. IBM never implemented SPE, because IBM already has the similar AltiVec extensions. AltiVec is more powerful than SPE but requires more silicon, partly because it defines 32 new 128-bit registers instead of stretching the existing 32-bit registers. (See *MPR 5/11/98-01*, "AltiVec Vectorizes PowerPC.") As they did with VLE, Freescale and IBM worked through

Power.org to integrate SPE into the latest Power ISA 2.03. The higher-end e200z3 and e200z6 processors have SPE, whereas the e200z0 and e200z1 cores do not.

Freescale's licensable e200 cores will compete most directly with IBM's licensable Power Architecture cores. For years, the only Power cores that IBM openly licensed were the Power 405, introduced in 1998, and the Power 440, introduced in 1999. (See *MPR 10/26/98-05*, "PowerPC Adopts Code Compression," and *MPR 10/25/99-03*, "IBM PowerPC 440 Hits 1,000 MIPS.") Last fall, with little fanfare, IBM introduced three new Power cores: the 460S, 464-H90, and 464FP-H90. (See the sidebar, "IBM's New Licensable Power Cores," in *MPR 11/27/06-01*, "Power.org's United Roadmap.") All five licensable IBM Power processors are 32-bit cores, like Freescale's e200.

Overall, Freescale's Power e200 is most like IBM's Power 405. Both are relatively simple synthesizable cores with uniscalar pipelining, in-order execution, MMUs, and optional FPUs. Their pipelines are similar: the 405 has five stages, whereas the e200z0, e200z1, and e200z3 have four stages, and the e200z6 has seven. The 405 has dynamic branch prediction and separate 16KB instruction and data caches; the e200z1, e200z3, and e200z6 cores also have dynamic branch prediction, but only the e200z6 has a cache (32KB, unified).

Several differences between the Power 405 and Power e200 could matter a lot to embedded-system developers, and most of these differences favor the e200. First, Freescale offers the e200 in four versions, allowing developers to choose one that's a closer fit for their design. Second, all e200 cores support VLE, which improves code density without the overhead of CodePack decompression. Third, the e200z3 and e200z6 have the SPE coprocessor, which provides a richer instruction set for signal processing and vector math than the Power 405 does. Fourth, e200 cores have an AMBA bus, whereas the 405 has IBM's CoreConnect bus. Putting technical differences aside, AMBA has a larger following in the licensable-IP community. Finally, all e200 cores have a Nexus debug interface, unlike IBM's Power 405 and 440 cores, which have plain-vanilla JTAG.

One factor in IBM's favor, however, is that the Power 405 is available as a synthesizable core and as a hard macro, whereas Freescale licenses the e200 in synthesizable format only. Prehardened cores are less flexible than soft cores, but they run faster and can reduce development time.

IBM Offers Faster Cores

For developers that need to license a higher-performance Power processor, IBM is currently the speed champ. Freescale's most powerful licensable core, the e200z6, suffers in comparison with IBM's higher-end cores: the Power 440, 460S, 464-H90, and 464FP-H90. All those IBM processors have two-way superscalar pipelines, out-of-order execution, and separate instruction/data caches up to 32KB in size. Those features should help them deliver greater raw throughput than the uniscalar, in-order e200z6. IBM's cores are swift, too. The hard-core 464-H90 and 464FP-H90 can hit 1.0GHz when fabricated at 90nm, and even the soft-core 460S reaches 700MHz at that geometry—twice as fast as the e200z6.

Of course, a more advanced microarchitecture and higher clock rates usually come at the price of additional silicon and greater power consumption. But not always. According to IBM, the 464-H90 consumes only 0.53mW per megahertz, including caches, which is a little less than the 0.64mW per megahertz that Freescale specifies for the e200z6 at 90nm. One explanation for this difference is that IBM has invested some custom design effort in the 464-H90 hard macro. Another factor is that the 464-H90 lacks an FPU, unlike the e200z6. FPUs occupy a big chunk of silicon—IBM's 464FP-H90 has one and is 21% larger than the 464-H90 (7.0mm^2 vs. 5.8mm^2). IBM hasn't published power-consumption estimates for the FPU version of this core, but, coincidentally, the e200z6 core with FPU consumes 21% more power than the 464-H90 does without an FPU.

Feature	Freescale Power e200z0	Freescale Power e200z1	Freescale Power e200z3	Freescale Power e200z6
Architecture	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03
16/32-Bit VLE	Yes (only)	Yes	Yes	Yes
Pipeline Depth	4 stages	4 stages	4 stages	7 stages
L1 Cache (Unified)	—	—	—	Up to 32K 8 ways
MMU (Unified)	—	8 entries	16 entries	32 entries
FPU	—	—	32 bits	32 bits
SPE (SIMD)	—	—	64 bits	64 bits
Debug Unit	Nexus 2+	Nexus 1	Nexus 3	Nexus 3
Bus Interface	AMBA 2.0v6 32-bit read 32-bit write 32-bit addr	AMBA 2.0v6 32-bit read 32-bit write 32-bit addr	AMBA 2.0v6 64-bit read 64-bit write 32-bit addr	AMBA 2.0v6 64-bit read 64-bit write 32-bit addr
Freq (Core)	150MHz	150MHz	150MHz	300MHz
Voltage (Core)	1.0V	1.0V	1.0V	1.0V
Size (Core)	0.5mm^2	0.6mm^2	1.4mm^2	3.8mm^2
Power (Core)	0.13mW / MHz	0.16mW / MHz	0.26mW / MHz	0.64mW / MHz
IC Process	90nm	90nm	90nm	90nm
Availability (IP)	Now	Now	Now	Now

Table 1. Freescale derived all four Power e200 licensable processor cores from the same basic design, but they have significant differences. Most notably, the e200z6 has a deeper pipeline, allowing much higher clock frequencies in the same fabrication process. Optional FPUs, MMUs, SIMD extensions, and caches are other distinguishing features. The e200z0 supports VLE instructions only. All clock rates, core sizes, and power-consumption figures in this table are Freescale's estimates, assuming fabrication in 90nm bulk CMOS and worst-case conditions, with operating temperatures to 105°C.

Raw throughput is good for Dhrystone scores but doesn't tell the whole story. For critical signal-processing code, Freescale's SPE and 222 additional instructions could overcome IBM's pipelining and clock-frequency advantages while conserving power, too. Unfortunately, this kind of assessment requires the developer to have access to the cores from both companies before deciding which one to license—not impossible, but not easy, either. Table 2 compares the high-level features of Freescale's highest-performance licensable Power core, the e200z6, with all licensable IBM Power cores: the 405, 440, 460S, 464-H90, and 464FP-H90.

Freescale Faces New Competition

Freescale's licensable cores will also compete with 32-bit processor-IP cores from ARC, ARM, MIPS, and Tensilica. Those competitors have very different and proprietary CPU architectures, so comparisons are less straightforward than those between the Power Architecture cores from Freescale and IBM.

ARM is far and away the market leader in processor IP. In the embedded world—especially low-power applications—ARM is much more pervasive than Power. One exception is automotives, which ARM is trying to remedy with its new Cortex-R4 and Cortex-R4F processors. (See *MPR 10/30/06-01*, "ARM Thumbs a Ride," and *MPR 5/16/06-01*, "ARM Reveals Cortex-R4.") In higher-performance applications, such as networking and communications infrastructures, the Power Architecture is particularly strong and ARM is particularly weak. ARM's superscalar Cortex-A8 is making a bid for those segments. (See our two-part coverage in *MPR 10/25/05-02* and *MPR 11/14/05-01*, "Cortex-A8: High Speed, Low Power.") ARM's biggest advantages over the Power Architecture, besides an entrenched position, are very low power consumption and a larger variety of licensable cores from which to choose. On the other hand, Power Architecture vendors offer a wider variety of standard parts, which complement the licensable cores and SoCs.

MIPS has a strong presence in networking, communications, and consumer electronics. The Power Architecture is well suited for those applications as well. Like ARM, MIPS has a variety of licensable cores from which to choose, including some unique designs, such as the multithreaded MIPS32 34K. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.") The Power Architecture's greatest triumph in consumer electronics is

Feature	Freescale Power e200z6	IBM Power 460S	IBM Power 464-H90	IBM Power 464FP-H90	IBM Power 440	IBM Power 405
Architecture	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03
Arch Width	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
Synthesizable	Yes	Yes	—	—	Yes	Yes
Hard Macro	—	—	Yes 1.1V, 5.8mm^2	Yes 1.1V, 7.0mm^2	Yes 1.1V, 6.0mm^2	Yes 1.2V, 2.17mm^2
Pipeline Depth	7 stages	7 stages	7 stages	7 stages	7 stages	5 stages
Instr Issue	In order 1-way	Out of order 2-way	Out of order 2-way	Out of order 2-way	Out of order 2-way	In order 1-way
Branch Predict	Dynamic	Dynamic	Dynamic	Dynamic	Dynamic	Dynamic
L1 Cache	Unified Up to 32K	I + D 16–32K each	I + D 32K each	I + D 32K each	I + D 0–32K each	I + D 16K each
16-Bit Instr	VLE	—	—	—	—	—
SIMD / MAC Instr	SIMD / MAC	MAC	MAC	MAC	MAC	MAC
Bus Interface	AMBA 2.0v6	CoreConnect	CoreConnect	CoreConnect	CoreConnect	CoreConnect
FPU	Integrated 32 bits	Optional coprocessor	—	Integrated 32 / 64 bits	Optional coprocessor	Optional coprocessor
MMU + TLB	Yes	Yes	Yes	Yes	Yes	Yes
Timers	3 + watchdog	3 + watchdog	3 + watchdog	3 + watchdog	3 + watchdog	3 + watchdog
Debug Interface	Nexus 3	JTAG	JTAG	JTAG	JTAG	JTAG
Core Freq (Hard)	—	—	1.0GHz	1.0GHz	667MHz	658MHz
Core Freq (Soft)	250–350MHz	Up to 700MHz	—	—	300–350MHz	250–300MHz
Dhrystone (Hard)	—	—	2,000Dmips	2,000Dmips	1,334Dmips	1,000Dmips
Dhrystone (Soft)	375–525Dmips	1,400Dmips	—	—	600–700Dmips	380–456Dmips
Power (Hard)	—	—	0.53mW / MHz	n/a	200mW + 0.76mW / MHz	0.145mW / MHz
Power (Soft)	0.64mW / MHz	n/a	—	—	n/a	0.25–0.6mW / MHz
Core Size (Type)	3.8mm^2 (soft)	n/a	5.8mm^2 (hard)	7.0mm^2 (hard)	6.0mm^2 (hard)	2.17mm^2 (hard)
Introduction	2004	2006	2006	2006	1999	1998

Table 2. All processors in this table are 32-bit Power Architecture cores licensed by Freescale or IBM. This table lists only Freescale's highest-performance licensable Power core, the e200z6; see Table 1 for other e200 variants. In most respects, the e200z6 resembles IBM's Power 405. Both are uniscalar machines with in-order instruction execution and 32K of cache. Freescale's Signal Processing Engine (SPE) and Variable-Length Encoding (VLE) are clear advantages, and some developers will prefer the e200's AMBA bus over IBM's CoreConnect. IBM's other Power cores are out-of-order superscalar processors with greater raw throughput, but Freescale's SPE extensions could offset that advantage in some critical code paths. All speed, area, and power numbers in this table are vendor estimates and assume fabrication in 90nm CMOS. (n/a: data not available)

Freescale Outsources Licensing to IPextreme

For more than 10 years, companies like ARM have built their whole business on licensing intellectual property (IP). But Freescale is a traditional semiconductor company—a Motorola spinoff—that owns fabs and sells chips. For Freescale, licensing processor-IP cores to outside chip developers is something new. To hit the ground running, Freescale is outsourcing the logistics of IP licensing to IPextreme, a young company specializing in this business.

Founded in January 2004, with headquarters in Silicon Valley, IPextreme is an independent licensing agent. Its sole business is licensing other companies' IP to chip developers. IPextreme has no processor or peripheral IP of its own. Instead, the company acts as a middleman, handling the chores of licensing from soup to nuts. On behalf of its clients, such as Freescale, IPextreme is empowered to negotiate IP licenses with customers, package the IP for delivery, and provide follow-up technical support. IPextreme even tracks production of the resulting chips and collects the royalties.

In other words, IPextreme relieves its clients of the day-to-day drudgery of licensing. In return, the company shares the revenues, including the upfront license fees and chip royalties. It appears to be a good business. IPextreme already handles ColdFire licensing for Freescale, and other clients include Cypress, Infineon, National Semiconductor, and NXP (formerly Philips Semiconductors)—not a bad record for a three-year-old company. Like Freescale, IPextreme is a member of the Power.org consortium.

IPextreme isn't merely a middleman for offloading bureaucratic chores. In addition to acting as a licensing agent, the company provides other services. For instance, the Freescale arrangement erects a firewall of sorts between Freescale and its licensees. A wall is desirable, because some licensees may use Freescale's Power e200 core to make chips that compete with Freescale's own standard products. IPextreme says it can license the e200 to almost anyone, although Freescale has some "carve-out" restrictions to protect the IP from the prying eyes of direct competitors and potential thieves. The same firewall protects the licensees' own proprietary IP from Freescale's eyes.

Another service IPextreme provides is delivering the IP in usable form. IPextreme has created its own IP-packaging and configuration software called XPack. XPack presents developers with a graphical user interface to configure the IP and prepare it for use with electronic design automation (EDA) tools. IPextreme's packaging is EDA-neutral, so developers can use the tools of their choice, such as those from Cadence or Synopsys. (IPextreme CEO Warren Savage came from Synopsys.) XPack even generates synthesis scripts and test benches.

An additional service that IPextreme offers is IP aggregation. Because IPextreme is a licensing agent for several companies, it can package IP from multiple sources to suit a licensee's development project—often at a discount price that's cheaper than licensing the same IP separately. However, IPextreme isn't a design house, so licensees needing help beyond technical support must look elsewhere for those services.

winning CPU sockets in all three next-generation videogame consoles: Microsoft's Xbox360, Nintendo's Wii, and Sony's PlayStation 3. In some cases, those design wins came at the expense of MIPS, whose cores occupied sockets in previous-generation game consoles. But those are IBM's wins, not Freescale's, and the CPUs are full-custom designs, not SoCs built on licensable cores. IBM and Freescale need to translate that street cred into high-volume wins for their processor IP.

ARC and Tensilica license a wide variety of low-power processor cores and take a different approach to high performance. Their cores are highly configurable, allowing developers to customize the architecture for specific applications. (Some MIPS cores are configurable, too.) EEMBC benchmarks show that custom instructions can dramatically boost the performance of critical routines without commensurate increases in clock frequency and power. (See *MPR 2/18/03-06*, "Soft Cores Gain Ground.")

In addition to having more experience with processor-IP licensing than Freescale does, ARC, ARM, MIPS, and Tensilica focus exclusively on IP. Freescale is a traditional semiconductor company whose primary business is making chips for sale as standard products. IP companies don't worry about licensing cores to companies that might undercut another line of business. Indeed, they have no other lines of business to fall back on, so licensing is their lifeblood. On the other hand, Freescale's history as a traditional semiconductor vendor isn't necessarily detrimental. Freescale eats its own dog food, so to speak, by making standard parts and platform-level products with its own processor cores. ARC, ARM, MIPS, and Tensilica don't make chips or platforms and are often a step removed from the customers making the end products.

Although the pure-play IP companies are much smaller than Freescale, they have amassed hundreds of licensees and thousands of design wins, so they are formidable competitors. Developers weighing all these factors might want to decide first if the CPU architecture is the driving factor, then proceed from there. The Power Architecture certainly gives up nothing to other CPU architectures in capability, compatibility, and long-term stability.

Price & Availability

Freescale Semiconductor is licensing its Power e200z0, e200z1, e200z3, and e200z6 embedded-processor cores now. IPextreme is Freescale's exclusive licensing agent, with the authority to negotiate licenses with customers and the responsibility to provide technical support. Freescale and IPextreme are not publicly disclosing their license fees or chip royalties. For more information, visit *www.freescale.com/powerarchitecture* and *www.ip-extreme.com*.

Licensing Brings Power to the People

There are two ways to spread a CPU architecture far and wide. One is Intel's approach: make chips for sale as standard products that become the de facto standard in an immensely popular end-product category, such as PCs. The other is ARM's approach: license processor cores to all comers and let *them* make the chips for an immensely popular end-product category, such as cellphones. The second approach requires less effort for the owner of the CPU architecture, because IP licensing is what the military calls a force multiplier—it turns every licensee into a soldier.

The Power Architecture is popular already, but *MPR* believes it can do better. Although the number of Power chip suppliers is slowly increasing (with newcomers like AMCC and P.A. Semi joining the original tag team of IBM and Motorola/Freescale), licensing can greatly expand the market for Power-based processors. Some market niches are too small to merit standard products, so they need custom SoCs. Other opportunities look small at first and escape the grasp of big companies like Freescale and IBM. (There's no technical reason why Power processors couldn't have filled ARM's role in billions of cellphones and iPods.) The Power Architecture is certainly versatile enough to span the range of the processor market, from low-power embedded systems to high-performance servers.

Perhaps the biggest challenge of processor-IP licensing is making money. ARM has been very profitable, thanks largely to the world's insatiable demand for cellphones. MIPS has been moderately profitable but is trying to resolve a stock-options problem that has prevented the company from stating its recent earnings. ARC has never made a profit but is nearly breaking even and could turn the corner soon. Tensilica is still a private company that doesn't publicly reveal its finances, but it seems to be surviving without frequent bailouts from investors, so it's probably not too different from ARC.

IBM appears satisfied with the progress of its Power Architecture licensing. IBM has been openly licensing Power cores for about four years now and recently introduced three new licensable cores, with hints of more to come. *MPR* believes the time is right for Freescale to enter this market. By proceeding carefully with a few Power e200 cores, Freescale can gauge the interest, solve any initial problems that arise, and decide whether a broader licensing strategy makes sense.