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MPR Innovation Award: Ambric

Ambric Fits New CPU Architecture to Parallel Programming Model

By Tom R. Halfhill {2/20/07-02}

Microprocessor Report is presenting an ***MPR* Analysts' Choice Award** in the Innovation category to Ambric, an Oregon-based fabless semiconductor company founded in 2003. Bucking the usual trend, Ambric designed a new microprocessor architecture by first creating an innovative programming model, then fashioning an architecture capable of efficiently executing it.

Most CPU architects start with the architecture, leaving the software-development tools almost as an afterthought. That's tolerable if the architecture is conventional. But if the new architecture is an exotic one intended for massive parallelism, the tools require more forethought. It's easier to slap down multiple processor cores on a chip than it is to write efficient parallel-processing code.

At Fall Microprocessor Forum in October 2006, Ambric introduced the Am2045 massively parallel processor. (See *MPR 10/10/06-01*, "Ambric's New Parallel Processor.") This 117-million-transistor chip is fabricated in a modest 0.13-micron CMOS process, but it crams 360 proprietary 32-bit RISC processors and 585KB of SRAM onto a single compact die. Maximum theoretical performance exceeds one trillion operations per second at 333MHz. The Am2045 is designed to replace high-end embedded processors, DSPs, and FPGAs in applications that require fast general-purpose integer and digital-signal processing.

More important than the chip is the programming model. Application programmers will write most of their code in Java, but the Am2045 isn't a Java chip. There's no Java virtual machine, bytecode interpreter, or just-in-time (JIT) compiler. There isn't even any bytecode. Instead, Ambric has adopted Java solely for its familiarity and object orientation. Ambric's software-development tools convert Java source code into proprietary machine language, then map the compiled objects onto the processor array.

Ambric is taking the right approach by starting with a relatively straightforward programming model and applying it to a flexible, powerful architecture. If Ambric's tools work as well as the company promises, they will advance the art of programming massively parallel arrays.

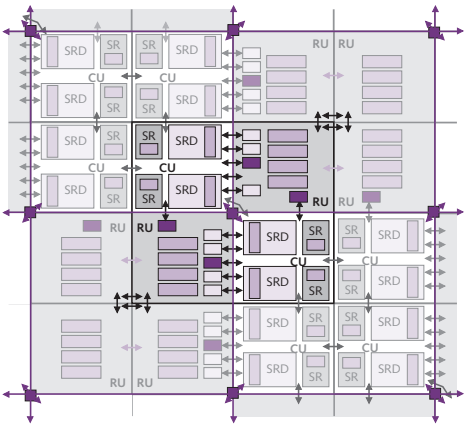

Figure 1. This partial Am2045 block diagram highlights a section of the chip that contains two processor-memory clusters, flipped to create two halves that mirror each other. The highlighted section has 16 of the chip's 360 proprietary 32-bit processor cores.