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TENSILICA UPGRADES XTENSA CORES

New Xtensa 7 and Xtensa LX2 Processors Get ECC and More

By Tom R. Halfhill {12/4/06-02}

Fending off ARM's latest punches, Tensilica is introducing two new versions of its 32-bit configurable-processor cores. The biggest improvements are error-correction codes (ECC) to protect caches and local memories, an optional memory-management unit (MMU) for both processors, and several new configuration options that can boost performance, save gates, and reduce power.

The enhanced processors are the Xtensa 7 and Xtensa LX2. Xtensa 7 is the latest incarnation of Tensilica's original configurable-processor family, which first appeared in 1999 and was last revised in 2005. (See the sidebar "Tensilica Introduces Xtensa 6 Processor Core" in *MPR 11/28/05-01*, "Tensilica Previews Video Engine.") The other new processor, the Xtensa LX2, is only the second member of Tensilica's newer Xtensa LX family, which made its debut in 2004. (See *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.") The base configurations of both processors are essentially the same, but Xtensa LX2 has more extension options than Xtensa 7 does.

With their latest improvements, the differences between Tensilica's two processor families continue to shrink. At first, the signature difference was compatibility with Tensilica's highly automated Xtensa PRocessor Extension Synthesis (XPRES) tools—Xtensa LX had it, Xtensa V didn't. (See *MPR 7/12/04-01*, "Tensilica's Automaton Arrives.") Xtensa 6 eliminated that difference when it, too, became compatible with XPRES. Another distinguishing feature between the two families was an optional MMU—Xtensa 6 had it, Xtensa LX didn't. Now the MMU is optional for both Xtensa 7 and Xtensa LX2. In addition, both cores have optional ECC and parity checking, entirely new features for Tensilica processors.

Nevertheless, some differences remain, as we will explain in detail below. In competitive terms, both Xtensa 7 and Xtensa LX2 are good power-performance alternatives to ARM7-, ARM9-, and ARM11-family processors, depending on their configurations and synthesis targets. Optional MMUs make them compatible with virtual-memory operating systems such as Linux, and their optional ECC matches a feature that ARM recently introduced with the Cortex-R4F. (See *MPR 10/30/06-01*, "ARM Thumbs a Ride.")

Both Xtensa 7 and Xtensa LX2 are available for licensing now. Like all Tensilica processors, they are 32-bit synthesizable cores that developers can extensively customize with Tensilica's proprietary configuration tools. These tools provide a graphical user interface that allows developers to modify the processors without hacking the hardware description language (HDL). The same tools automatically generate synthesis scripts, compilers, assemblers, debuggers, and simulators that are compatible with the customer's processor configuration.

ECC Counters ARM's Cortex-R4F

Tensilica's configurable processors already are extremely flexible, so the new features in Xtensa 7 and Xtensa LX2 merely enhance their capabilities. Overall, Tensilica has taken steps to reduce power consumption, add more configuration options, and allow developers to use Xtensa cores in mission-critical applications.

Optional ECC and parity checking are significant new features. Although developers could manually implement their own error-checking schemes with older Xtensa cores, Xtensa 7 and Xtensa LX2 are the first Tensilica processors to offer ECC and parity as standard options. By selecting a new

check box in the Xtensa configuration tool, developers can instantly add ECC or parity checking to the instruction cache, data cache, and local scratchpad memories. Protection against the rising probability of soft errors makes the new Xtensa processors more suitable for critical embedded applications, such as industrial and automotive controllers. It was ARM's quest for greater penetration in the automotive power-train market that led to the recent introduction of ECC in the Cortex-R4F.

ECC wasn't critical for chips fabricated in 90nm or larger processes, but developers targeting next-generation 65nm processes are increasingly asking for it. Smaller transistors are more vulnerable to cosmic rays and other sources of soft errors. With parity enabled, the processor throws an exception if it detects a single-bit error. With ECC, the processor can detect single- and double-bit errors and automatically correct single-bit errors.

Tensilica is taking a slightly different approach to ECC than ARM is. Tensilica's ECC is much finer grained, operating at the byte level. Each byte carries five bits of error coding. This stringent scheme catches more errors and preserves the ability of Xtensa processors to read and write byte-size data. But the trade-off is 63% overhead—five guard bits for each byte of data.

ARM considered that scheme for the Cortex-R4F but rejected it as inefficient. Instead, a synthesis option lets Cortex-R4F developers apply ECC to 32-bit words (22% overhead) or to 64-bit double words (12% overhead). This is perhaps the only example of greater configurability in an ARM processor than in a Tensilica processor. (Tensilica says future Xtensa processors may offer developers more control over ECC granularity.) ARM's trade-offs for requiring less overhead are weaker error protection and clumsier operations when writing smaller chunks of data. For instance, if the Cortex-R4F implements double-word ECC, the processor must perform a 64-bit read/modify/write operation to change an 8-, 16-, or 32-bit quantity. This multiple-step operation isn't atomic, so it's interruptible.

Ideally, ARM and Tensilica would allow developers to choose any degree of ECC granularity. The configuration tools or synthesis scripts should let developers apply ECC to individual bytes (five bits of overhead), half words (six bits of overhead), full 32-bit words (seven bits of overhead), or double words (eight bits of overhead). Then developers could make their own trade-offs, according to the needs of the application. Some critical industrial- or automotive-control signals need the strongest possible error protection. At the other extreme, audio/video datastreams may need no protection at all, because occasional bit errors aren't audible or visible.

More Flexibility for I/O Interfaces

Xtensa 7 and Xtensa LX2 offer several new options for configuring their various I/O interfaces. In general, these options allow developers to fine-tune the interfaces to optimize performance and save power. For instance, both processors now permit developers to independently choose the widths of the

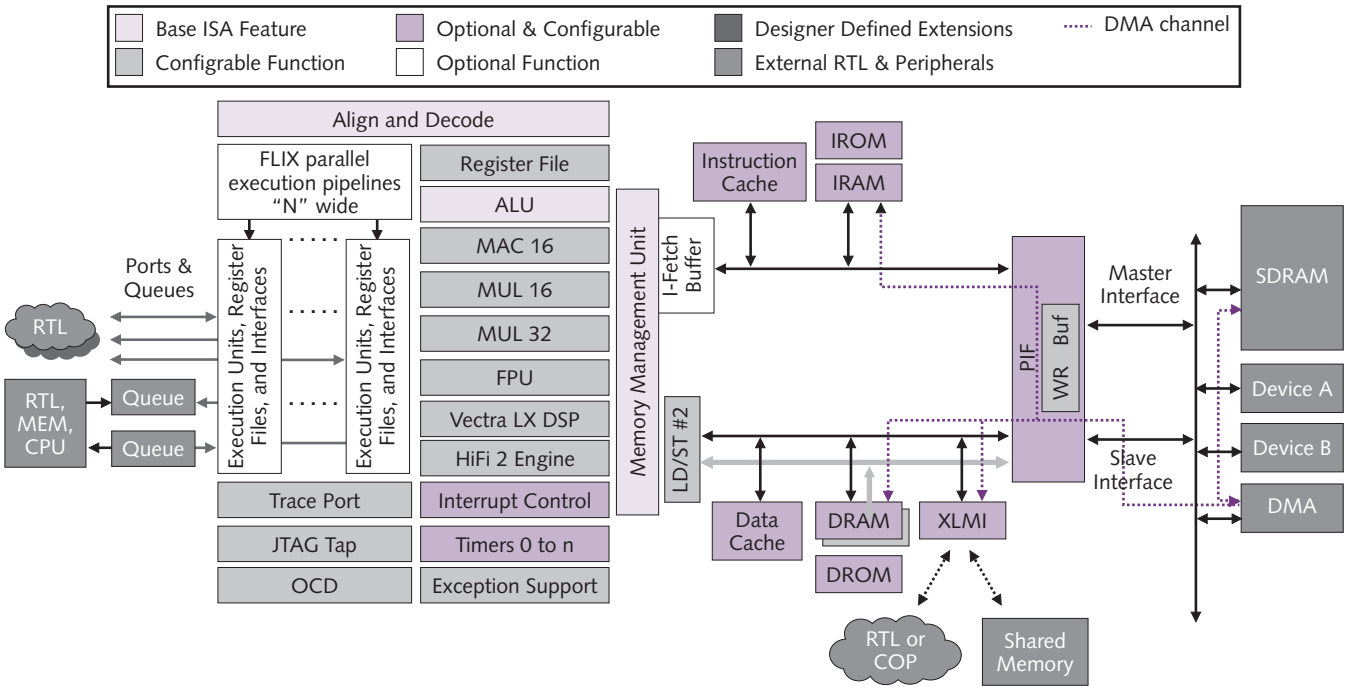

Figure 1. Xtensa LX2 block diagram. Enhanced I/O interface options give developers more control over performance and allow more-highly-optimized designs. Xtensa 7 has an almost identical microarchitecture, except that it lacks support for Vectra LX DSP extensions, HiFi 2 extensions, FLIX, and the special TIE (Tensilica Instruction Extension) ports and queues shown at the left.

main processor interface (PIF), local instruction-memory interface, and local data-memory interface. Before, developers could configure those interfaces for data widths of 32 bits, 64 bits, or 128 bits, but not independently of each other—all three interfaces had to be the same width. Developers can also configure the depth of the PIF buffer, from one entry to eight.

In addition, the new processors allow developers to make the instruction-fetch buffer up to 128 bits wide. Previously, the buffer could be either 32 or 64 bits wide. The 128-bit option allows the buffer to grab more instructions at a time. Note that the standard length for Xtensa instructions is 24 bits, not 32 bits as with most RISC architectures. Xtensa also has a subset of 16-bit instructions, similar to ARM's Thumb. Therefore, a 128-bit-wide instruction buffer can retrieve as many as eight 16-bit instructions per fetch. Of course, the processor can't execute that many instructions at once, so it caches the extra instructions and uses them in subsequent cycles, which saves power by reducing the number of memory accesses.

Wider memory interfaces and instruction buffers are especially useful if Xtensa LX2 developers implement Tensilica's optional Flexible-Length Instruction Xtensions (FLIX). FLIX is Tensilica's unique spin on VLIW, packing multiple operations into 32- or 64-bit instruction words. Operations that invoke custom logic can be as short as a single bit. With a 128-bit-wide instruction-memory interface and buffer, an Xtensa LX2 can fetch two or four FLIX words, each containing up to 15 operations, in a single clock cycle. (See *MPR 11/25/02-06*, "FLIX: The New Xtensa ISA Mix.") Figure 1 is a block diagram of Xtensa LX2.

To further improve efficiency, a new configuration option adds some logic to assist unaligned loads and stores in both Xtensa 7 and Xtensa LX2. Previously, Xtensa processors either assumed that reads or writes were properly aligned (relying on the software to manage alignment) or threw an exception if such an operation crossed a memory boundary. The new logic automatically detects misalignments and converts the operation into two reads or writes.

In addition, Xtensa 7 and Xtensa LX2 speculatively access memory less often than previous Xtensa processors do. In some circumstances, this modification could reduce performance by slightly increasing the latency of memory enables and accesses. However, Tensilica says the power reduction is worth the small sacrifice.

Obviously, these various I/O enhancements will improve throughput, but they can also save power by reducing memory accesses. Compared with earlier Xtensa processors, Xtensa 7 and Xtensa LX2 can reduce instruction-memory cycles by 75%, according to Tensilica. All together, the new I/O-interface options and other enhancements can reduce total power consumption by 15–30%. That's significant for processor cores that already consume very little power. In their base configurations, both processors consume only 0.046mW per megahertz, assuming power-optimized synthesis for a generic 90nm CMOS process (worst case).

Miscellaneous Improvements

New power-down modes in Xtensa 7 and Xtensa LX2 allow external sources to switch off the processor's trace-port control and debug logic, saving a little more power. It might seem that saving power on those ports wouldn't matter after a development project is finished, when the ports become redundant. However, some developers are using the debug ports for master/slave communications with other devices or to link two or more Xtensa processors together in a multicore design. (Quite a few Xtensa designs are multicore chips. The largest publicly disclosed example—a packet-processing ASIC for Cisco System routers—crams 196 Xtensa cores on a single die.)

The Xtensa LX2 has two optional improvements not available for Xtensa 7: "connection boxes" for dual load/store units, and "lookup ports" that supplement the standard I/O interfaces. Connection boxes are optional logic blocks that simplify the task of connecting two load/store units to separate data memories. Typically, a developer would use these boxes to provide independent interfaces to X and Y data memories for DSP extensions. This arrangement allows a DSP instruction to fetch two operands per clock cycle from conventional single-ported SRAMs.

Lookup ports are closely coupled I/O interfaces that developers can create using Tensilica Instruction Extension (TIE) language—the company's proprietary HDL, which resembles Verilog. These ports provide an alternative way to access local data without suffering the latency of conventional load/store instructions. In effect, the ports link the processor's instruction pipeline directly to an external data source, such as a lookup table, queue, or even an application-specific compute engine. Lookup ports are much like the TIE ports and queues that Tensilica introduced with Xtensa LX two years ago, but they are a little easier to implement for simple lookup functions. (See *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.")

When a custom-defined lookup-port instruction reaches the pipeline's execution stage, it can read or write data

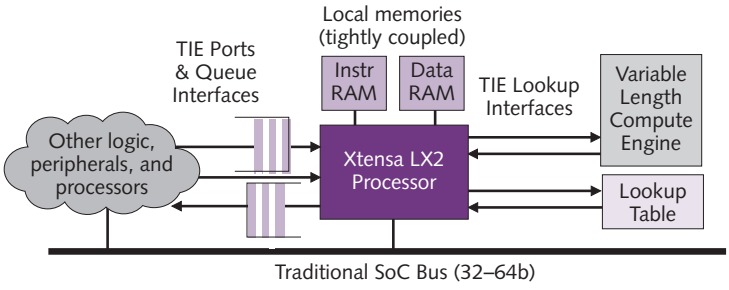

Figure 2. The Xtensa LX2 processor offers more I/O options than Xtensa 7 does. Of course, both cores support tightly coupled scratchpad memories, as well as a "traditional SoC bus" (Tensilica's term for an AMBA-compatible bus, which attaches to the main processor interface, or PIF). But Xtensa LX2 also supports special back-side interfaces called TIE ports and the new TIE lookup ports. Developers can add these I/O interfaces using TIE language, exercising great flexibility over the number and widths of the ports.

from or to the external data source. These special instructions differ from conventional load/store instructions in an important way—they bypass the normal instruction and data paths, including the register file and data cache. Developers can define the number of lookup ports (up to 1,024 ports per core) and their data widths (up to 1,024 bits per port). These ports should be extremely useful for operations requiring quick references to tables or other data sources. One example might be a lookup table for the tokens that compression algorithms use; another might be a network-address table. Figure 2 shows the full range of closely coupled I/O options for Xtensa LX2.

To assist developers writing custom extensions in TIE language, Tensilica has improved the file-management features of TIE development tools. Teams of programmers can now share TIE blocks more efficiently, and different companies can more easily share their TIE libraries. These features will be of particular interest to large development teams, independent design houses, and third-party IP providers.

Xtensa Architecture Gradually Matures

Table 1 summarizes the features of Tensilica's new Xtensa 7 and Xtensa LX2 processors, comparing them with the existing Xtensa 6 and Xtensa LX. Although the improvements are worthwhile, they are more incremental than dramatic. This isn't necessarily a bad thing. The Xtensa architecture has gradually reached a state of maturity since its debut in 1999, and Tensilica hasn't lost sight of its original goal of providing highly customizable embedded-processor cores that consume very little power. No doubt, Tensilica could go wild with superscalar pipelines and other advanced features, but that would undermine the primary purpose of these processors. Tensilica prefers to deliver high performance through developer-defined extensions and rich I/O resources.

The Dhrystone mips numbers in Table 1 are even more misleading than Dhrystone numbers usually are. They measure the basic throughput performance of these customizable processors in their minimal base configurations. Presumably, developers wouldn't bother licensing a customizable processor if they didn't intend to customize it. The real advantage of a customizable processor lies in defining application-specific extensions, which can boost performance dramatically. Depending on the application, improvements of one or two orders of magnitude are possible. Although Tensilica hasn't subjected its latest processors to EEMBC benchmarking, previous Xtensa processors have achieved superlative EEMBC scores. (See *MPR 9/16/02-01*, "Tensilica Xtensa V Hits 350MHz" and *MPR 4/9/01-01*, "Stretching Silicon to the Max.")

However, some developers don't want to customize the cores, so Tensilica offers its Diamond line of preconfigured processors. Diamond processors have Xtensa 6 or Xtensa LX cores, customized by Tensilica for various classes of embedded applications. We wouldn't be surprised if next year Tensilica introduces a revised line of Diamond processors updated with the new Xtensa 7 and Xtensa LX2 cores. (See *MPR 3/20/06-01*, "Tensilica's Preconfigured Cores.")

Feature	Tensilica Xtensa 7	Tensilica Xtensa 6	Tensilica Xtensa LX2	Tensilica Xtensa LX
Architecture Width	32 bits	32 bits	32 bits	32 bits
Uniscalar Pipeline	5 stages	5 stages	5 or 7 stages	5 or 7 stages
FPU	Optional	Optional	Optional	Optional
MAC (16-Bit)	Optional	Optional	Optional	Optional
Multiplier (16-Bit)	Optional	Optional	Optional	Optional
Multiplier (32-Bit)	Optional	Optional	Optional	Optional
Xtensa PIF	Optional	Optional	Optional	Optional
New PIF Config Options	Yes	—	Yes	—
Xtensa Local Memory I/F	Optional	Optional	Optional	Optional
MMU & TLB	Optional	Optional	Optional	—
ECC & Parity Checking	Optional	—	Optional	—
Vectra LX DSP Engine	—	—	Optional	Optional
HiFi 2 Engine	—	—	Optional	Optional
Flexible-Length Instr Extensions (FLIX)	—	—	Optional	Optional
Load/Store Units	1	1	1 or 2	1 or 2
Custom Ports & Queues	—	—	Optional	Optional
TIE Lookup Ports	—	—	Optional	—
Dual-RAM Interface Connection Box	—	—	Optional	—
Xtensa Dev Tools	V7	V6	V7	V6
XPRES Tools	Yes	Yes	Yes	Yes
Better TIE Management	Yes	—	Yes	—
Lower-Power Memory I/O Options	Yes	—	Yes	—
New Power-Down Modes	Yes	—	Yes	—
Size (Base Config)	20k gates	20k gates	20k gates	20k gates
Power (Base Config)*	0.046mW/MHz	0.046mW/MHz	0.046mW/MHz	0.046mW/MHz
Performance (Dhrystone 2.1)	1.28 Dmips/MHz	1.28 Dmips/MHz	1.52 Dmips/MHz	1.52 Dmips/MHz
Max Clock Speed*	350–400MHz	350–400MHz	350–400MHz	350–400MHz
Introduction	Dec-2006	2005	Dec-2006	2004

Table 1. This comparison of the new Xtensa 7, existing Xtensa 6, new Xtensa LX2, and existing Xtensa LX processors shows key differences in purple text. Over the past seven years, Tensilica has steadily refined the Xtensa architecture and introduced many new features without unduly bloating the sizes of these small cores. The main difference between the two processor families is that Xtensa LX2 offers more extension options and high-throughput features. *Assumes fabrication in a generic 90nm CMOS process, worst-case conditions.

Tensilica's latest enhancements will strengthen the position of Xtensa processors against competing licensable processor cores from ARC International, ARM, and MIPS Technologies. In particular, the optional I/O interfaces for Xtensa LX2 surpass anything available from ARC and MIPS—unless developers get their hands dirty and directly modify the HDL models of the processors. (ARC and MIPS provide customers with Verilog models of the cores and allow low-level modifications, whereas Tensilica allows customers to modify the core only through its proprietary configuration tools and TIE language. ARM permits customers to modify the Verilog models only in very limited ways, through synthesis scripts.)

Another distinguishing feature of Tensilica's new cores is the optional parity protection and ECC. ARM's Cortex-R4F is the only competition in that regard. Tensilica will enjoy a competitive advantage in mission-critical embedded applications until ARC and MIPS add error detection and correction to their processors. Of course, developers can implement their own error-correction schemes with any processor core, but having that feature as a check-box option in a graphical configuration tool is a real plus. However, *MPR* would like to see Tensilica provide developers with full control over ECC granularity. The only current option—byte-level protection—carries too much overhead for some applications.

Price & Availability

Tensilica's Xtensa 7 and Xtensa LX2 32-bit processor cores are available for licensing now. A single-project license for Xtensa 7 starts at $250,000. Tensilica hasn't publicly disclosed licensing fees for Xtensa LX2, but it's probably more expensive than the less-capable Xtensa 7 processor. Xtensa processors come with Tensilica's standard processor-configuration tools, which automatically generate a suite of software-development tools matched to the customer's processor configuration. Tensilica's more highly automated XPRES processor-generation tools are available at extra cost for both Xtensa 7 and Xtensa LX2. For more information, visit *www.tensilica.com*.

In sum, Tensilica has improved the Xtensa 7 and Xtensa LX2 processors in several ways that make sense and resist creeping featuritis. A big advantage of a configurable processor is that the vendor can offer a large number of optional features that customers can adopt or ignore, as they see fit. With Xtensa 7 and Xtensa LX2, Tensilica has expanded the capabilities of its Xtensa processors while maintaining their flexibility and power efficiency.