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POWER.ORG'S UNITED ROADMAP

Power Architecture Consortium Hints at Future Processors and Cores

By Tom R. Halfhill {11/27/06-02}

Until now, forecasting the future of the Power Architecture (formerly PowerPC) required assembling a mosaic of individual roadmaps from different companies—some of which didn't even disclose roadmaps. That situation changed a few weeks ago, when the Power.org consortium released its first microprocessor roadmap consolidating the future plans of member companies.

Of course, the roadmap isn't very detailed. To some degree, Power.org members compete with each other, as well as with companies promoting other CPU architectures, so specific product plans remain closely guarded secrets. However, the high-level roadmap serves three important purposes. First, it reinforces the message that the Power Architecture has a future, despite Apple's defection and stiff competition in all markets. Second, it shows that Power.org members are pushing the architecture forward as a team, even though the various processors on the roadmap are very much the fruit of independent efforts by their respective vendors. Third, it illustrates the architecture's breadth and scope while roughly sketching out the market territories claimed by each vendor.

Inadvertently, the roadmap also reveals markets where the Power Architecture competes weakly or not at all. But that's useful information, too—both for Power.org and for potential customers. In sum, the consolidated roadmap is a worthwhile appendix to the Power instruction-set architecture (ISA) 2.03 specification, which Power.org officially released at the same time and that *Microprocessor Report* covered in detail last summer. (See *MPR 8/21/06-01*, "The New Power Architecture.")

Beyond 2006: Not Necessarily 2007

Power.org's roadmap actually consists of six individual roadmaps subdivided by architecture widths and processor types. There are three 64-bit roadmaps and three 32-bit roadmaps, and each threesome includes separate roadmaps for processors, processor cores, and a miscellaneous type called "hybrid/accelerated architectures."

Seven Power.org members are represented: AMCC, Freescale Semiconductor, HCL Technologies, IBM, Rapport, Synopsys, and Xilinx. Conspicuously missing from the official roadmaps is P.A. Semi, a Power Architecture licensee that hasn't yet joined the consortium. P.A. Semi has a valuable architectural license, which permits the company to create its own unique core designs instead of using cores from ranking members IBM and Freescale. For the sake of completeness, *MPR* has taken the liberty of unofficially adding P.A. Semi's PWRficient processor to the 64-bit processors roadmap. (See *MPR 10/25/05-01*, "P.A. Semi: New Blood for Power.")

Figure 1 shows all three 64-bit roadmaps, which are more sparsely populated than the 32-bit roadmaps. At first glance, a few things leap out. To begin with, all the Power.org roadmaps terminate in a nether region labeled "Beyond 2006." Product roadmaps are necessarily ambiguous, but this ambiguity fairly rings of committee negotiation. We can imagine consortium members wrangling over that wording late into the night. In any case, Power.org confirms that "Beyond 2006" doesn't necessarily mean 2007, so don't attempt to divine future product introductions by reading the roadmaps too literally.

Another interesting feature of the 64-bit roadmaps is what they say about Freescale's future plans. In the "Beyond

2006" region is a processor labeled 87*xx*. According to Freescale's customary nomenclature, "8" indicates a highly integrated chip (think PowerQUICC) and "7" indicates the family to which the chip's Power core belongs. And sure enough, the 64-bit cores roadmap shows Freescale's Power e700, a likely candidate for next-generation PowerQUICC designs.

Freescale hasn't publicly disclosed much technical information about the e700 core, which the company created before joining Power.org earlier this year. (See *MPR 3/6/06-01*, "Freescale Strengthens Power.Org.") Although the e700 implements the old PowerPC Book E architecture, Power.org has absorbed Book E into Power ISA 2.03, so the 64-bit e700 complies with the latest specification. The same is true of Freescale's Power e200 and e500 32-bit cores.

Speculating About IBM's 64-Bit Future

IBM plans to introduce a next-generation Power Architecture core, too. The 64-bit cores roadmap shows an IBM color-coded "NextGen Core" in the mysterious "Beyond 2006" region. The roadmap doesn't explicitly distinguish between cores intended for embedded processors and cores destined for server processors, so it's possible that this next-generation 64-bit core is destined for IBM's POWER family. At last month's Fall Microprocessor Forum, IBM presented the POWER6, a new 64-bit multicore design. (See *MPR 10/30/06-02*, "POWER: The Sixth Generation.") Perhaps the next-generation 64-bit core is for POWER7.

However, *MPR* interprets the roadmap differently. We think IBM intends to use the next-generation 64-bit core in embedded processors and license it to third-party chip developers. Currently, all of IBM's licensable embedded-processor cores are 32-bit implementations of the Power Architecture. If our supposition is correct, IBM's future 64-bit core will compete with the licensable 64-bit embedded-processor cores from MIPS Technologies. Other leading vendors of licensable processor cores (including ARC International, ARM, and Tensilica) don't have 64-bit architectures. The MIPS64 cores aren't best sellers, but they extend the MIPS architecture into high-performance networking—a market IBM covets for the Power Architecture.

The third section of the Power.org 64-bit roadmap shows "hybrid/accelerated architectures," a catch-all category that currently includes only one microprocessor family, IBM's Cell. The only known implementation of that family—the Cell Broadband Engine—has a 64-bit Power processor core that serves as an on-chip controller for eight coprocessors called Synergistic Processing Elements. Cell BE is indeed hybrid and accelerated. (See *MPR 2/14/05-01*, "Cell Moves Into the Limelight.")

Although IBM created Cell BE primarily for the Sony PlayStation 3 videogame console, it's turning out to be a highly versatile processor that's finding its way into workstations, servers, supercomputers, medical imaging equipment, and other systems far removed from the entertainment market. Unfortunately, the Power.org roadmap reveals nothing about Cell's future except what we already know: it appears bright.

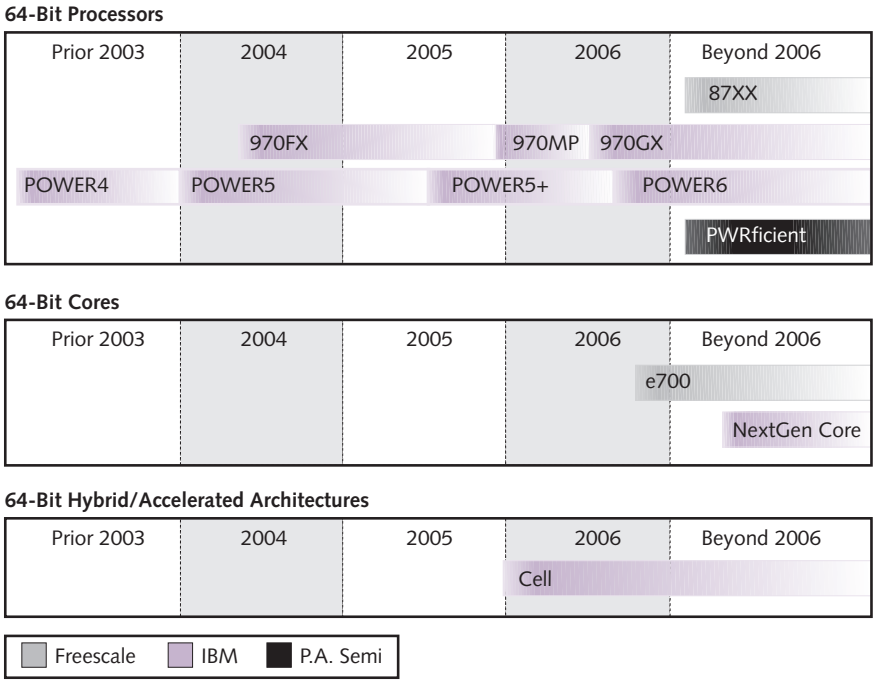

Figure 1. These three roadmaps plot the future of 64-bit Power Architecture microprocessors, processor cores, and hybrid architectures. To date, only two Power.org members are competing in the 64-bit weight class: IBM and Freescale. *MPR* has unofficially added P.A. Semi to this roadmap, even though that company hasn't yet joined the consortium.

32-Bit Roadmaps Show More Traffic

As expected, Power.org's 32-bit roadmaps are more crowded than the 64-bit roadmaps. In particular, the map of 32-bit processors indicates the deep penetration of the Power Architecture in the embedded market. AMCC, Freescale, and IBM offer numerous chips for networking, communications, network storage, automotives, industrial control, and general-purpose processing.

AMCC specializes in network and storage processors derived from the PowerPC 405 and PowerPC 440 chips the company acquired from IBM in 2004. (See the sidebar "AMCC Strikes a Big Deal for PowerPC" in *MPR 4/26/04-02*, "IBM Loosens Up CPU Licensing.") Freescale offers general-purpose processors like the swift MPC7448 but specializes in highly integrated PowerQUICC chips for communications and networking. (See *MPR 7/5/05-01*, "PowerPC Ain't Dead Yet," and *MPR 3/21/05-01*, "Freescale Quickens

PowerQUICC.") IBM offers high-performance general-purpose processors like the Power 750GX and recently announced 750CL. Figure 2 shows the Power.org roadmap for these and other 32-bit Power processors.

Unfortunately, this roadmap reveals nothing about future plans, other than to indicate that most of the existing product lines will remain available for at least another year (and probably much longer). However, it's easy to speculate.

MPR expects AMCC to continue rolling out Power 405/440 derivatives, such as the latest 440SPe (for storage) and 440EPx (a more general-purpose design). But AMCC has bigger things in mind. As an architectural licensee, AMCC is permitted to design new Power cores, and, last March, AMCC announced an alliance with Intrinsity to develop such a core. The new 32-bit core will appear in SoCs for control-plane processing and storage subsystems. It's an ambitious project that represents a significant investment for AMCC. Curiously, the core doesn't appear on any Power.org roadmaps—not even in the vague "Beyond 2006" regions. However, it's sure to be a multigigahertz design, because Intrinsity is using its unique Fast14 logic, which can reach clock rates in the 3.0GHz range. (See *MPR 1/10/05-02*, "Intrinsity Takes Its IP on the Road.")

Freescale is investing heavily in the Power Architecture, too. Freescale's PowerQUICC line is a hands-down winner, and the company introduces new PowerQUICC devices on an aggressive schedule. Recently, Freescale announced some PowerQUICC III parts with e500 cores running as fast as 1.33GHz. We expect PowerQUICC to continue breeding like rabbits.

Meanwhile, IBM keeps squeezing more life from its aging Power 750 family, which dates back to 1997. (See *MPR 7/21/03-04*, "IBM Proliferates 750 Family.") The broad trend in embedded systems is toward integrated processors, not general-purpose processors, so we won't be surprised if IBM revises its product line at some point.

Core Licensing Still Has Limitations

The other 32-bit roadmaps are much smaller than the 32-bit processor roadmap. Freescale, HCL Technologies, IBM, and Synopsys all show products on the cores roadmap, but these companies aren't quite equals. Only HCL (based in New Delhi), IBM, and Synopsys openly license Power Architecture cores to chip developers, and the HCL and Synopsys cores (synthesizable versions of the Power 405 and 440) are sublicensed from IBM.

HCL can sublicense implementation views of the Power cores to its customers, but Synopsys customers are limited to design views. Even when developers obtain a Power license directly from IBM, they have limited flexibility. They must manufacture their chips at IBM or at an IBM-approved foundry, such as Chartered Semiconductor or Samsung. Other popular foundries, such as TSMC and UMC, are off limits.

At present, Freescale doesn't openly license its Power Architecture processor cores, preferring to hold them close

For More Information

To view the latest versions of Power.org processor roadmaps, visit *www.power.org/resources/devcorner/-roadmap/*. The Power.org consortium's home page is at—where else?—*www.power.org*.

IBM's new Power 460S, Power 464-H90, and Power 464FP-H90 processor cores are available for licensing now. IBM doesn't publicly announce licensing fees or terms. For more information about these cores and the older Power 440 and Power 405 cores, visit *www.ibm.com/chips/techlib/techlib.nsf/products/PowerPC_Cores*.

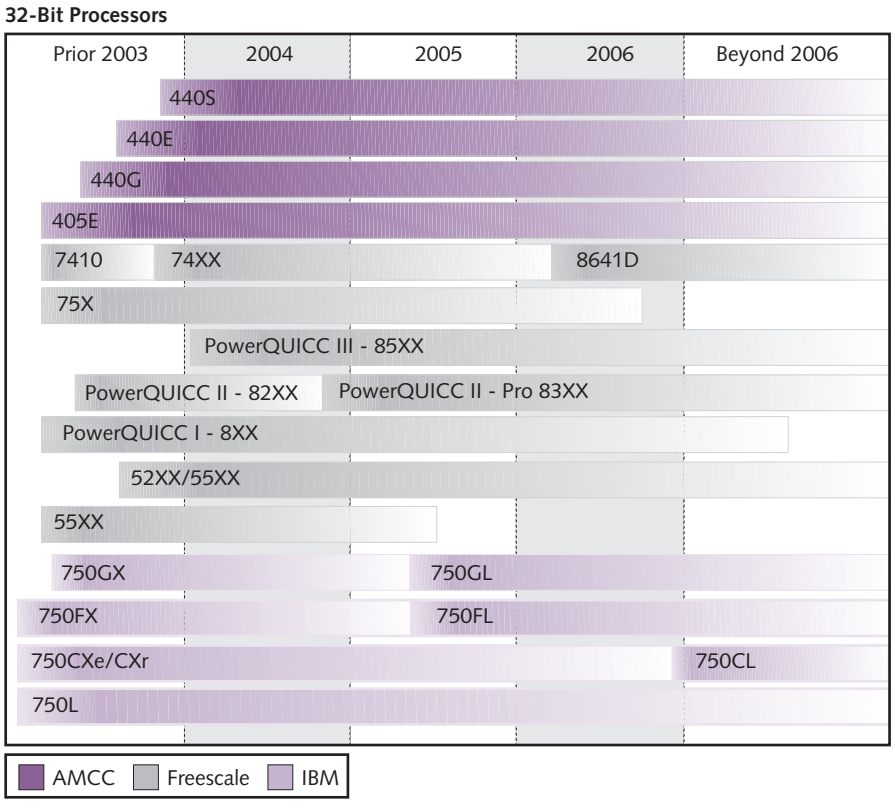

Figure 2. Power.org's roadmap for 32-bit chips shows where Power Architecture processors have the strongest presence in the marketplace. All these chips are high-performance standard parts suitable for a wide variety of embedded applications. Some are standalone general-purpose processors, while others are specialized storage processors or highly integrated communications chips.

IBM's New Licensable Power Cores

In October, IBM introduced its first completely new embedded-processor cores in seven years. All three are 32-bit licensable cores that implement the new Power ISA 2.03. (See *MPR 8/21/06-01*, "The New Power Architecture.") One processor is a synthesizable core, while the other two are hard macros.

The synthesizable core is the Power 460S. It has a seven-stage, out-of-order superscalar pipeline that can issue two integer instructions per clock cycle. Dynamic branch prediction helps reduce the branch penalty in this pipeline. During logic synthesis, developers can configure the size of the instruction and data caches (16KB or 32KB). Both nonblocking caches have parity protection, line locking, and writeback and write-through modes.

A memory-management unit (MMU) with a 64-entry translation lookaside buffer (TLB) allows the Power 460S to run sophisticated virtual-memory operating systems, such as Linux. Four timers are standard: a 64-bit time-base timer, a 32-bit decrementing timer, a fixed-interval timer, and a watchdog timer. The instruction set has 24 DSP operations, including a single-cycle 32-bit multiply-accumulate (MAC) instruction. IBM offers an optional FPU that attaches to a coprocessor interface. Optional peripherals include DDR1/DDR2 memory controllers, DMA controllers, PCI/PCI-X/PCIe controllers, interrupt controllers, and an L2 cache controller that supports coherency and snooping in multicore designs. All peripherals attach to the customer-configurable CoreConnect bus.

The other two new processors—the Power 464-H90 and Power 464FP-H90—are almost identical to the Power 460S and to each other. All share the same basic instruction set and seven-stage integer pipeline. However, the Power 464-H90 and Power 464FP-H90 are available only as prehardened cores for the standard 90nm processes at IBM, Chartered, and Samsung foundries.

The only significant microarchitectural difference between the Power 464-H90 and Power 464FP-H90 is that the latter has a double-precision FPU. Note that this FPU is fully integrated with the core, not attached to a coprocessor interface like the optional FPU for the Power 460S. The integrated FPU is almost identical to the "double hummer" FPU that IBM created for the BlueGene/L supercomputer processor. (See *MPR 10/11/04-01*, "IBM Makes Designer Genes.")

IBM sells the new processor cores to SoC developers as licensable intellectual property (IP). However, IBM offers less flexibility than do other processor-IP vendors, such as ARC International, ARM, MIPS Technologies, and Tensilica. IBM licensees can manufacture their designs only at IBM, Chartered, and Samsung. Other processor-IP vendors allow

Feature	IBM Power 460S	IBM Power 464-H90	IBM Power 464FP-H90	IBM Power 440	IBM Power 405
Power ISA	ISA 2.03	ISA 2.03	ISA 2.03	PPC Book E	PPC Book 1
Arch Width	32 bits	32 bits	32 bits	32 bits	32 bits
Synthesizable	Yes	—	—	Yes	Yes
Hard Macro	—	Yes 1.1V, 5.8mm ^{2}	Yes 1.1V, 7.0mm ^{2}	Yes 1.1V, 6.0mm ^{2}	Yes 1.1V, 2.0mm ^{2}
Pipeline Depth	7 stages	7 stages	7 stages	7 stages	5 stages
Instr Issue	Out of order 2-way	Out of order 2-way	Out of order 2-way	Out of order 2-way	In order 1-way
Branch Predict	Dynamic	Dynamic	Dynamic	Dynamic	Dynamic
I-Cache	16K or 32K	32K	32K	32K	16K
D-Cache	16K or 32K	32K	32K	32K	16K
FPU	Optional coprocessor	—	Integrated 32/64 bits	Optional coprocessor	Optional coprocessor
MMU + TLB	Yes	Yes	Yes	Yes	Yes
Timers	3 + watchdog	3 + watchdog	3 + watchdog	3 + watchdog	3 + watchdog
Core Freq (Hard)	—	1.0GHz	1.0GHz	667MHz	400MHz
Core Freq (Soft)	Up to 700MHz	—	—	300–350MHz	250–300MHz
Dhrystone (Hard)	—	2,000Dmips	2,000Dmips	1,334Dmips	608Dmips
Dhrystone (Soft)	1,400Dmips	—	—	600–700Dmips	380–456Dmips
Power (Hard)	—	0.53mW/MHz	n/a	200mW + 0.76mW/MHz	0.19mW/MHz
Power (Soft)	n/a	—	—	n/a	0.25–0.06mW/MHz
Introduction	Oct 2006	Oct 2006	Oct 2006	1999	1998

IBM's new Power H460S processor is synthesizable, and the new Power 464-H90 and Power 464FP-H90 processors are prehardened macros. The existing Power 440 and Power 405 processors are available as both hard macros and soft cores. The three new processors have virtually identical microarchitectures, the main exception being an integrated FPU in the Power 464FP-H90. Notice that the FPU adds about 20% to the die area of the 464FP-H90 when compared with the 464-H90. All die area, clock frequency, and power consumption numbers in this table are IBM worst-case estimates that assume fabrication in IBM's 90nm copper process. (n/a: data not available)

POWER CORES *(Continued)*

licensees to manufacture their designs anywhere, including the industry's most popular independent foundries, TSMC and UMC. This limitation will most likely affect the price of the chips, not their performance. IBM's fabrication technology is among the best in the world, and IBM works with Chartered and Samsung to maintain the same high standards. The Power 460S soft core is certified for 130nm and 90nm fabrication processes, whereas the Power 464-H90 and 464FP-H90 are certified only for 90nm.

Our table compares the new Power H460S, 464-H90, and 464FP-H90 processors with two existing embedded-processor cores that IBM offers for licensing: the Power 440 and Power 405. These older cores date from the late 1990s and deliver less performance than the new cores do. (For background on the older cores, see *MPR 10/25/99-03*, "IBM PowerPC 440 Hits 1,000 MIPS," and *MPR 10/26/98-05*, "PowerPC Adopts Code Compression.")

Interestingly, the Power 405 is the only processor in this group with in-order execution. The additional complexity of out-of-order execution enlarges the other cores but improves their throughput—at least, according to the Dhrystone mips numbers that IBM has provided. In addition, the new processors can attain higher clock frequencies. Even when hardened versions of both cores are compared, the new Power 464-H90 can reach a higher clock speed (1.0GHz vs. 667MHz, worst case) in the same fabrication process (IBM's 90nm) and deliver 50% more Dmips (2,000 vs. 1,334) than the older Power 440 can.

IBM's new cores will compete with 32-bit embedded-processor cores licensed by ARC, ARM, MIPS, and Tensilica. Only ARM and MIPS offer superscalar processors in the same microarchitectural class as IBM's cores, although ARC and Tensilica processors can execute multiple instructions per clock cycle under some circumstances. However, the configurable processors from ARC, MIPS, and Tensilica allow developers to extensively customize the architecture for specific applications. This advantage can boost performance far beyond the additional throughput of dual-issue pipelines. Also, IBM's competitors have processors that consume less power than IBM's processors do.

We believe IBM's cores have four prime attractions. First, they implement the Power Architecture, which is important to some developers that have existing PowerPC software or an aversion to other CPU architectures. Second, IBM's Blue Logic IP library has a huge selection of preverified peripherals and controllers. Third, the Power 464-H90 and 464FP-H90 cores are prehardened for IBM's excellent 90nm fabrication process, eliminating the need for logic synthesis, logic-level verification, and fab characterization. (Almost all competing licensable processors are available only as soft cores.) Fourth, some customers simply prefer to deal with a big, reliable company like IBM—although this factor has become less important in recent years, now that smaller processor-IP vendors have a proven track record.

for internal chip development. Understandably, Freescale is reluctant to license its valuable cores to potential competitors. This dilemma—the same companies that own Power cores also make Power chips—keeps the Power Architecture from competing more fiercely with the licensable processor architectures from ARC, ARM, MIPS, and Tensilica. Those competitors have different business models centered on licensing their intellectual property (IP), not on making chips, so they don't fear creating new rivals. In addition, they allow their customers to use any foundry.

However, Freescale is not averse to making an exception and licensing its Power cores if the circumstances are just right. Those stars aligned earlier this year, when Freescale agreed to share IP with STMicroelectronics. Freescale is licensing its 32-bit Power e200 core to STMicro, and they will jointly design chips that each company will bring to market separately. *MPR* hopes this deal will open the door to a broader licensing strategy in the near future.

Figure 3 shows the Power.org 32-bit processor-cores roadmap. IBM recently introduced three new Power cores—the

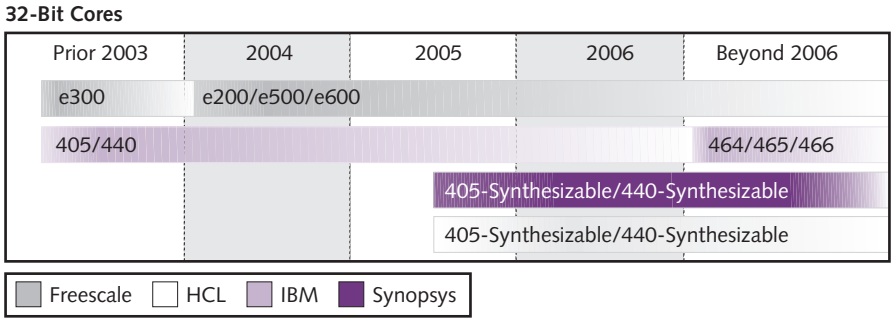

Figure 3. The Power.org roadmap for 32-bit processor cores has few surprises but does indicate that IBM intends to broaden its new Power 46x line. Synthesizable versions of the Power 405 and 440 cores remain available from IBM and, through sublicenses, from HCL Technologies and Synopsys.

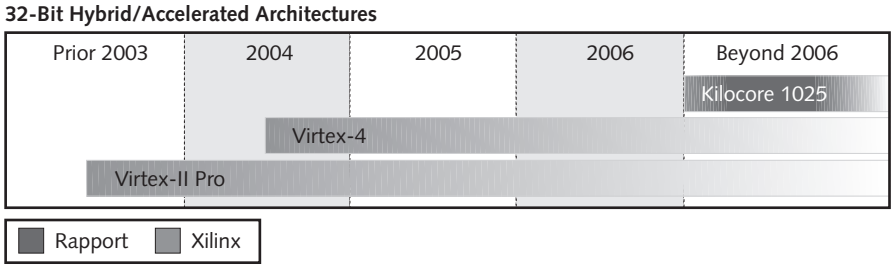

Figure 4. The Power.org roadmap for 32-bit hybrid/accelerated architectures currently has only one processor from Rapport—a massively parallel chip scheduled to debut in 2007. Actually, Rapport is sampling a smaller implementation of the architecture now. Xilinx makes some FPGAs with Power 405 processor cores.

460S, 464-H90, and 464FP-H90—and the roadmap indicates that additional cores in this series are coming in the future. (See the sidebar, "IBM's New Licensable Power Cores.")

Power.org's roadmap for 32-bit hybrid/accelerated processors is only a little more populated than the similar roadmap for 64-bit processors. The only two Power licensees on this map are Rapport Inc. and Xilinx. Rapport plans to introduce its Kilocore1025 device next year. For some reason, the roadmap omits the smaller Rapport KC256 chip, which is sampling now. Xilinx earns a place on the roadmap because some of its Virtex-4 and Virtex-II Pro FPGAs have integrated Power 405 hard cores. (See *MPR 11/5/01-03*, "FPGAs Catch Fire at MPF.") Figure 4 shows the 32-bit hybrid/accelerated roadmap.

Rapport announced its massively parallel architecture at Spring Processor Forum 2005. It uses a single Power core as a master controller for hundreds of tiny eight-bit processing elements, which aren't based on the Power Architecture. The Rapport KC256 chip has 256 processing elements; the Kilocore1025 will have a Power core plus 1,024 elements. These specialized chips are intended for media acceleration, communications, and security applications. They will compete with several other massively parallel processors, including those from Ambric, Connex Technology, Elixent (now owned by Matsushita), MathStar, and PicoChip. (For a roundup of this fast-growing field, see *MPR 10/10/06-01*, "Ambric's New Parallel Processor.")

What's Missing From the Roadmaps

Overall, the Power.org roadmaps deliver an important marketing message ("the Power Architecture is alive and thriving") and provide useful insight into the consortium members' future plans. The roadmaps show the architecture to be pervasive, versatile, and muscular.

The only hole—a big one—is the PC market. Apple's defection to the x86 relegates the Power Architecture to embedded systems and high-end servers. Of course, those markets account for about 98% of the volume in semiconductors (almost wholly embedded), which makes the PC-processor market seem unimportant. But PC processors reap most of the semiconductor revenue, which makes them lucrative products, especially if your company's name is Intel.

Unfortunately for Power.org and the Power Architecture, the battle for the PC market is lost. "PowerPC" has become simply "Power." In partial compensation, IBM won a clean sweep of Power-based designs in all three next-generation home videogame consoles: Microsoft's Xbox 360, Nintendo's Wii, and Sony's PlayStation 3. This demonstrates that there are still plenty of fresh opportunities for an architecture that has great breadth and a growing consortium of supporters.