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XILINX REVS UP MICROBLAZE

Licensable Soft-Processor Core for FPGAs Gets Faster and Smaller

By Tom R. Halfhill {11/13/06-01}

Small improvements add up. At last month's **Fall Microprocessor Forum**, Xilinx unveiled an enhanced version of its licensable 32-bit processor core for FPGAs. Optimized for synthesis in next-generation Virtex-5 programmable-logic devices, the new MicroBlaze v5.00 processor uses deeper pipelining and higher clock speeds to boost integer performance by as much as 25% and floating-point performance by as much as 50% over the existing MicroBlaze v4.00 core.

Ralph Wittig, director of engineering for the Xilinx Embedded Processing Division, delivered the MicroBlaze v5.00 presentation at MPF. Wittig began his presentation on what seemed like a tangent—gate-level differences between current-generation Virtex-4 and next-generation Virtex-5 devices. Was he introducing a processor or leading a tutorial about FPGAs? But the detour made sense as Wittig explained that a new six-input lookup table (LUT) in the Virtex-5 programmable-logic fabric helps improve the performance of MicroBlaze v5.00 while reducing the number of LUTs it requires. The enhanced processor core is faster *and* smaller.

Xilinx will manufacture Virtex-5 FPGAs in a new 65nm CMOS process at fabs owned by Toshiba and UMC, the company's foundry partners. (Today's Virtex-4 FPGAs are fabricated in a 90nm CMOS process.) Xilinx decided to take advantage of the smaller transistors by increasing the density of the LUTs, which are basically programmable logic gates. Virtex-4 LUTs have four inputs; Virtex-5 LUTs have six. This seemingly minor change is significant. It allows the Xilinx synthesis tools to squeeze the MicroBlaze v5.00 soft-processor core into significantly fewer LUTs, leaving more room for on-chip peripherals and custom logic. In addition, the denser programmable logic helps improve the processor's efficiency, while a deeper instruction pipeline allows slightly higher clock frequencies.

MicroBlaze v5.00 is available now as licensable soft intellectual property (IP). However, the Virtex-5 devices for which the new processor is optimized aren't in mass production yet. Xilinx began sampling the chips in May and plans to make production quantities available in 2007. As with current Virtex-4 devices, Xilinx will offer the next-generation FPGAs in various sizes, with optional DSP blocks, optional transceiver blocks, and optional hard-processor cores on chip. Until Virtex-5 becomes available, developers can synthesize MicroBlaze v5.00 in existing Xilinx FPGAs, though with some loss of performance.

Smaller Processor Aids Multicore Designs

It's unusual for a new processor core to be smaller than its predecessor. Actually, if MicroBlaze v5.00 were synthesized in conventional fixed logic instead of programmable logic, it would almost certainly be larger than MicroBlaze v4.00. Although Xilinx allows customers to implement MicroBlaze cores in fixed logic, the processors are designed and optimized for synthesis in Xilinx FPGAs. The apparent shrinkage from v4.00 to v5.00 is almost entirely due to the six-input LUTs in Virtex-5. Xilinx says the register file is six times denser and muxes are twice as dense.

Not every MicroBlaze customer will want to use Virtex-5 devices, which have up to 1.1 billion transistors and are the largest and most expensive FPGAs in the Xilinx

	Xilinx MicroBlaze v5.00 Virtex-5 (5VLX30-3)	Xilinx MicroBlaze v5.00 Virtex-4 (4VLX25-12)
IC Process	65nm	90nm
LUT Type	6 inputs	4 inputs
LUTs Available	207,360 LUTs	200,448 LUTs
BRAM Available	10.1KB (576 x 18Kb)	9.7KB (552 x 18Kb)
CPU Configuration	32-bit multiplier 8K I-cache 16K D-cache	32-bit multiplier 8K I-cache 16K D-cache
CPU Size	960 LUTs	1,700 LUTs
CPU Capacity (Max)	216 cores per chip	117 cores per chip
Core Freq (Max)	210MHz	160MHz
Integer Perf	1.15Dmips/MHz	1.15Dmips/MHz
Integer Perf (Max)	241Dmips	184Dmips

Table 1. Although MicroBlaze v5.00 is optimized for next-generation Virtex-5 devices and their new six-input LUTs, it remains compatible with existing Xilinx FPGAs, such as the high-end Virtex-4 family and lower-end Spartan 3E family, which have four-input LUTs. This table shows the results of synthesizing a typical MicroBlaze v5.00 configuration in Virtex-5 and Virtex-4. Note that the Virtex-5 implementation runs 31% faster yet requires 44% fewer LUTs.

catalog. No worries—MicroBlaze v5.00 works with any Xilinx FPGA sufficiently large to accommodate the core. Table 1 compares the results of synthesizing the new processor in both a Virtex-5 and a Virtex-4. Obviously, Virtex-5 has the performance edge, but Virtex-4 isn't too shabby, either.

By requiring fewer LUTs, MicroBlaze v5.00 fits into smaller FPGAs and leaves more of the chip's programmable logic available for other purposes. Typically, developers use the remaining LUTs to implement on-chip peripherals and application-specific logic. Developers can also use the extra room to create a multicore design. As Table 1 indicates, the largest Virtex-5 device that Xilinx has announced will have room for 216 MicroBlaze v5.00 cores, assuming a developer configures the processor as shown and has no other use for the chip's logic. Even if a developer targets the less optimal Virtex-4, there will be enough room for 117 processor cores.

Of course, it's highly unlikely that a real-world application will need so many processors at the expense of leaving no room for peripherals and custom logic. But the point is that MicroBlaze v5.00 is both smaller and faster when synthesized in a Virtex-5 device, and together they make a powerful combination for rapidly developing multicore designs. This marriage opens the door to new and creative solutions.

For instance, Teja Technologies is using MicroBlaze v4.00 processor cores as packet-processing macro blocks, dedicating one or more cores to each stage in the data-plane pipeline. To handle control-plane tasks, Teja is using a Xilinx Virtex-4 FX device with integrated PowerPC 405 cores—thus creating a heterogeneous multicore design that combines soft-core MicroBlaze processors with hard-core Power Architecture processors on a single chip. By adopting MicroBlaze v5.00 and future Virtex-5 FX devices, Teja could allow developers to build even larger multicore packet processors. (See *MPR 4/3/06-02*, "Teja's FPGA Play.")

MicroBlaze v5.00 Echoes v4.00

In most respects, MicroBlaze v5.00 is identical to MicroBlaze v4.00, which *Microprocessor Report* covered in depth after its introduction at Spring Processor Forum 2005. The biggest improvement in v4.00 was an optional single-precision FPU. (See *MPR 5/17/05-02*, "MicroBlaze Can Float.")

The new core announced at Fall MPF 2006 is a smaller step forward, but not because Xilinx couldn't do any better. As Wittig explained during his MPF presentation, the MicroBlaze processor is already near its ideal microarchitecture for the vast majority of Xilinx developers. Xilinx wants to keep the core small and power efficient, roughly equivalent to an ARM9-family processor. For now, at least, Wittig foresees no overpowering need for superscalar execution and other complexities that would significantly inflate the core's size and power consumption.

The most important enhancement in v5.00 is a deeper pipeline, which permits slightly higher clock frequencies and improves the efficiency of some operations. MicroBlaze v4.00 and earlier cores have a very short three-stage pipeline, much

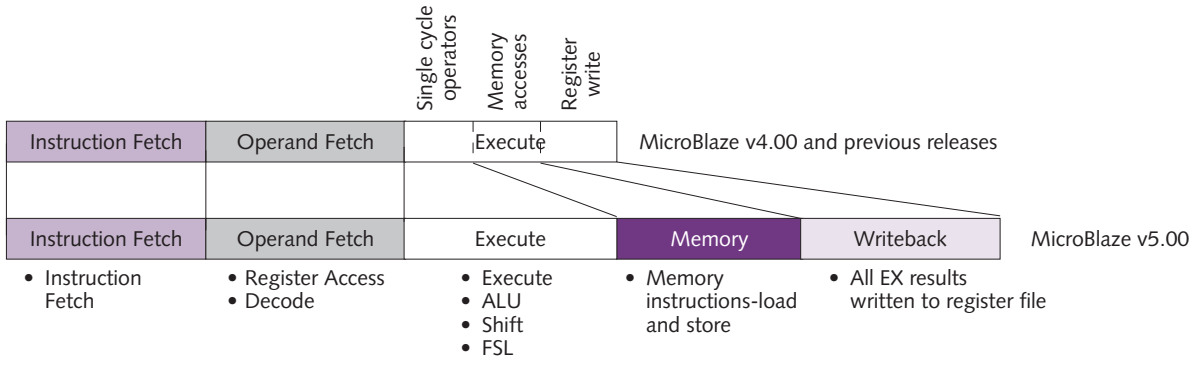

Figure 1. At top is the existing MicroBlaze v4.00 three-stage pipeline, and below is the new MicroBlaze v5.00 five-stage pipeline. By dividing the execution, load/store, and writeback functions into separate stages, the v5.00 pipeline relieves a bottleneck, permits higher clock speeds, and improves the throughput of multicycle instructions.

like the ARM7TDMI. MicroBlaze v5.00 lengthens the pipeline to five stages by dividing the last stage into three. In the old pipeline, stage 3 was a busy bee, responsible for executing instructions, accessing memory for data, and writing results back to registers. In the new pipeline, stage 3 executes ALU instructions, stage 4 executes load/store instructions, and stage 5 is writeback. Figure 1 compares the old and new pipelines.

In addition to enabling higher clock frequencies, the five-stage pipeline improves the efficiency of multicycle operations. In many cases, the v5.00 processor can execute multicycle operations at a single-cycle rate of throughput. This is useful for complex integer-type instructions, but it's especially helpful for floating-point instructions, which are multicycle by nature. Xilinx says v5.00 can execute up to 25% more integer instructions per cycle (IPC) and up to 50% more floating-point IPC than v4.00 does. Of course, the degree of improvement varies, depending on the code.

According to Xilinx, a finite impulse-response (FIR) filter using single-precision (32-bit) floating-point arithmetic runs 40% faster on v5.00 than on v4.00, even though their FPUs are functionally identical except for the pipelines. A 1,024-sample fast Fourier transform (FFT) runs 30% faster on v5.00. The Whetstone benchmark shows mixed results: overall: v5.00 is 50% faster than v4.00, although actual measured floating-point performance is only 7% better (13.56 megaflops vs. 12.72 megaflops). Under ideal conditions, the new processor's maximum theoretical floating-point throughput is 50 megaflops, compared with 33 megaflops for v4.00. That difference reflects the improved IPC as well as the new processor's slightly higher maximum clock frequency (220MHz versus 205MHz).

Price & Availability

Xilinx is licensing the MicroBlaze v5.00 processor core now. A royalty-free license is $495, including Embedded Development Kit 8.2i. For $995, developers can get the Virtex-5 ML501 Evaluation Platform, which includes a MicroBlaze v5.00 license; EDK 8.2i; a development board with a Virtex-5 LX50 FPGA; and additional documentation and materials. Xilinx plans to ship Virtex-5 devices in volume sometime in 2007. For more information, visit *http://www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=micro_blaze*

In general, the Xilinx benchmark results confirm what anyone would expect—a classic RISC five-stage pipeline tends to work more efficiently than a constricted three-stage pipeline. All ARM processors following the ARM7 generation have pipelines of five or more stages, as do the embedded-processor cores from Altera, ARC International, MIPS Technologies, and Tensilica.

Some of those competing processors also have something that MicroBlaze lacks: branch prediction. The ability to anticipate branches is scarcely necessary with a three-stage pipeline, because the branch-taken penalty is small. The penalty for branching starts to matter when pipelines grow to

Feature	Xilinx MicroBlaze v5.0	Xilinx MicroBlaze v4.0	Altera Nios II/f	Altera Nios II/s	Altera Nios II/e
Architecture	MicroBlaze	MicroBlaze	Nios II	Nios II	Nios II
Primary FPGA Targets	Virtex-5	Virtex-4 Spartan-3E	Stratix, Cyclone, HardCopy	Stratix, Cyclone, HardCopy	Stratix, Cyclone, HardCopy
Configurable ISA	—	—	Yes	Yes	Yes
Pipeline Depth	5 stages	3 stages	6 stages	5 stages	1 stage*
I-Cache	0–64K	0–64K	0–64K	0–64K	—
D-Cache	0–64K	0–64K	0–64K	0–64K	—
Local Memory	0 or 2 256K each	0 or 2 128K each	0–8 Configurable	0–4 Configurable	—
32-Bit Multiplier	Optional	Optional	Optional	Optional	—
32-Bit Divider	Optional	Optional	Optional	Optional	—
Barrel Shifter	Optional	Optional	Optional	Optional	—
FPU	Optional 32 bits	Optional 32 bits	Optional 32 bits	Optional 32 bits	Optional 32 bits
Branch Predict	—	—	Dynamic	Static	—
Privilege Levels	1	1	2	2	2
Core Freq (Max)	220MHz †	205MHz ‡	205MHz	165MHz	200MHz
Int. Perf (Max)	240Dmips	166Dmips	225Dmips	127Dmips	31Dmips
FP Perf (Max)	50MFLOPS	33MFLOPS	n/a	n/a	n/a
Logic Cells	960–1,700	950–2,400	1,800	1,150	600
Introduction	Oct 2006	May 2005	2004	2004	2004

Table 2. All the processors in this table are 32-bit embedded-processor cores designed for synthesis in programmable-logic devices from their respective vendors. Purple text highlights key differences between the new Xilinx MicroBlaze v5.00 processor and its immediate predecessor. Altera's Nios II processor is available in three basic configurations that developers can customize. *Nios II/e has a six-stage pipeline, but it works like a one-stage pipe. n/a: data not available.

five or more stages, because the processor wastes more clock cycles when it flushes the pipeline of instructions behind the branch. That's the reason Xilinx rival Altera added branch prediction to some versions of Nios II, a 32-bit soft-core processor that competes with MicroBlaze. A five-stage pipe is a borderline case, but if Xilinx adds any more stages to future versions of MicroBlaze, branch prediction will become a necessary feature.

Denser Logic Allows More Local Memory

A smaller improvement in MicroBlaze v5.00 is the option to integrate more local memory with the core: two 256KB blocks, instead of two 128KB blocks in v4.00. These scratchpad memories are in addition to the optional instruction and data caches, which can be as large as 64KB each (unchanged from v4.00). Denser 65nm logic in Virtex-5 makes the larger scratchpad memories possible. If the new core is synthesized in a lesser device, such as a Virtex-4, the scratchpads are limited to 128KB each, as before.

Although the deeper v5.00 pipeline improves execution efficiency and permits higher clock speeds, the frequency boost is disappointing. Ordinarily, we would expect that moving from 90nm to 65nm technology would allow the processor's frequency to rise commensurately with the programmable fabric's frequency, which is 30% faster in Virtex-5 than in Virtex-4. Instead, the actual increase in maximum clock frequency of v5.00 over v4.00 is only 7.3% (220MHz versus 205MHz). This small increase may reflect an inherent limitation of soft processor cores synthesized in programmable logic instead of in fixed logic. In any case, if future transitions to smaller geometries yield equally poor frequency gains, Xilinx may have no alternative but to increase the complexity of the MicroBlaze core in order to squeeze out more performance.

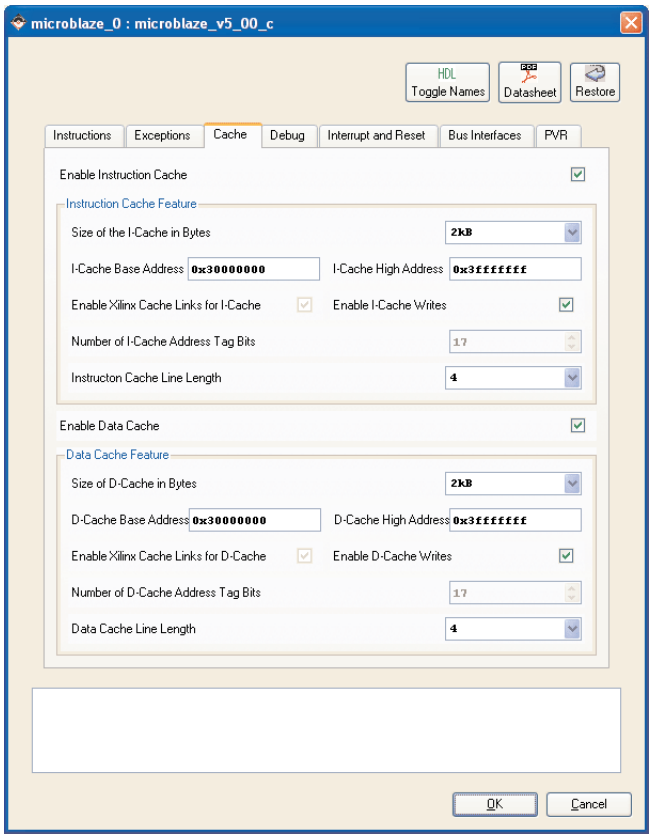

Figure 2. The Xilinx Embedded Development Kit includes a processor-configuration tool that lets developers customize a MicroBlaze processor core without getting their hands dirty in Verilog. The point-and-click user interface resembles the graphical development tools from configurable-processor vendors. On this screen, a developer can add instruction and data caches and tweak their features.

Xilinx says that in real-world applications, the clock rate of the MicroBlaze processor is less important than the performance of the peripherals and custom logic surrounding it. That's a good argument. Presumably, the flexibility of programmable logic is what motivates a developer to choose an FPGA in the first place. Typically, developers use the fabric to implement application-specific algorithms and I/O transceivers, using the MicroBlaze core as a microcontroller. The real intelligence and performance lies in the surrounding logic.

When particular logic blocks become popular and are fairly general-purpose in nature, Xilinx often introduces FPGAs that harden those blocks and integrate them with the fabric, greatly improving performance. Ethernet is a good example. Originally implemented solely in programmable logic, Ethernet controllers are now built into some FPGAs as a standard feature. Indeed, Xilinx offers Ethernet in multiple flavors. The smallest version is Ethernet Lite, a simple 10–100Mb/s controller delivered as soft IP. A slightly larger 10–100Mb/s controller adds DMA. The next-higher model adds a data realignment engine and checksum-offloading hardware. But the top-end controller supports Gigabit Ethernet and is an optional hard block on chip. In fact, Virtex-5 is the first FPGA to offer hardened tri-mode Ethernet (10/100/1,000Mb/s) and PCI Express controllers on chip.

Other FPGA vendors are pursuing similar strategies. The biggest Xilinx rival by far is Altera, whose Nios II processors are designed for synthesis in Altera FPGAs and compete head-to-head with MicroBlaze. The most notable difference between these processors is that Nios II allows developers to customize the architecture by adding as many as 256 application-specific instructions. Although Nios II isn't quite as customizable as ARC and Tensilica processors are, the ability to define custom instructions can significantly boost performance. (See *MPR 6/28/04-02*, "Altera's New CPU for FPGAs.") Table 2 summarizes the features of MicroBlaze and three variations of Nios II.

MicroBlaze is customizable, too, though at the function-block level, not the instruction level. Optional synthesizable blocks include the FPU, 32-bit multiplier, 32-bit divider, barrel shifter, caches, and I/O interfaces for scratchpad memories. These options allow developers to tailor MicroBlaze for their needs and will greatly affect the core's size and performance. Roughly speaking, the processor doubles

in size when a developer adds all the options. Floating-point performance is particularly variable, because without the optional FPU, the processor must emulate floating-point operations in software. According to Xilinx benchmarks, the difference can be as small as 3× for JPEG compression/decompression or as great as 42× when executing an FIR filter.

Improved Configuration Tools

Xilinx is delivering MicroBlaze v5.00 with a new version of the company's Embedded Development Kit (EDK). EDK 8.2i has an improved processor-configuration tool that resembles the more powerful tools from ARC, MIPS, and Tensilica. It allows MicroBlaze developers to rapidly configure and synthesize the processor with optional function blocks and other features. Figure 2 shows a typical screen from the new tool.

The Xilinx EDK is a complete hardware and software development system, including a GNU C/C++ compiler, software libraries, debugger, peripheral soft-IP, and board-support packages. The configuration tool automatically generates the appropriate board-support package and even defaults to the older MicroBlaze v4.00 core if the developer chooses to target a smaller Spartan FPGA instead of the larger Virtex-family devices. (MicroBlaze v5.00 doesn't replace earlier versions of the core—all four previous MicroBlaze cores are still available.)

What's most important is that the price hasn't changed. Developers can still buy a MicroBlaze license for the ridiculously low price of $495, which includes EDK 8.2i. That's a tremendous bargain compared with the processor cores from ARC, ARM, MIPS, and Tensilica. Their licenses cost hundreds of thousands to millions of dollars in upfront fees, not including chip royalties. The MicroBlaze license is royalty free.

For Xilinx, MicroBlaze is a loss leader—a way to sell more FPGAs. Given a price difference of three orders of magnitude, it's easy to overlook any shortcomings in the processor. As MicroBlaze (and Nios) continue to improve, and the cost of designing processors in fixed logic continues to rise, soft processors in programmable logic are looking more and more attractive.