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MICROPROCESSOR REPORT

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PREVIEW: FALL MICROPROCESSOR FORUM

Advances in Power Efficiency Is Theme of 18th Annual Fall Conference

By Tom R. Halfhill {8/28/06-01}

Engineers everywhere are tackling one of the greatest engineering challenges of the early 21st century: pushing microprocessor performance against the physical limits of power and heat. If they fail, the party is over. The "party," of course, is the long run of smaller-better-faster semiconductors spurred by Moore's law. Yes, exotic new technologies are glimmering on the horizon. But no one is certain how practical they will be. For at least the next decade, the industry is stuck with conventional silicon and process scaling. Make do or drop out.

Hence, our theme at In-Stat's **Fall Microprocessor Forum**: Advances in Power Efficiency—Addressing the Global Challenge. All developers face the same problems, whether their design uses a tiny automotive microcontroller or a mighty supercomputer processor. Surprisingly, the solutions are largely the same, too, across the design spectrum. The power-efficiency challenge is equally relevant to processor architects, SoC developers, system designers, programmers, and project managers.

Fall MPF will be held on October 9–11 at the Doubletree Hotel in San Jose, California. It will be our 18th annual fall conference, and it also marks In-Stat's 25th anniversary as a leading industry-analyst firm. To celebrate, we are reviving the famous MPF chip portfolio (every paid conference attendee gets a notebook with real microprocessor chips embedded in the cover), and we have arranged a stellar lineup of presenters.

As always, the forum begins with an all-day seminar. This year's seminar, on Monday, October 9, is "Maximum Performance, Minimum Power" by Max Baron, a *Microprocessor Report* principal analyst. It's a significant update of Baron's previous power-efficiency seminar, with new technical tutorials by AMD, Cadence, CoWare, Nextreme Thermal Solutions, and Texas Instruments.

The two-day conference portion of MPF is on Tuesday and Wednesday, October 10 and 11. It will feature no fewer than *four* keynotes by ARM, Cadence, Intel, and Microsoft. The companies and organizations making technical presentations include Ambric, Analog Devices, Boston Circuits, Cavium Networks, Ceva, Emulex, Eutecus, Freescale Semiconductor, Fujitsu, IBM, Imagination Technologies, Taiwan's

The theme of this year's Fall Microprocessor Forum is "Advances in Power Efficiency—Addressing the Global Challenge." More than 20 companies and organizations will give keynote talks and technical presentations. (Photo: MPR)

Industrial Technology Research Institute (ITRI), LSI Logic, Optosecurity, Renesas Technology, Sun Microsystems, Texas Instruments, and Xilinx.

Another customary event at MPF is the Tuesday night expo and party. This year's exhibitors include ARC International, ARM, Ceva, CodePlay, CoWare, Green Hills Software, IntellaSys, Obsidian, OCP, Silicon Hive, Tensilica, and Vast. Forum sponsors are IBM, InsideChips.com, Sun, and VIA. Separate or combined admissions are available for the one-day seminar, two-day conference, and Tuesday night expo and party. To register online, visit *www.in-stat.com/FallMPF/06/*.

Monday: Power-Efficiency Seminar

Fall MPF begins on Monday, October 9, with Max Baron's all-day seminar, "Maximum Performance, Minimum Power." For different reasons, two groups of designers are employing new techniques to obtain the best performance with the lowest power. Designers of mobile systems must increase performance at a faster pace than the relatively slow advance of battery technology. And designers of all types of systems must face the challenge of controlling device temperatures.

Baron's seminar will address the problems of performance, power consumption, and heat dissipation in both mobile and fixed systems. The seminar will examine these different types of designs, analyze the technology common to both, and explain the differences imposed by specific applications.

In-Stat will provide power outlets for notebook computers and a wireless network with access to forum presentations. Presentations will also be available on USB flash drives. (Photo: MPR)

Part 1 of the seminar is an overview of the ways SoC and big-iron processor vendors use architecture, microarchitecture, software, and power management to attain high performance while achieving the best combination of power consumption, integration, and flexibility. Following the overview, **AMD**, **Cadence**, **CoWare**, **Nextreme Thermal Solutions**, and **Texas Instruments** will present technical tutorials focused on design tools, homogenous multicore processors, systems using heterogeneous architectures based on accelerators, nanoengineered cooling of hot spots, and implementation aspects of embedded systems and desktop systems. The seminar will conclude with an analysis of several processor cores, chips, and SoCs.

Admission to the Monday seminar is separate from admission to the conference portion of Fall MPF. Package deals and group discounts are available. For more information or to register online, visit *www.in-stat.com/FallMPF/06/seminar.htm*.

Tuesday Morning: Server Processors

The conference portion of Fall MPF gets under way on Tuesday, October 10, with an opening keynote by Dr. Dileep Bhandarkar, architect-at-large in the Digital Enterprise Group at **Intel**. His talk is entitled "Energy-Efficient Performance: The Next Frontier." Bhandarkar will sketch a brief history of PC processors leading up to the latest Intel Core Microarchitecture, which has new power-management features. He will discuss some of the challenges to delivering energy-efficient performance and some techniques that Intel and other companies are exploring.

Following Intel's keynote is the first conference session: "New Server Architectures." This session has four presentations from Fujitsu, IBM, Sun, and Emulex.

Fujitsu starts the session with a presentation entitled "Fujitsu SPARC64 VI: A State-of-the-Art Dual-Core Processor" by Aiichiro Inoue, chief scientist of Fujitsu's Server Systems Group. This will be a detailed update on a powerful server processor that Fujitsu announced at our forum in 2004. (See *MPR 11/14/05-02*, "SPARC's Still Going Strong.")

IBM follows with "Power6: IBM's Next-Generation Microprocessor" by Dr. Brad McCredie, IBM Fellow and Power6 chief engineer. At the International Solid-State Circuits Conference (ISSCC) earlier this year, IBM announced that the new Power6 will ship at clock speeds between 4.0GHz and 5.0GHz. (See *MPR 2/27/06-02*, "ISSCC '06: The Large and the Fast.") McCredie's presentation at MPF will reveal more about this blazing processor and the 65nm silicon-on-insulator (SOI) fabrication process in which IBM will manufacture it.

Sun is next with "Niagara2: A Highly Threaded Server on a Chip" by Robert Golla, lead designer. Today, Sun's Niagara server processor can simultaneously run 32 threads of execution. (See *MPR 1/3/06-01*, "Sun's Niagara Begins CMT Flood.") The Niagara2 will run 64 threads, and it will support a coherent dual-CPU system capable of running 128

threads. Sun shared some details about Niagara2 with *MPR* earlier this year, and the MPF presentation will answer many remaining questions. (See *MPR 2/27/06-03*, "Processor Innovation Is Not Dead.")

Emulex wraps up the Tuesday morning session with "Multicore Processor Provides Low-Latency Virtualization" by Mukund Chavan, hardware architect and senior director of engineering. Emulex will introduce its new Intelligent Storage Processor, which integrates 11 configurable-processor cores from ARC International and a high-bandwidth memory interface. This will be Emulex's first appearance at a Microprocessor Forum.

Tuesday Afternoon: Processor Cores

After lunch, **Cadence Design Systems** will deliver Tuesday's second keynote presentation, "Performance, Power Efficiency, and Function: Optimizing Chip Design for the New Generation," by Ted Vucurevich, senior vice president and chief technology officer. Vucurevich will describe how electronic design automation (EDA) tools will improve the performance and power efficiency of future microprocessors—especially multifunction, highly integrated processors. Following his keynote is the conference's second session, "Processor Cores," which has three presentations, by Ceva, ITRI, and Xilinx.

Ceva begins the session with "RISC-Free Voice-Over-IP System Architecture" by Yair Siegel, senior applications engineer. Siegel will describe a licensable system architecture for handling both the DSP and control tasks of a VoIP system without using a CPU. This presentation was coauthored by Konstantin Merkher, VoIP applications manager.

ITRI comes next with "PAC Digital-Signal Processor" by Dr. David Chih-Wei Chang, deputy general director of the SoC Technology Center at Taiwan's Industrial Technology Research Institute. Chang will describe the Parallel Architecture Core (PAC), two applications processors, and related technologies developed by ITRI's SoC Technology Center in Taiwan. The PAC DSP is a 32-bit programmable DSP for next-generation portable consumer-electronics products, such as portable media players, PDAs, and smartphones. (See *MPR 12/20/04-01*, "Taiwan's Roadmap to Leadership in Design.")

Xilinx wraps up the Processor Cores session with "A High-Performance FPGA-Based System Architecture" by Ralph Wittig, director of the company's Embedded Processing Division. Wittig will introduce a new processor core based on MicroBlaze, a 32-bit RISC core specially designed for integration in Xilinx FPGAs. Xilinx says its new fifth-generation MicroBlaze will run at more than 200MHz in a Virtex-5 device and is backward compatible with previous MicroBlaze processors. (See *MPR 5/17/05-02*, "MicroBlaze Can Float.")

Tuesday Afternoon: Embedded Multicore

The last session on Tuesday afternoon is "Multicores for Embedded Applications," and it contains so many presentations that it continues on Wednesday morning. There will be three presentations on each day.

Ambric begins the session with "A Power-Efficient TeraOPS IC Employs Massively Parallel Architecture" by Mike Butts, Ambric Fellow and IC architect. Ambric will disclose a new chip that the company claims is the first globally asynchronous embedded-processor array capable of executing one trillion operations per second. Initially, Ambric is targeting media processing, but the long-range goal is to tackle applications currently served by high-end DSPs and FPGAs.

Boston Circuits is next with "The Multicore Architecture of the gCORE16" by Hiro Kataoka, president and CEO. Kataoka will disclose the company's unusual Grid on Chip architecture, which integrates several customized 32-bit RISC cores on a chip, along with hardware support for scheduling and managing multiple threads. Kataoka's technical presentation will include an application-level example showing the processing flow of an H.264 video decoder.

Eutecus closes the first portion of this two-part session with "A Multicell Massively Parallel Sensor-Processor Architecture" by Dr. Akos Zarandy, the company's chairman, vice president of technology, and co-chief technology officer. Zarandy will announce a new class of massively parallel multicell sensor processors based on the principles of a cellular neural network. Using algorithms inspired by biological processes, Eutecus is designing these devices for image-processing applications, such as intelligent video surveillance and high-speed object identification.

Following this session, the conference will adjourn to the traditional Tuesday night expo and party in an exhibition room down the hall. In addition to food buffets and an open bar, the expo will have numerous tables of demos and literature sponsored by participating companies. Paid conference attendees will be admitted at no extra charge; others may purchase a separate expo pass for $95.

The traditional Tuesday night expo and party is an opportunity to mingle with exhibitors and fellow attendees. The food and drinks are pretty good, too. (Photo: MPR)

Microprocessor Forums in Japan and Europe

This fall, In-Stat is hosting two additional Microprocessor Forums in Japan and Europe. Several companies participating in our San Jose forum will travel to Japan and Germany to repeat their presentations. There will also be new presentations and keynote speeches unique to each forum.

Microprocessor Forum Japan will be a two-day event on November 7 and 8 at the New Takanawa Prince Hotel in Tokyo. **NTT Docomo** will open the forum with a keynote address on the requirements for higher-performance application processors and other components in next-generation cellphones. For more information about Microprocessor Forum Japan or to register online, follow these links:

- Japanese: *www.ednjapan.com/content/mpf2006/index.html*
- English: *www.ednjapan.com/content/mpf2006/index_english.html*

Microprocessor Forum Europe will be a one-day event on November 13 at the Hilton Munich Park Hotel in Munich (München), Germany. It will precede the opening of the Electronica trade show, to be held November 14–17. Owing to limited facilities, forum attendance is limited to 300 people. For more information or to register online, follow this link:

- English: *www.in-stat.com/empf/06/*

For other inquiries about Microprocessor Forum Japan or Microprocessor Forum Europe, contact Elaine Potter at 480.483.4441 (epotter@reedbusiness.com).

Wednesday: ARM's Keynote, More Multicore

ARM opens the second day of the conference with a keynote: "Priorities in Energy-Optimized Processing" by John Cornish, vice president of ARM's processor division. This will be a technical discussion on the challenges of optimizing throughput while minimizing power consumption. Cornish will describe the trade-offs of various techniques and evaluate which approaches make the most sense for various design goals. After ARM's keynote, Wednesday's first session of presentations continues the "Multicores for Embedded Applications" session that ended on Tuesday afternoon.

Cavium Networks begins with a presentation entitled "A 16-Core MIPS64 Networking Services Processor" by Richard E. Kessler, principal member of Cavium's technical staff. Kessler will introduce the newest member of Cavium's Octeon family of multicore processors, which follows the Octeon CN38xx family. It has a newly enhanced MIPS64-compatible processor core and is designed for a broad range of networking applications, including unified threat management, storage, 3G wireless networks, routing-service blades, and web servers. (See *MPR 2/6/06-01*, "Cavium Expands Octeon Family.")

Optosecurity comes next with "A Massively Parallel Processor for Security Applications" by Dan Gudmundson, chief technology officer. Optosecurity has developed an optical scanner that integrates 16 to 2,048 processors in a parallel-processing fabric. Designed for physical security at airports and other locations, the scanner can detect weapons and weapon components in baggage or on people. It can automatically identify numerous types of weapons, explosives, and contraband items by using X-rays, millimeter waves, and other electromagnetic-wave technologies.

Renesas Technology ends this session with "SH-X3: An Enhanced SuperH Core for Low-Power MP Systems" by Tatsuya Kamei, SH-X3 project leader. Renesas has developed a new embedded processor with four SH-4A processor cores, and it supports both symmetric and asymmetric multiprocessing. To reduce power, the clock frequency of each core is dynamically configurable, in step with workloads. Renesas will fabricate the chip in a 90nm digital CMOS process.

Wednesday PM: Microsoft and Multimedia

After lunch, **Microsoft** will deliver the fourth keynote of the conference, "Balancing the Hardware and Software Components in Mobile Systems," by Kurt Kennett, development lead for Windows CE drivers. Kennett oversees existing and new technology design and implementation for Windows CE. The foundation of his keynote is that a correct hardware/software balance is vital to the power efficiency of any mobile product. Software must understand the capabilities of the hardware, and hardware must know which activities are better left to software. Kennett will outline the current, emerging, and future methods for improving power efficiency and balancing the hardware/software equation. After his keynote, the conference continues with the final session, "Multimedia at the Hardware-Software Interface," which contains five presentations.

Analog Devices (ADI) begins the session with "Fast-Track Development and Processors for Embedded Audio Products" by Dr. David A. Jaffe, senior engineer. Jaffe will show how ADI's VisualAudio graphical development tool lets programmers rapidly create audio-processing code for all types of embedded systems. Examples will cover fixed-point and floating-point implementations.

Freescale Semiconductor is next with "Video and Surveillance Applications Employing the MSC8144 DSP" by Ed Martinez, manager of video systems engineering for Freescale's Digital Systems Division. Martinez will describe Freescale's new MSC8144 DSP, which has four StarCore SC3400 DSP cores (each running at 1.0GHz), 10.5MB of on-chip memory, and integrated peripherals. He will give real-world examples showing how to use the DSP for video encoding, video decoding, and video analytics. (See *MPR 7/17/06-01*, "Freescale's Quad-Core MSC8144.")

Imagination Technologies is next with "The World's First OpenGL/ES 2.0 Mobile GPU Core" by Peter McGuinness, system architect and director of business development. McGuinness will talk about the migration from OpenGL/ES 1.1 to 2.0 and what it means for the design of graphics processors. Imagination Technologies' solution is a scalable architecture for shader-based graphics on mobile devices. Among other things, McGuinness will discuss the concept of tile-based deferred shading, paying special attention to saving power while improving system performance.

LSI Logic follows with "An Advanced Media Processor Architecture for Consumer Applications," presented by Simon Bewick, director of VLSI design. Bewick will review the technical requirements for next-generation media processors, such as the ability to support advanced video-compression standards and to perform multistream video encoding and decoding. He will then describe LSI Logic's latest solution. Earlier this year, at Spring Processor Forum, LSI Logic revealed the details of its new Zevio SoC-design platform. (See *MPR 6/12/06-01*, "LSI Logic Wants Your SoC.")

Texas Instruments ends the hardware-software session with "Demands Placed by HD Transcoding Technologies on DSP Chips" by Jeremiah Golston, CTO for streaming media at TI. Golston will focus on optimizing high-definition transcoding algorithms for DSPs. One problem he will tackle is that of implementing a high-quality transcoding algorithm without exceeding typical bandwidth constraints on external memory. Another challenge is that of supporting the wide range of transcoding combinations among different codec formats, resolutions, frame rates, and bit rates.

MPF will close with a special discussion panel featuring the speakers from all four conference keynotes: John Cornish of **ARM**; Ted Vucurevich of **Cadence**; Dr. Dileep Bhandarkar of **Intel**; and Kurt Kennett of **Microsoft**. This wide-ranging 60-minute discussion will be moderated by Max Baron of *MPR*. Audience questions are welcome. MPF is scheduled to adjourn at 5:25 p.m.

For More Information

Early-bird pricing for **Fall Microprocessor Forum 2006** is open through September 8, with savings up to $600. Separate admissions are available for the all-day seminar (Monday, October 9), two-day conference (Tuesday and Wednesday, October 10 and 11), and Tuesday night expo and party. Low-priced packages and group discounts are available, as are student discounts. For general information or to register online, visit *www.in-stat.com/FallMPF/06/*. For information about group discounts and other matters, contact Elaine Potter at 480.483.4441 (epotter@reedbusiness.com).