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LSI Logic Wants Your SoC

Zevio SoC-Design Platform Has New IP for Consumer Electronics

By Tom R. Halfhill {6/12/06-01}

There was a time when "turnkey solution" meant a preconfigured computer with preinstalled application software for nontechnical users who needed a simple black-box system. A classic example was the Wang dedicated word processor of the 1970s. Any competent typist could quickly learn to use it. In the 1980s, expensive dedicated systems like the Wang were superseded by IBM PCs with preinstalled word-processing software and a daisy-wheel printer.

Lately, the demand for turnkey solutions has been moving much further down the food chain. Semiconductor companies are hearing their customers clamor for board-level "reference designs" that are virtually finished product designs. Just wrap the board in some metal or plastic, write some software, and presto—it's a product. Actually, this trend started in the 1980s, when semiconductor vendors introduced the first PC-compatible chip sets. Anyone could become a PC clone vendor by designing a motherboard and adding an x86 processor, a BIOS, and some DRAM. Soon afterward, Taiwanese suppliers even made it unnecessary to design the motherboard.

Now, the demand for turnkey solutions has reached the chip level. More and more OEM companies want to introduce products that need an ASIC or SoC to be competitive, but either the OEMs don't want to design the chips themselves, or they lack the engineering resources to undertake such a complex project. This is particularly true in the fast-growing consumer-electronics industry, where hundreds of companies fiercely compete in a rapidly changing market. They need expert design services and ready-to-use intellectual property (IP) so they don't have to spend time and money developing everything from scratch.

That is the reason LSI Logic has introduced a new SoC-design platform called Zevio. It consists of hardware IP, software IP, and professional design services for consumer-electronics application processors. Zevio also has emulators and prototyping systems that allow customers to write software in parallel with hardware development. Zevio is compatible with several 32-bit processor cores from ARM and MIPS Technologies, as well as the ZSP family of 16-bit DSP cores. Customers can take the finished chip design to any independent foundry or use one of LSI Logic's affiliated foundries. (In May, LSI Logic completed its exit from the fabrication business by selling its last in-house fab to a subsidiary of ON Semiconductor.)

Zevio made its debut at the annual Consumer Electronics Show in Las Vegas last January, but LSI Logic didn't publicly disclose the technical details until last month's **Spring Processor Forum** in San Jose. Zevio's principal architect, Shinya Fujimoto, described the new IP that LSI Logic developed for the platform: an efficient memory controller, a 2D/3D graphics engine, and a 3D audio engine. In addition, Zevio is compatible with IP already available from LSI Logic—including I/O controller cores and mixed-signal components—as well as licensable IP from third parties. If a customer has proprietary IP, LSI Logic can probably adapt it to the platform as well.

Zevio is available now. LSI Logic has used the platform to develop a one-million-gate multicore test chip that will become a standard part later this year.

Target: Low-Priced Multimedia Gadgets

LSI Logic is well positioned to support an SoC platform like Zevio. The company has nearly 15 years of experience

designing highly integrated chips for consumer electronics, beginning with the MIPS-based chips in Sony's PlayStation-1 and PlayStation-2 videogame consoles. As a long-time ARM and MIPS licensee, LSI Logic can offer 32-bit CPU cores from both those processor-IP vendors without requiring Zevio customers to take a separate license. If the DSP extensions in those general-purpose processors can't handle the application's signal-processing demands, LSI Logic can integrate ZSP-family DSP cores. For instance, the Zevio test chip integrates both an ARM9 and a ZSP400.

Zevio was born after LSI Logic noticed that most of the consumer-electronics SoCs it was designing had common functions. Zevio is primarily intended for customers designing consumer-electronics products retailing for less than $150, although some products—particularly those using the Global Positioning System (GPS)—may cost $300 or more. In general, these products will be electronic toys, edutainment devices, GPS navigation systems, and other gizmos. They typically have small LCD screens for graphics or video, plus audio capabilities. A custom SoC can significantly reduce manufacturing costs by consolidating multiple processors and functions on a single chip.

Unfortunately, many OEMs can't afford the in-house engineering resources required to design an SoC for under-$150 products. As Figure 1 shows, project costs are skyrocketing as fabrication technology migrates to deeper submicron processes. Consequently, developers must resort to using off-the-shelf standard parts, which usually aren't optimal. Zevio is intended to reduce the development costs and time-to-market delays for OEMs facing that dilemma.

LSI Logic says Zevio is not intended for SoCs that would compete against sophisticated processors for mobile communicators, such as the Texas Instruments OMAP chips. (See *MPR 4/24/06-01*, "OMAP3 Sets Specs for Cellphones.") The mixed-signal components required for those kinds of chips tend to be process dependent. For now, Zevio's mixed-signal IP is optimized for 0.13-micron processes—too large and too slow to compete with the latest 90nm and 65nm processes in which vendors like TI are fabricating their cutting-edge communications chips. Also, the Zevio platform lacks a DDR2 memory controller, although LSI Logic plans one in the future.

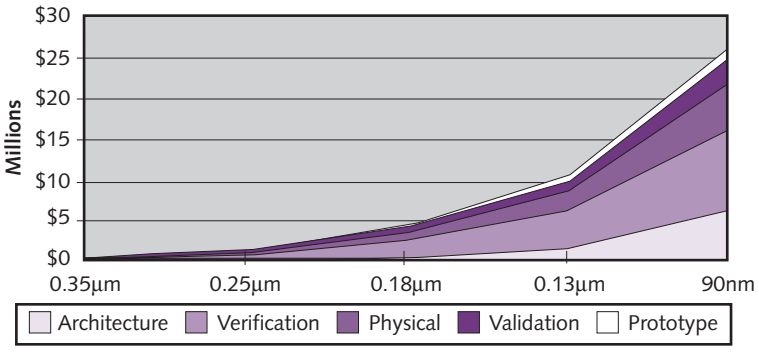

Figure 1. SoC-development costs are rising fast as fabrication technology moves to geometries below 0.18-micron. Larger designs in smaller processes are particularly difficult to verify. As a result, verification costs may actually exceed the costs of other phases of the project. (Data source: International Business Strategies)

Instead of aiming to compete with higher-end SoCs, Zevio concentrates on preverified IP for low-cost consumer electronics. Currently, the platform includes several general-purpose 32-bit processor cores, including the ARM7, ARM9, and ARM11 families and the MIPS32 24K, 5Kf, and 4Ke processors. Just about any core will work with Zevio, but those are the third-party cores that don't require customers to obtain a separate license from the processor-IP vendor. Note that Zevio currently doesn't include ARM's latest Cortex cores or the MIPS32 24KE, which adds DSP extensions to the MIPS32 24K. (See *MPR 5/31/05-01*, "White Paper: The MIPS32 24KE Core Family.") For signal processing, LSI Logic offers the ZSP200, ZSP400, ZSP500, and ZSP600 cores. All the ZSP cores are 16-bit fixed-point DSPs with superscalar pipelining, so their signal-processing capabilities surpass the basic DSP extensions available for the ARM and MIPS processors.

Peripheral IP includes I/O controllers popular in consumer-electronics products: USB 2.0 (including USB On the Go), IEEE 1394 Firewire, and Secure Digital I/O. Zevio's memory-controller cores can interface to SDRAM and NAND flash memory; mobile DDR-DRAM is coming in the future. Mixed-signal components include a USB 2.0 physical-layer interface (PHY), power-management unit (PMU) regulators, and digital-to-analog converters (DAC) for video and stereo audio. For graphics and sound, LSI Logic designed a new 2D/3D graphics engine and a new 64-channel audio engine. There's also an LCD controller for TFT displays. LSI Logic provides software codecs for several audio and video standards, including voice over Internet Protocol (VoIP), MP3, MPEG4, and H.264. An NTSC/PAL decoder and video DAC support TV-out connections.

SDRAM Controller Improves Performance

The most interesting aspect of Zevio is the new IP that LSI Logic created for it. The new memory controller, graphics engine, and audio engine are specifically designed for integration in low-cost consumer-electronics SoCs.

Zevio's AMBA 2.0-compatible memory controller works with inexpensive 16-bit SDRAM and requires only 20,000 gates for a 12-port configuration. Comparable memory controllers from other vendors require more than 100,000 gates, so LSI Logic obviously cut some corners. To save gates, the Zevio SDRAM controller has no caches or FIFO buffers. It compensates by running twice as fast as the AMBA high-speed bus (AHB) and by pipelining control commands to memory, taking advantage of open command cycles without impeding traffic on the bus.

The Zevio SDRAM controller fetches two 16-bit words from memory on every AHB clock cycle.

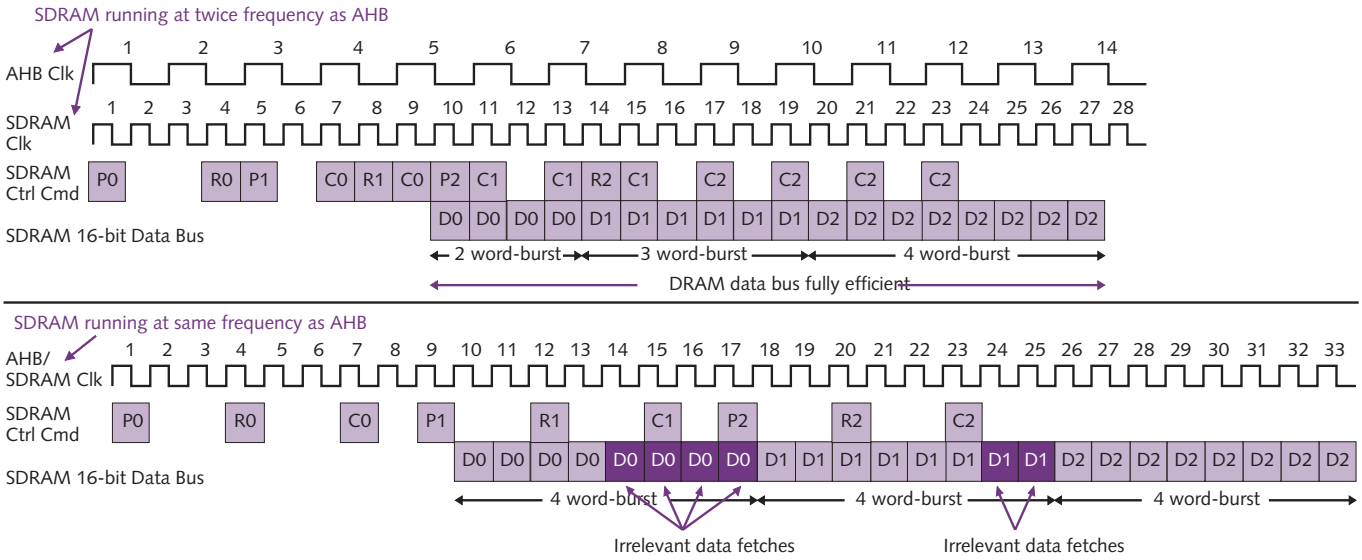

Figure 2. LSI Logic created a new SDRAM controller for the Zevio platform that runs twice as fast as the AMBA 2.0 AHB and fetches data in shorter memory bursts, reading only as much data as the AHB master needs. This is important, because in order to save gates, the memory controller has no internal caches or FIFO buffers for excess data. Notice how pipelined control commands make more efficient use of open command cycles on the bus.

Unlike most memory controllers, it doesn't fetch more data than the AHB master asks for. A typical controller would always request eight bursts of data from memory, in order to fetch as much data per memory access as possible, then cache any excess data in case it was needed later. But the Zevio controller always requests data in shorter bursts, fetching only as much data as the AHB master needs. The controller doesn't speculatively fetch data, because it has no caches or buffers for storing the excess.

LSI Logic says that reading data in shorter, variable-length bursts improves overall throughput by 37.5% and eliminates the controller's need for internal caches and buffers. The trade-off is that a subsequent load from a sequential memory address won't hit the memory controller's cache—because there is no cache. Figure 2 shows an example of variable-length burst reads and pipelined memory commands.

In another refinement, the Zevio memory controller can write bursts of data to nonconsecutive memory addresses without rearbitrating the AHB between bursts, thus reducing the overhead for arbitration. This technique is particularly effective for graphics data that isn't contiguous in memory. To make it possible, LSI Logic defined additional AHB sideband signals that allow the memory controller's AHB master to

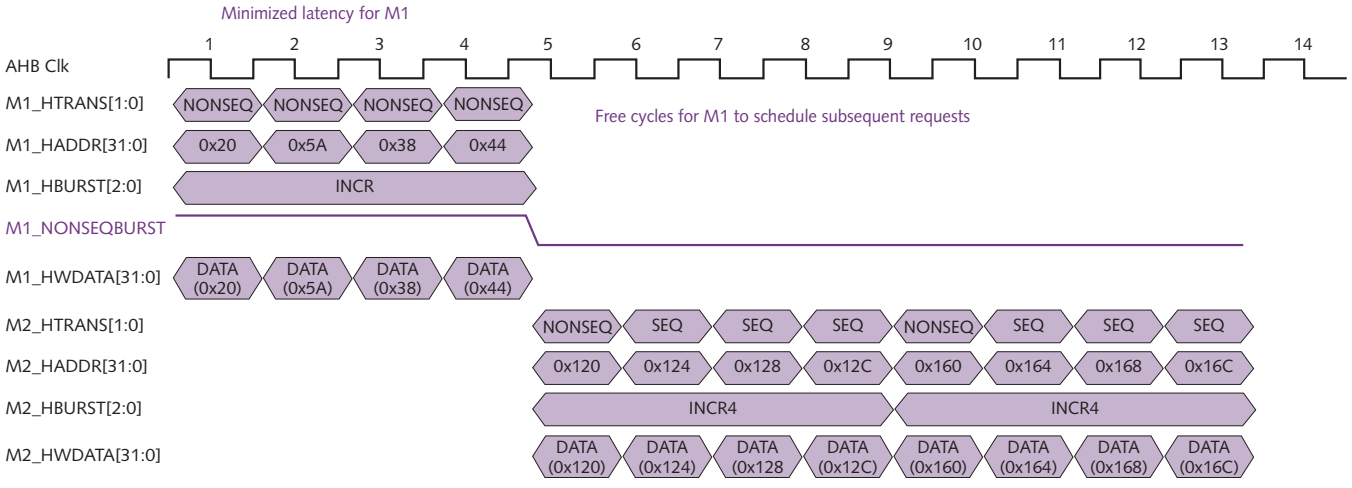

Figure 3. The Zevio SDRAM controller can write data to nonconsecutive memory addresses without rearbitrating the AHB. By holding control of the AHB during these bursts, the controller can reduce the bus-arbitration latency by 70%, according to LSI Logic.

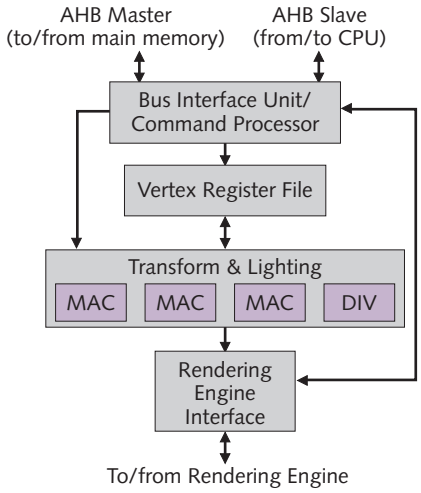

Figure 4. LSI Logic and a Japanese design house, Koto Co. Ltd., created a new AHB-compatible graphics core for the Zevio platform that includes this geometry engine. To save gates, the engine uses 16-bit floating-point math instead of 32-bit for drawing 3D polygons.

maintain control of the bus throughout a nonsequential burst. Figure 3 shows an example.

Overall, LSI Logic made intelligent trade-offs when designing the new memory controller. Although the lack of internal caches and buffers will sometimes impair performance, the ability to read variable-length bursts of data and pipeline the control commands will compensate much of the time. Most important, LSI Logic was able to significantly reduce the controller's gate count. On a million-gate chip, it occupies only about 2% of the area instead of about 10%, which will shave costs.

Graphics and Audio Engines for Multimedia

LSI Logic made similar trade-offs when designing the new graphics and audio engines for the Zevio platform. The goal is to endow low-cost consumer-electronics gadgets with lively multimedia capabilities without bloating the silicon or busting the development budget. These cores are no match for the graphics and sound armaments in the latest videogame consoles, but they aren't intended to be. Even so, the graphics engine delivers performance that's about halfway between a Sony PlayStation-1 and a PlayStation-2.

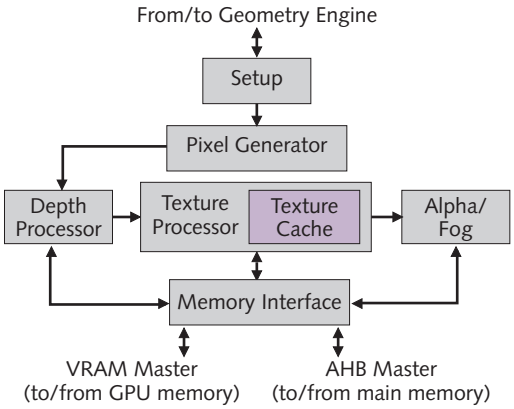

Figure 5. Zevio's 3D rendering engine would have been considered state of the art in the 1990s. Together with the geometry engine, the entire graphics core requires only about 300,000 gates—relatively small for its features.

A Japanese design house, Koto Co. Ltd., codeveloped the Zevio 2D/3D graphics core. Some of Koto's engineers are veterans of the Nintendo Gameboy design team, so they are experienced at squeezing features into small packages. To save gates, the Zevio graphics core requires no local memory for buffering the screen or storing data structures. When graphics performance is secondary—for instance, in a GPS device—the graphics core can buffer the screen entirely in main memory (a unified memory architecture). If performance is more important, the graphics core can integrate local memory for such things as frame buffers and textures. (LSI Logic suggests dedicating 150KB of SRAM to a depth buffer for quarter-VGA screens.)

In another gate-conservation measure, the Zevio graphics core uses the Float16 format instead of 32-bit floating-point numbers for calculating polygon vertices. All together, these economies hold the graphics core to 300,000 gates and limit power consumption to about 20mW at 75MHz for a chip fabricated in a 0.13-micron process.

What do 300,000 gates buy these days? A graphics core with 16 bits per pixel and a 4,096- × 1,024-pixel address space, plus geometry and rendering engines that can draw 1.5 million polygons per second at 75MHz. That's not too shabby, especially considering all the graphics features implemented in hardware, which was state-of-the-art technology not long ago. As Figure 4 shows, the geometry engine has three 16-bit multiply-accumulate (MAC) units and a 16-bit floating-point division unit. It supports autonomous list processing (fetching graphics commands from a programmable list), vertex transformations, and object lighting. For lighting effects, it supports three directional lights and one ambient light, plus three specular lights.

Additional features implemented in the geometry engine's hardware include various types of culling, clipping, and model morphing. Culling eliminates the need to draw polygons, textures, or other elements that won't be visible on screen. Similarly, a feature called near-clipping eliminates the need to draw portions of an object whose coordinates fall outside the image area. Model morphing allows 3D objects to change dynamically, instead of relying entirely on static data. Together, these features accelerate performance and software development by reducing the amount of work the software must do.

As Figure 5 shows, the graphics core's rendering engine has some impressive hardware acceleration, too. It supports Gouraud shading, depth buffering, offset colors, dithering, alpha blending, fog effects, table lookups for color conversions, texture mapping, perspective correction, and bilinear filtering. It has a small 4KB texture cache, which

can store 64- × 32-pixel textures in 16-bit mode, 64- × 64-pixel textures in 8-bit mode, and 128- × 64-pixel textures in 4-bit mode.

All told, the Zevio graphics core has impressive features for its size. However, in a low-cost SoC, the limiting factor on graphics performance will be data bandwidth, not the engine's capabilities. At 75MHz—the graphics engine's clock speed in LSI Logic's test chip—there's only enough bandwidth to support a 512- × 240-pixel screen when using all the fancy graphics features. By using fewer features, the engine can support a 640- × 480-pixel VGA-resolution screen at 75MHz.

Nevertheless, LSI Logic made good trade-offs when designing the graphics core for low-cost systems. Although performance suffers with a unified memory architecture, having that option lets customers decide if the target application justifies the extra gates required for large local memories. Using Float16 instead of 32-bit floating-point math to draw polygons will result in slightly chunkier 3D objects, but the difference will hardly be noticeable on the small displays typically built into inexpensive products. One luxury that increases the graphics core's gate count—bilinear filtering—makes sense, because it reduces pixelation when viewing small texture maps at high magnifications. This feature allows the rendering engine to make the most of its small 4KB texture cache.

Audio Engine Supports 64 Channels

For audio tasks—such as playing music, synthesizing voices, and digitizing speech—Zevio has an optional sound engine that supports up to 64 independent audio channels at a clock frequency of only 24MHz. Developers can use 16 of those 64 channels to create 3D audio effects through stereo headphones and speakers. The audio engine supports three input formats: 8- or 16-bit pulse-code modulation (PCM) and 4-bit adaptive differential PCM (ADPCM). The output format is two-channel 16-bit PCM.

To improve efficiency, the audio engine processes data in 32-sample frames, computing multiple samples for each channel before moving to the next channel. This improves performance and fetches data from external memory in larger bursts, reducing the number of memory accesses. Each channel has independent volume and pitch controls, plus a gain control for the attack-decay-sustain-release (ADSR) envelope, which is useful for shaping musical notes.

Special transfer functions for the 16 3D-audio channels help programmers position sounds anywhere on the stereo sound stage. For example, sounds can appear to emanate from different distances—and from the left, right, front, or back—of a first-person viewpoint on screen. To support this feature, the audio engine has some additional local memory, known as 3D History RAM: 25 16-bit memory locations for each of the 16 3D channels. The 3D sound effects are audible through stereo headphones, or through stereo speakers with help from a cross-talk cancellation filter. (For background information about 3D digital-audio effects, see *MPR 2/22/05-02*, "Hearing Is Believing.") Figure 6 is a block diagram of the Zevio audio engine.

A programmable reverb filter can add echo-like effects to anything from surf guitars to game characters exploring caves. The audio engine can even apply reverb and 3D stereo sound effects to digitized speech or to music decoded from MP3 files by the DSP engine. Despite all these features, the audio engine requires only 80,000 gates and consumes a mere 2mW at 24MHz. It's about the same size as Tensilica's HiFi-2 audio engine for Xtensa configurable processors, but it has higher-level features. (HiFi-2 is a package of low-level extensions based on the original HiFi engine released in 2003; see *MPR 9/29/03-01*, "Tensilica Makes Music.")

LSI Logic provides a driver for MIDI playback and sound-font compression, as well as for MP3 decoding and VoIP on the DSP engine.

For some minimal audio applications, the SoC's host processor could handle the sound processing, eliminating the need for a dedicated audio engine. But for more-demanding applications, the Zevio audio engine—coupled with a ZSP core—offers better capabilities. Even though Apple's iPod dominates the portable-audio market, there are still numerous opportunities for digital-audio products. VoIP is potentially an even larger frontier.

From Specs to Silicon in Nine Months

To demonstrate the effectiveness of the Zevio platform and create a standard part for its own product catalog, LSI Logic has designed a million-gate test chip. It integrates an ARM9 host processor, a ZSP400 DSP, a display processor, and an NTSC video DAC. In addition, it has the new memory

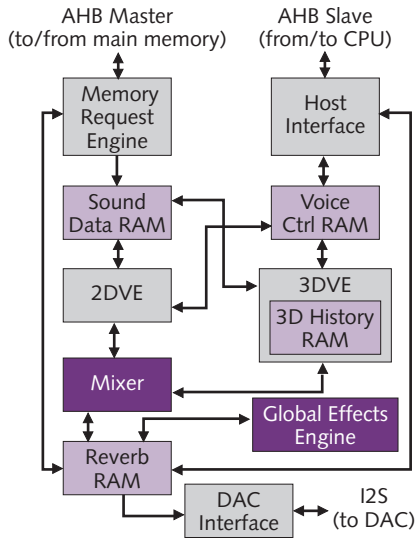

Figure 6. LSI Logic designed a 64-channel audio engine for the Zevio platform. Although it's a relatively small core, it supports a wide variety of stereo sound effects and playback features. It requires a digital-to-analog converter (DAC) either integrated on chip or externally connected to the SoC.

Price & Availability

LSI Logic's Zevio platform for consumer-electronics SoC development is available now. A Zevio license may eliminate the need to obtain separate licenses from LSI Logic's IP partners, such as ARM and MIPS Technologies. The cost of a Zevio license varies, depending on the IP selected. LSI Logic doesn't publicly disclose licensing fees. For more information about Zevio, visit *www.lsilogic.com/zevio*.

controller (supporting 1.8V SDRAM), the 3D-graphics engine, and the audio engine. The ARM9 and ZSP400 run at 150MHz; the graphics and audio engines run at 75MHz. Typical power consumption is below 150mW when driving a QVGA-resolution LCD (320 × 240 pixels).

LSI Logic says it finished drafting the chip's specifications in December 2004, ran software demos on an FPGA simulator in March 2005, taped out the design in August 2005, and received the first silicon in September 2005. Programmers ported the software demos to the chip only three days later. That's nine months from specifications to working silicon and software. A typical project of this type would take 12 to 24 months, barring problems. LSI Logic says the same project would take only six months today, because some of the Zevio IP wasn't finished when the test chip was developed.

To speed development, LSI Logic offers an FPGA prototyping system for Zevio and some low-level software from third parties. The prototyping system has sockets for three FPGAs, which can simulate up to two million ASIC-equivalent gates at clock speeds of 24–48MHz. Each FPGA socket has an associated daughtercard slot. Daughtercards can accommodate mixed-signal blocks or discrete components that can't be simulated in an FPGA.

In addition to the software codecs and drivers already mentioned, the Zevio platform supports two debuggers and in-circuit emulators (Sophia Systems' Watchpoint and Kyoto Microcomputer's Partner); a real-time operating system (Access MicroMore); a compact web browser (Access NetFront, which is found in more than 300 million cellphones and PDAs); and 3D-graphics software (HI Corp.'s MascotCapsule, found in more than 50 million cellphones, PDAs, digicams, and car navigation systems). LSI Logic is porting an embedded version of Linux and says it can port other operating systems on demand.

Sensible Trade-Offs Cut Costs

What's missing from Zevio? Until the Linux port is finished, there's only one operating system to choose from. However, that operating system—MicroMore (μMore), an implementation of MicroItron (μItron)—is popular in Japan, where so many consumer-electronics products are designed.

Some customers may want Windows CE, although it's rather heavy for the low-cost products that Zevio targets. Wind River's VxWorks remains popular, but, like Windows CE, it may be overkill for these applications. Of course, some diehards still prefer to write their own embedded operating systems. Software development shouldn't be a problem, because the two CPU architectures that Zevio supports (ARM and MIPS) have a wealth of tools.

LSI Logic isn't pitching Zevio as a platform for digital-camera chips, but some customers might want to incorporate imaging capabilities into their SoCs for low-end digicams, webcams, and the like. Although the ARM or MIPS host processor might be able to handle those tasks for low-resolution images, a welcome future option might be a small image-processing engine that accelerates such functions as Bayer interpolation, color-space conversion, JPEG compression, and unsharp masking. If present, a ZSP core can accelerate JPEG compression.

Overall, Zevio is a well-conceived SoC platform that makes wise trade-offs between cost and performance. It offers a surprising number of features without falling victim to that scourge of modern times, featuritis. Although similar hardware and software IP is available from other sources, the main attraction of Zevio is that LSI Logic can become a customer's one-stop shop. Zevio reduces or eliminates the need to negotiate multiple licenses and integrate multiple IP blocks from different vendors—a complex process that can fatally lengthen the design and verification stages of an SoC project.