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More Patents for Tensilica

Portfolio Now Includes Ten Patents Related to Configurable Processors

By Tom R. Halfhill {5/30/06-01}

The U.S. Patent and Trademark Office recently issued three new patents to Tensilica for its configurable-processor technology. They follow seven related patents issued from 2002 to 2005. In addition, the patent office has reaffirmed a key Tensilica patent issued in 2002 that was anonymously challenged a year later. As a result, Tensilica now holds an impressive portfolio of at least ten patents on configurable-processor technology.

Tensilica has several additional patents on other aspects of its Xtensa microprocessor architecture, including at least two patents somewhat related to configurable processing. No matter how they're counted, it's a strong portfolio and a testament to Tensilica's contributions in this field.

Chris Rowen, Tensilica's CEO, told *Microprocessor Report* that he has no current plans to assert the patents offensively against competitors. "We're not a belligerent company," he said. Instead, Rowen views Tensilica's growing portfolio as a defensive bulwark against potential action by other companies and as recognition that Tensilica has invented fundamental technology for configurable processors.

MPR has been closely following the race between Tensilica and archrival ARC International to patent their intellectual property (IP) in this field. We believe configurability is critically important for the future of microprocessor design. Customizing a CPU architecture for specific applications can tremendously improve performance, and sophisticated configuration tools enable SoC developers, system designers, and even programmers to play a role formerly restricted to CPU architects.

Anonymous Patent Challenge Backfires

Tensilica received its first U.S. patents for configurable processing in 2002 with patents 6,477,683 and 6,477,697, both issued November 5, 2002. These patents describe the fundamental technology underlying Tensilica's Xtensa microprocessor core and related configuration tools. (See *MPR 12/9/02-01*, "Tensilica Patents Raise Eyebrows.") A few months later, an anonymous challenger—most likely ARC—asked the patent office to reexamine the important '683 patent and narrow the scope of about half the claims. (See *MPR 6/2/03-03*, "Tensilica Patent Challenged.")

But the challenge backfired. Although the patent office required Tensilica to amend five of the '683 patent's 104 original claims, the changes are trivial. *MPR* believes the alterations do little or nothing to weaken the patent. More significantly, the patent office allowed Tensilica to add 102 entirely new claims during the reexamination—almost doubling the original number of claims. The patent office issued a certificate of affirmation for the '683 patent on April 11. So in the end, the anonymous challenge has almost certainly strengthened this key patent. Having survived a lengthy reexamination and emerging with almost twice as many claims, it is unlikely to ever be challenged again.

In 2004 and 2005, the patent office issued five more patents to Tensilica for configurable-processor technology. In January, March, and April of this year, the patent office issued three additional patents to Tensilica in this field. Table 1 lists all these related patents with their numbers, titles, application dates, and issue dates. Note that the table doesn't list Tensilica's other patents that are peripherally related to configurable-processor technology.

In all, Tensilica's ten patents contain nearly 450 claims of inventions in the rapidly evolving field of configurable-processor technology. Although judging the strength of a patent portfolio by counting claims is like measuring microprocessor performance by counting megahertz, the large number of claims does indicate that Tensilica is staking out a great deal of territory.

Five Patents Describe Automated Tools

Of the eight U.S. patents issued to Tensilica for configurable-processor technology since 2004, four are continuations of previous Tensilica patents or are based on previous Tensilica patents or patent applications. By definition, they incorporate the specifications and claims of the patent or patents on which they are based, and they extend the invention by adding new claims. This is an important point, because continuation patents inherit the "priority date" of the earliest original patent on which they are based. The priority date establishes when the patent became effective, even if it's years before the issue date.

Three patents describe highly automated technology for rapidly generating processor extensions, such as new application-specific instructions. These three patents are 6,701,515 ("System and Method for Dynamically Designing and Evaluating Configurable Processor Instructions"); 6,760,888 ("Automated Processor Generation System for Designing a Configurable Processor and Method for the Same"); and 6,941,548 ("Automatic Instruction Set Architecture Generation").

The technology those patents describe appeared in 2004 when Tensilica introduced its XPRES (Xtensa PRocessor Extension Synthesis) tools. XPRES can create thousands of possible processor configurations in minutes by analyzing application software written in ordinary C code. (See *MPR 7/12/04-01*, "Tensilica's Automaton Arrives.") The '888 patent is a continuation of Tensilica's important '683 patent, so it inherits the earlier patent's priority date of February 5, 1999.

Two other patents describe technology related to hardware abstraction layers. These layers consist of low-level software that insulates higher-level software from implementation details of the processor. Abstraction is especially important for a configurable-processor architecture that can morph into many forms. Patent 6,763,327 ("Abstraction of Configurable Processor Functionality for Operating Systems Portability") describes an abstraction layer for an embedded operating system. It allows a single binary kernel to be compatible with many different processor configurations.

For example, during a context switch, the operating system must save all of a processor's state information (registers, the program counter, and so on) for the current context so the operating system can restore the state later. But doing this poses a problem for configurable processors, because developers can freely add new registers and other state when customizing the processor for specific applications. Ordinarily, this would require modifying the operating-system kernel for each new configuration. Instead, Tensilica's automatically generated abstraction layer has a static "save context" subroutine that the operating system calls. The subroutine knows about any new registers or other state.

Similarly, patent 6,986,127 ("Debugging Apparatus and Method for Systems of Configurable Processors")

U.S. Patent Number	Patent Title	File Date	Issue Date	Notes
6,477,683	"Automated Processor Generation System for Designing a Configurable Processor and Method for the Same"	5-Feb-99	5-Nov-02	A fundamental patent; see *MPR* 9-Dec-02
6,477,697	"Adding Complex Instruction Extensions Defined in a Standardized Language to a Microprocessor Design to Produce a Configurable Definition of a Target Instruction Set, and HDL Description of Circuitry Necessary to Implement the Instruction Set, and Development and Verification Tools for the Instruction Set"	28-May-99	5-Nov-02	A fundamental patent; see *MPR* 9-Dec-02
6,701,515	"System and Method for Dynamically Designing and Evaluating Configurable Processor Instructions"	27-May-99	2-Mar-04	Technology for modifying software-dev tools
6,760,888	"Automated Processor Generation System for Designing a Configurable Processor and Method for the Same"	1-Nov-02	6-Jul-04	Continuation of 6,477,683
6,763,327	"Abstraction of Configurable Processor Functionality for Operating Systems Portability"	17-Feb-00	13-Jul-04	Related to five other patent applications
6,854,046	"Configurable Memory Management Unit"	5-Aug-02	8-Feb-05	Based on provisional application filed 3-Aug-01
6,941,548	"Automatic Instruction Set Architecture Generation"	16-Oct-01	6-Sep-05	XPRES tool technology
6,986,127	"Debugging Apparatus and Method for Systems of Configurable Processors"	3-Oct-00	10-Jan-06	Abstraction layer for debugger
7,020,854	"Automated Processor Generation System for Designing a Configurable Processor and Method for the Same"	2-Jul-04	28-Mar-06	Continuation of 6,760,888
7,036,106	"Automated Processor Generation System for Designing a Configurable Processor and Method for the Same"	17-Feb-00	25-Apr-06	TIE-language technology

Table 1. Tensilica has accumulated a portfolio of ten patents explicitly related to configurable-processor technology. A particularly important one is the '683 patent, which recently survived a challenge and reexamination. (And yes, four of these patents really do have the same title.)

describes technology related to a hardware abstraction layer for debuggers. Like an operating system, a debugger must be aware of the processor's state information so it can display the contents of registers and so forth. Tensilica's highly automated tools generate a processor-aware abstraction layer that allows a single binary of a debugger to work with any processor configuration.

Additional Patents Cover MMU and TIE

Three patents issued since 2004 describe technology related to Tensilica's configurable memory-management unit (MMU) and automatic processor-generation tools. Patent 6,854,046 ("Configurable Memory Management Unit") is merely one example of the numerous hardware and software components that Tensilica's engineers had to create in order to provide developers with a flexible configurable-processor architecture.

By itself, an MMU isn't particularly difficult to design. But Tensilica's configurable MMU allows developers to tailor many aspects of memory management to a specific application. The MMU is an option for Tensilica's Xtensa V and Xtensa 6 processor cores, but not for the Xtensa LX. (See the sidebar, "Tensilica Introduces Xtensa 6 Processor Core" in *MPR 11/28/05-01*, "Tensilica Previews Video Engine.")

The two newest patents were issued in March and April of this year. Both of them—7,020,854 and 7,036,106—share the same title: "Automated Processor Generation System for Designing a Configurable Processor and Method for the Same." (The U.S. patent office doesn't require unique titles; the same title appears on the 6,760,888 patent issued in 2004 and the '683 patent issued in 2002.) The '854 and '106 patents expand on the general configurable-processor technology that earlier patents describe, thereby providing additional protection for Tensilica's IP. The '854 patent is a continuation of the '888 patent, which itself is a continuation of the fundamental '683 patent. Therefore, the '854 patent inherits the priority date of the '683 patent (February 5, 1999), even though it was filed in 2004 and issued in 2006.

Both the '854 and '106 patents are lengthy and extremely detailed. They include examples of Tensilica Instruction Extension (TIE) language, the company's proprietary hardware-description language for crafting custom instructions and other processor extensions. TIE is the keystone for much of Tensilica's patented IP. It's a high-level, correct-by-design language that allows developers to write behavioral descriptions of new instructions, registers, I/O ports, and other features.

TIE Distinguishes Tensilica's Technology

As we noted in our 2002 in-depth article about Tensilica's first patents in this field, TIE is an important differentiation between Tensilica's configurable-processor technology and a large body of related prior art. Despite many years of research and development at various companies and academic institutions, no other configurable-processor system has successfully assembled all the same pieces that distinguish Tensilica's Xtensa system. (See the sidebar "Earlier Configurable Processors: Close, But No Cigar" in *MPR 12/9/02-01*, "Tensilica Patents Raise Eyebrows.")

Near the beginning of the new '854 patent is an interesting section titled "Background of the Invention." Nearly 3,000 words long, it reviews similar technology from other companies, specifically describing processors from competitors like ARC and ARM. The same text appears in some earlier Tensilica patents related to the '854 patent. It's a well-written comparative analysis that seems intended to educate the patent examiners about an arcane subject. After all, even some experienced CPU architects may not be familiar with the technical details of configurable processors. The language in this section is more straightforward that the usual legalese in the claims, which are more difficult for laypeople to interpret.

A similar section in the identically titled '106 patent provides additional background and explanation. This patent—which has only one independent claim, followed by 38 dependents—appears to focus more narrowly on Tensilica's technology for automatically generating software-development tools that support an extended instruction-set architecture. For instance, the patent cites an example of creating new datatypes for DSP algorithms. Tensilica's processor-generation tools can automatically modify the company's C/C++ compiler to recognize the new datatypes as if they were native types. This capability keeps the development tools in sync with the customized instruction-set architecture.

Two additional U.S. patents we omitted from Table 1 are somewhat related to configurable processing but are more focused on other things. On November 13, 1998, Tensilica filed patent 6,282,633, which was granted on August 28, 2001. Entitled "High Data Density RISC Processor," it describes the Xtensa microprocessor architecture, a 32-bit RISC architecture that Tensilica purposefully designed for configurability. On February 9, 2001, Tensilica filed patent 6,888,838, which was granted on May 3, 2005. Entitled "Fast IP Route Lookup With Configurable Processor and Compressed Routing Table," it describes how to apply a configurable processor to a specific application domain—in this case, network routing. Tensilica's foundation is configurability, so almost all the company's patents have some connection with the technology.

Tensilica and ARC Have the Nukes

Will Tensilica's newly fattened patent portfolio alter the competitive landscape? For now, probably not. Tensilica's most direct competitor for configurable processors is ARC. ARC's corporate predecessor, Argonaut Software, began licensing its first configurable processor in 1997—the same year Tensilica was founded and a year before Tensilica launched Xtensa. Although ARC got the jump on Tensilica, the latter company has created a more sophisticated end-to-end system and was quicker to file patents. Nevertheless, ARC received an important U.S. patent on its own automated tools last year. (See our in-depth analysis in *MPR 8/29/05-01*, "ARC Patent Looks Formidable.")

For More Information

Full text and graphics for U.S. patents are freely available online at the U.S. Patent and Trademark Office website. Enter the patent number on the following web page, or click the search button to browse the patent database using other criteria:

http://164.195.100.11/netahtml/srchnum.htm.

Another direct competitor is MIPS Technologies. MIPS introduced the configurable Pro Series versions of some of its processors in 2003. (See *MPR 3/3/03-01*, "MIPS Embraces Configurable Technology.") As a relative newcomer to this field, MIPS doesn't offer quite as much flexibility and automation as ARC and Tensilica do. But then, MIPS doesn't aggressively market itself as a configurable-processor vendor, either. MIPS prefers to compete in other ways, such as introducing the first licensable processor with hardware multithreading. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.")

Looming over the whole landscape is ARM, by far the most successful processor-IP vendor. ARM's sales dwarf those of all competitors put together. Flush with success, ARM perceives little need to imitate the configurability that ARC, MIPS, and Tensilica provide. True, ARM's latest processor does offer a few more configurable features than previous ARM cores do. (See *MPR 5/16/06-01*, "ARM Reveals Cortex-R4.") However, the Cortex-R4 still doesn't approach the free-wheeling philosophy that ARC, MIPS, and Tensilica espouse—mainly because ARM still forbids developers to alter the instruction-set architecture. If ARM ever feels more competitive pressure from its configurable foes, the growing number of ARC and Tensilica patents may limit ARM's range of motion in this area.

So far, ARC and Tensilica have wisely chosen not to wield their patents against each other. It's a standoff not unlike the mutually assured destruction (MAD) that prevented the Cold War from exploding into World War III. Neither company can afford a nuclear exchange.

ARC went public in 2000, just in time for the tech bust. Shareholders found their equity hammered into a penny stock (actually, a pence stock, because ARC trades on the London Stock Exchange), and the feisty company is still struggling toward profitability. Meanwhile, Tensilica is approaching its tenth birthday and remains private, so its finances aren't public. Of course, the tech bust made initial public offerings as obsolete as $50,000 signing bonuses for newly graduated engineers, which may explain why Tensilica has been playing hermit. Now that the economic climate for technology companies has improved, Tensilica may be contemplating a public offering. A one-megaton patent lawsuit lobbed by either company wouldn't make potential investors feel very comfortable.

The most likely scenario is that ARC and Tensilica will continue expanding their patent portfolios for defensive purposes, and to deter ARM and other companies from encroaching too far into their territory. Both companies are also filing patents in other geographical regions—particularly in Asia, where emerging markets promise future growth. Eventually, *MPR* believes, the industry will become more aware of the value of configurable processors, and demand will surge. If ARC and Tensilica can survive that long, their pioneering work will pay off. ◇