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POWER EFFICIENCY AT SPF 2006

Preview: Spring Processor Forum's Theme Is Power-Efficient Design

By Tom R. Halfhill {4/24/06-02}

Power consumption is the immovable object that is coercing irresistible forces like Intel, Apple, and IBM to find strategic detours. Searing wattage compelled Intel to abandon its pursuit of high clock frequencies and instead design PC processors with power-efficient cores. The same power-performance trends exerted so much gravity on Steve Jobs's reality-distortion field that Apple has abandoned PowerPC in favor of Intel's newly improved processors. And the very same immovable object persuaded IBM, Sony, and Toshiba to design the Cell Broadband Engine with a relatively simple PowerPC core surrounded by an array of power-efficient coprocessors.

If the industry's heavyweights can't displace the immovable object of power consumption, but can only steer around it, what hope is there for the average line engineer designing an SoC? Aggravating the problem is the public's growing demand for mobility and versatility in consumer electronics. Not only do people want smaller, cuter cellphones, but they also want their new phones to integrate a multimegapixel digital camera, an MP3 player, a videogame machine, and sundry other power-hungry functions—while running longer on a battery charge, of course.

Enrolling consumers in a crash course on electrical engineering isn't an option, so designers must seek alternatives. That's why our theme for **Spring Processor Forum 2006** is power-efficient design. You've got problems. We've got answers.

SPF 2006: A Quick Overview

Hosted by In-Stat and *Microprocessor Report*, **SPF 2006** will be held May 15–17 at the Doubletree Hotel in San Jose, California. As usual, there's a seminar on Monday, followed by a two-day conference on Tuesday and Wednesday. An evening vendor expo and party will follow Tuesday's conference sessions. Separate admissions are available for each event, as well as discounted package deals. (For more information and to register online, visit *www.in-stat.com/spf/06*.)

Monday's all-day seminar is "Implementing Low-Power SoC Configurations," presented by Max Baron, *MPR* principal analyst. Baron's newly updated seminar shows how SoC vendors use architecture, microarchitecture, software, and power management to attain high performance while achieving the best combination of power consumption, integration, and flexibility. The seminar will analyze and compare more than 25 processor cores, chips, and SoCs, including the latest introductions for cellphones, digicams, PDAs, and other low-power systems. (To register online, visit *www.in-stat.com/spf/06/seminars.htm*.)

Each day of the conference will feature a theme-related session on power-efficient design. Other sessions are dedicated to DSPs, licensable intellectual property (IP), and video processors. There will be several introductions of new processors and other products, as well as presentations disclosing new technical details about previously announced products. Each day will begin with a keynote address—this year's speakers are from AMD and P.A. Semi. As always, audience questions are welcome.

Companies participating in SPF 2006 include ARM, Connex Technologies, Element CXI, EEMBC, Freescale Semiconductor, Handshake Solutions, Intellasys, LSI Logic, MIPS Technologies, National Instruments, National Semiconductor,

P.A. Semi, Sci-worx, Silicon Hive, Tarari, Tensilica, Texas Instruments, Transmeta, and Vivace Semiconductor. Sponsors include Freescale, IBM, InsideChips.com, and Vivace.

Conference Day One: DSPs and IP

AMD Senior Fellow Chuck Moore opens the first day of the conference with his keynote address, "Redefining Performance Through System Balance." Until recently, microprocessor architects concentrated on the raw speed of the microprocessor core, but things have changed dramatically. Moore will discuss the evolving roles of power efficiency, on-chip system architecture, chip multiprocessing, throughput performance, modularity, and flexibility.

The first conference session is "Advances in DSP Engines," with four presentations of power-efficient digital-signal processors and cores, including some complex multicore designs.

Element CXI begins with "The Elemental Computing Architecture," by Paul Master, director of technology. Element CXI is a two-year-old startup founded by engineers from Chameleon, Morphics, Quicksilver, and Xilinx. They have created an entirely new microprocessor architecture based on arrays of processing elements, including several elements optimized for signal processing. Master will unveil technical details about the architecture and show some programming examples.

Freescale Semiconductor follows with two closely related presentations by two of the lead DSP architects from the company's design center in Israel. The first presentation is "Freescale's Developments on the Newest Core Architecture from StarCore," by Zvika Rozenshein, director of DSP cores and platforms. In this presentation, Rozenshein will discuss Freescale's implementations of the latest StarCore DSP core, announced last October. This new core is the foundation of a new multicore DSP from Freescale. The company's second presentation, "Freescale's High-Performance DSP Aims at Next-Generation Converged Networks," will introduce that multicore DSP. Odi Dahan, chief architect of DSP SoC design, will reveal significant technical details about the DSP's microarchitecture, performance, and software support.

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Texas Instruments wraps up the DSP session with "F1: TI's Implementation of the ARM Cortex-A8," by Ty Garibay, the ARM cores program manager for TI's wireless terminal business unit. Garibay will disclose new technical details about TI's first implementation of the ARM Cortex-A8 superscalar processor core. (See our two-part coverage of the ARM Cortex-A8 in *MPR 10/25/05-02* and *MPR 11/14/05-01*, "Cortex-A8: High Speed, Low Power.") This is the same core that TI is integrating into its powerful new OMAP3430 chip. (See *MPR 4/24/06-01*, "OMAP3 Sets Specs for Cellphones.")

New Licensable IP for SoC Designers

Tuesday's second conference session is "Next-Generation Licensable Processors and IP." IP cores are indispensable for designing ASICs and SoCs in embedded systems, and the growing demand for power-efficient processing is driving the evolution of licensable IP in new directions. This session includes presentations about the first commercially available clockless 32-bit processor core, the first licensable multithreaded processor core, a new low-power 32-bit embedded processor, and a new IP platform for chip design.

ARM begins with "A New ARM Cortex Processor for Power-Efficient Embedded Systems," by Richard York, product manager. In this presentation, ARM will reveal a previously undisclosed 32-bit processor core—the latest member of the Cortex family. This processor is designed specifically for developers working within tight power and cost constraints in real-time systems. Among other improvements, it sharply reduces the number of clock cycles required for interrupt handling and is more configurable during logic synthesis.

Handshake Solutions follows with "ARM996HS: The First Licensable, Clockless 32-Bit Processor Core," by Arjan Bink, chief design engineer at this Royal Philips Electronics subsidiary in the Netherlands. Bink will explain the intriguing technology inside the new ARM996HS, the world's first commercially available 32-bit processor core implemented with asynchronous (clockless) logic. The ARM996HS is a breakthrough design that consumes very little power and dramatically reduces electromagnetic emissions. (See *MPR 2/21/06-01*, "Can ARM Beat the Clock?" and *MPR 11/29/04-02*, "ARM's Asynchronous Handshake.")

LSI Logic is next with "The Zevio Architecture for Consumer SoC Development," by Shinya Fujimoto, principal architect. Fujimoto will describe the technology behind Zevio, a new SoC-development platform. Zevio includes ready-to-use IP cores for memory control, 3D graphics, and 3D sound synthesis—all designed for efficiency in portable consumer electronics. Zevio also enhances the performance of the ARM AHB bus, enabling smoother data traffic through on-chip interconnects.

MIPS Technologies wraps up this session with "The MIPS32 34K Processor: Multithreading Optimizations in a Single-Issue Pipeline," by Darren Jones, engineering director for microprocessor development. The new 34K is the first licensable embedded-processor core with hardware support

for pipelined multithreading. It can simultaneously mix instructions from as many as five different processes in its uniscalar pipeline, and it can switch contexts in a single clock cycle. MIPS will reveal new details about the technology inside this innovative processor. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.")

Technology for Power-Efficient Processing

The last session on the first day of the conference directly addresses the theme of SPF 2006. It's actually a megasession with seven presentations distributed over two days. "Technology for Power-Efficient Processing, Part 1" begins with two technical presentations from Tensilica and National Semiconductor.

Tensilica starts the session with "Xtensa Energy Xplorer," by Dr. Jagesh Sanghavi, engineering manager, and Eliot Gerster, a member of the technical staff. Tensilica will explain how its special tools allow SoC developers to accurately estimate the power consumption of an Xtensa configurable-processor core and subsystems before committing the design to silicon. The Xtensa architecture supports thousands of possible processor configurations and unlimited custom extensions. By using simulated workloads, feedback from known configurations, and other data, Tensilica's tools can estimate how much energy the processor will require.

National Semiconductor follows with "Optimizing the Power for Multiple Voltage Domains," by Mark Hartman, staff applications engineer. Hartman will describe the challenges facing today's chip designers and system developers, delving into technical details about different methods of power saving and power-conversion control in multifunction cellphones. He will then introduce National's second-generation PowerWise technology for adaptive voltage scaling and compare it with existing PowerWise technology. (See *MPR 1/21/03-01*, "Analog and CPU Wizards Reduce Digital Power.")

After these presentations, the conference will adjourn until Wednesday so attendees can move to another ballroom for the customary vendor expo and party. This lively food-and-drink event continues until about 8:00 p.m. Exhibitors will include ARM, Ceva, CoWare, Green Hills Software, Infineon, InsideChips.com, Intellasys, MIPS, Obsidian, Silicon Hive, Tensilica, Vast Systems, Vivace, and Xilinx. (Admittance to the expo is free with forum registration; others can attend for a separate fee without attending the conference. See *www.in-stat.com/spf/06*.)

Day Two: Power Efficiency and Video

Wednesday's opening keynote address—"From StrongARM to PWRficient: the Ongoing Battle to Reduce Power in Microprocessors"—is by famed engineer Dan Dobberpuhl, president and CEO of **P.A. Semi**. In the 1990s, Dobberpuhl led the team that developed the high-performance, low-power StrongARM chip. Most recently, at P.A. Semi, he led the development of the new PWRficient family of processors based on the Power Architecture. (See *MPR 10/25/05-01*, "P.A. Semi: New Blood for Power.") At SPF, Dobberpuhl's keynote will review the basic physics of power in ICs and the design principles behind StrongARM, then explain the evolution of those principles when applied to the latest 65nm fabrication technology and the PWRficient family. He will also extrapolate those concepts to future generations of microprocessors at 45nm and beyond.

After the keynote, the conference resumes with Part 2 of the session started on Tuesday afternoon, "Technology for Power-Efficient Processing." **Freescale** begins by presenting "Improved Scalable Power-Management Solutions," by Mike Olivarez, principal staff scientist. Olivarez will describe Freescale's Smart Speed technology, which employs several techniques to reduce power consumption in embedded processors and DSPs. His presentation builds a strong case in favor of top-to-bottom power management that starts with the processor architecture and extends all the way to the operating system and energy source.

Silicon Hive follows with "New Core Enables Programmable Camera-Sensor Signal Processing," by Jeroen Leijten, chief technology officer of this Royal Philips Electronics line of business in the Netherlands. Silicon Hive will introduce a new licensable processor core designed for manipulating image data in digital cameras and camera-equipped cellphones. It's based on the same configurable parallel-processor architecture that Leijten described at our forums in 2003 and 2005. (See *MPR 12/1/03-02*, "Silicon Hive Breaks Out," and *MPR 6/20/05-01*, "Busy Bees at Silicon Hive.")

ARM is next with "ARM Cortex-A8: Power-Aware, High-Performance Design," by Vivek Nagaraj, the lead implementation engineer on the Cortex-A8 project. Nagaraj will deliver an in-depth technical presentation about ARM's first test-chip implementation of the Cortex-A8 superscalar processor core. He will reveal new details about the semicustom design techniques that allow ARM's most powerful processor to achieve high throughput while holding power consumption to surprisingly low levels. A key technique is the tiled structure of the circuit layouts.

Transmeta follows with "Power Reduction Using LongRun2 in Efficeon Processors," by Dave Ditzel, founder and chief technology officer. LongRun2 is a transistor-level

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For More Information

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power-saving technology that Transmeta originally developed for its x86-compatible microprocessors. The company is now licensing LongRun2 technology to other companies. (See *MPR 5/2/05-01*, "The Transformation of Transmeta.") Ditzel will describe LongRun2 and how it has reduced power in Transmeta's Efficeon processors.

EEMBC (Embedded Microprocessor Benchmark Consortium) wraps up the session on power-efficient processing with "Benchmark Methodology for Evaluating Processor Energy Costs and Performance," by Shay Gal-On, director of software engineering for EEMBC. This presentation was coauthored by Greg Crouch, the embedded-systems business-development director at National Instruments. EEMBC will introduce new methods for measuring and characterizing the power consumption of embedded processors—a difficult project that has been under way for more than two years. These new benchmark tests will join the throughput-oriented benchmark suites that numerous engineers use when evaluating embedded processors and cores. (See *MPR 2/22/05-01*, "EEMBC Expands Benchmarks.")

New Video Processors Proliferate

The last conference session at SPF 2006 is "Innovative Video Processors," a hot category. Digital video is one of the fastest-growing markets for embedded processors. The long-anticipated rise of HDTV and plunging prices of flat-panel displays are driving millions of consumers to buy new TVs for their homes. At the same time, trend-setting companies like Apple and Google are jump-starting a new market for portable video players and video downloads. The video processors in this session include aggressive low-power designs for portable systems and a new massively parallel architecture for high-definition video processing.

Connex Technology begins the session with "The CA1024: A Massively Parallel Processor for Cost-Effective HDTV," by Gheorghe Stefan, the chief scientist of this Silicon Valley startup. Dr. Stefan is also a professor of electrical engineering at the Polytechnica University of Bucharest in Romania. He worked on the concept for this radical microprocessor architecture for 20 years before finding backers to help launch Connex in 2002. His presentation will introduce the first commercial implementation of a video processor based on the architecture, which *MPR* recently covered in some detail. (See *MPR 1/9/06-01*, "Massively Parallel Digital Video.")

Intellasys comes next with "A New Multicore Architecture for High Performance and Low Power," by Charles Moore, chief technology officer. Intellasys is a Silicon Valley startup with an unorthodox multicore-processor architecture targeting distributed digital-media applications. Moore will introduce the architecture, describe the first core implementation, and reveal the first chip that integrates multiple instances of the core. The programming model of this architecture is particularly unusual. It's a dual stack-oriented design with an unbelievably small instruction set, and programmers will use a library of code objects written in a RISC version of ANSI Forth.

Sci-worx, a German company based in Hannover, will present "MuViStar: A New Video-Processor Architecture Using Custom Extensions," by Hans Volkers, senior system architect. MuViStar (which stands for Multistandard Video decoder and encoder) uses Tensilica's Xtensa LX configurable-processor core, plus VLIW extensions, SIMD instructions, and custom logic. It's designed to support multicore implementations that can scale to several levels of performance. Sci-worx will reveal technical information about the nature of its extensions and how they accelerate audio/video processing.

Tarari follows with "Multicore Content Processors for Efficient HD-Video Encoding," by Jeff Carmichael, who is the vice president of engineering, chief technology officer, and cofounder of this four-year-old company from southern California. Carmichael will describe how Tarari's video accelerators and boards can efficiently encode high-definition video while holding power consumption to a few watts. Tarari first appeared at SPF 2005.

Vivace Semiconductor is a Massachusetts-based fabless semiconductor company only six months old. Vivace is making its debut at the forum with a presentation entitled, "Two New Video Processors for Portable Media Players and Digital TV," by Cary Ussery, the company's president, CEO, and founder. Vivace is designing two programmable media processors supporting several popular media standards. A key feature is the JazzDSP core from Improv Systems. (See *MPR 3/17/03-04*, "ZSP500 and Jazz Play Different Beats," and *MPR 3/27/00-03*, "Jazz Joins VLIW Juggernaut.") These VLIW engines are central to Vivace's processor modules. In addition, the chips will have special hardware for accelerating digital-rights management and security protocols.

The session on video processors will conclude the two-day conference and the forum. In all, this year's SPF will have 20 technical presentations, two keynote addresses, one full-day seminar, and the vendor expo. As at last year's Fall Processor Forum, registered attendees can download Adobe PDF versions of the presentations over a wireless network at the conference or receive the files on a Flash drive. (And this time we'll try to keep the wireless network from crashing.) ◇

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