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TENSILICA'S PRECONFIGURED CORES

Six Embedded-Processor Cores Challenge ARM, ARC, MIPS, and DSPs

By Tom R. Halfhill {3/20/06-01}

Tensilica has introduced six preconfigured versions of its 32-bit processor cores to suit an unusually broad range of embedded applications. Whereas the smallest configuration is suitable for deeply embedded microcontrollers in real-time systems, the largest configuration

sets a new record for DSP benchmarks. The six cores in Tensilica's new Diamond Standard Series are the 108Mini, 212GP, 232L, 570T, 330HiFi, and 545CK. The 232L is based on Tensilica's latest Xtensa 6 configurable-processor core, while the others use the older but similar Xtensa LX core. All Diamond processors are available now for licensing as synthesizable intellectual property (IP). Tensilica plans to offer prehardened firm cores in the near future.

We will describe these cores in more detail below, but here's a quick summary. The 108Mini is a low-power cacheless controller positioned against the ARM7TDMI-S; the 212GP is a higher-performance controller with caches and variable-size scratchpad memories, similar to an ARM9-class processor; the 232L has an MMU capable of supporting sophisticated operating systems such as Linux; the 570T uses long-instruction-word extensions and other enhancements to compete with ARM11-family cores; the 330HiFi is a 24-bit audio processor for digital music and speech; and the 545CK has powerful DSP extensions that push it past every licensable processor core ever benchmarked by Berkeley Design Technology (BDTI).

It may seem odd that a company as closely wedded to configurable-processor technology as Tensilica would introduce so many preconfigured cores. But it makes sense for several reasons, without signaling a retreat from Tensilica's central strategy.

Some customers simply don't want to bother configuring a processor core, even though Tensilica's configuration tools are the best in the business and a custom configuration

would probably deliver better performance. By introducing preconfigured cores positioned against the ARM7, ARM9, ARM10, and ARM11, Tensilica is confidently inviting direct comparisons with processors from the industry's leading IP vendor. Indeed, to ease the software transition, Tensilica has configured the first Diamond cores as little-endian processors, just like most ARM designs. Tensilica plans to release big-endian versions later. (Xtensa cores are configurable as either little- or big-endian.)

Another rationale for preconfigured cores is to counter recent moves by ARM, ARC International, and MIPS Technologies. ARM has introduced the superscalar Cortex-A8 and the uniquely asynchronous ARM996HS. (See *MPR 10/25/05-02* and *MPR 11/14/05-01*, "Cortex-A8: High Speed, Low Power," and *MPR 2/21/06-01*, "Can ARM Beat the Clock?") Last year, ARC introduced six preconfigured cores based on the ARC 600 and ARC 700 configurable processors. (See *MPR 3/14/05-02*, "ARC's Preconfigured Cores.") And last month, MIPS introduced the MIPS32 34K, the first licensable multi-threaded processor core. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.")

Tensilica's new cores demonstrate the versatility of the Xtensa architecture and the power of Tensilica's development tools, which the company used to create all six variations. In addition, Tensilica plans to introduce prehardened firm cores that will help the company penetrate fast-growing embedded markets in developing nations, where soft cores are more vulnerable to IP thieves.

Configurations Are Remarkably Diverse

Anyone unfamiliar with the concept of configurable-processor technology would probably never guess that all six Diamond cores are offspring of the same basic microarchitecture. Their features are so varied that they could come from different companies. Yet, Tensilica generated all six processors from the configurable Xtensa 6 and Xtensa LX cores, using the same development tools available to customers. Some features in the Diamond cores are point-and-click configuration options in those tools. In other cases, Tensilica's engineers created custom extensions using Tensilica Instruction Extension (TIE) language, a proprietary hardware description language (HDL) resembling Verilog.

All Diamond cores share the same basic Xtensa architecture. It's a 32-bit RISC architecture with shortened 24-bit instructions that conserve memory. For even greater code density, most 24-bit instructions have 16-bit alternatives, with modeless switching between the 16- and 24-bit subsets. Software written with the standard instruction set is binary compatible with all Xtensa 6, Xtensa LX, and Diamond processors. However, each Diamond core has additional instructions that vary across the product line. Tensilica provides a customized C/C++ compiler, assembler, debugger, profiler, simulator, and other software-development tools, along with an Eclipse-based integrated development environment (IDE).

The Xtensa 6 and Xtensa LX are closely related microarchitectures that have nearly identical five-stage pipelines and I/O interfaces. The Xtensa 6 is the newer model, introduced last fall. (See the sidebar, "Tensilica Introduces Xtensa 6 Processor Core," in *MPR 11/28/05-01*, "Tensilica Previews Video Engine.") The Xtensa LX made its debut in 2004. (See *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.") Each Xtensa core has some optional features unavailable for the other core, which is why one of the new Diamond cores is based on the Xtensa 6 and the others use the Xtensa LX.

Tensilica based the Diamond 232L on the Xtensa 6 because that configurable core has an optional memory-management unit (MMU)—a feature unavailable with the Xtensa LX. Consequently, the 232L is the only Diamond core with an MMU, which allows it to run more-sophisticated operating systems, such as MontaVista Linux. Other Diamond cores have a region-protection unit (RPU), which is Tensilica's variation of a memory-protection unit (MPU). The RPU allows programmers to protect memory regions of variable sizes. Although this RPU lacks the virtual-memory addressing of a full-fledged MMU, it's capable of supporting a real-time operating system (RTOS), such as Mentor/ATI's Nucleus Plus.

The higher-end Diamond cores—the 570T, 330HiFi, and 545CK—are extensions of the Xtensa LX. This was necessary because the Xtensa LX has two optional features unavailable for the Xtensa 6: Flexible-Length Instruction Xtensions (FLIX) and Tensilica's Vectra LX DSP engine. FLIX adds long instruction words to the Xtensa architecture, much like the bundled instructions in a VLIW processor.

(See *MPR 11/25/02-06*, "FLIX: The New Xtensa ISA Mix.") All three of the higher-end Diamond cores use FLIX, although the implementations vary.

The only Diamond core with a Vectra LX DSP engine is the powerful 545CK, which aced the BDTI DSP Kernel Benchmarks. As implemented in the 545CK, Vectra LX is an 18-bit vector DSP engine with versatile SIMD instructions. The Diamond 330HiFi is another special case—it's the only Diamond core with Tensilica's HiFi-2 extensions for digital-audio processing. HiFi-2 includes a 24-bit DSP engine that improves on the original HiFi-1 engine introduced in 2003. (See *MPR 9/29/03-01*, "Tensilica Makes Music.") This makes the Diamond 330HiFi core ideal for portable MP3 players and Voice over Internet Protocol (VoIP). Table 1 compares the features of all six new Diamond cores.

Be Wary of Area and Power Comparisons

Throughout this article, *MPR* compares Tensilica's Diamond cores with similar processor cores from ARC, ARM, and MIPS. As with all comparisons of synthesizable processor cores, we rely on the vendor's die-area and power-consumption estimates, which the vendors derive from gate-level simulations, not from production silicon. Their estimates can vary widely, depending on the layout efficiency, the physical-IP library they used for logic synthesis, the target fabrication process, and other factors. Those factors can vary from one vendor to another, and vendors don't always specify all the factors they use. As always, regard these die-area and power-consumption comparisons as rough estimates, not as gospel truth.

Tensilica's estimates for Diamond cores are fairly conservative. Die-area estimates are post-layout extractions that include the clock tree, scan, and power rails, and they assume synthesis for maximum clock frequency, not minimum area. Tensilica says its die-area estimates assume routing efficiencies of 85% for the 108Mini, 212GP, and 232L; 65% for the 570T and 330HiFi; and 50% for the 545CK. Developers should have little trouble achieving those targets.

Tensilica bases its power-consumption estimates on post-route layouts synthesized for the maximum clock frequency, using Artisan Sage-X libraries under typical conditions while running typical workloads. Tensilica says it derives those workloads from real-world applications, not just from Dhrystone benchmarks. Using different physical libraries under ideal conditions, Tensilica says it could reduce power by as much as 75% in some cases.

ARM usually measures power consumption by running Dhrystone 2.1 benchmarks and real-world code on post-layout simulations under typical conditions. For internal testing, ARM uses EEMBC benchmark suites to a much greater degree than its rarely published EEMBC scores would imply. (ARM is more bashful about publishing certified EEMBC scores than Tensilica is.)

Like Tensilica, ARC measures power on post-layout gate-level simulations after inserting the clock tree and other circuits. ARC uses 3D extraction techniques and also

Feature	Tensilica Diamond 108Mini	Tensilica Diamond 212GP	Tensilica Diamond 232L	Tensilica Diamond 570T	Tensilica Diamond 330HiFi	Tensilica Diamond 545CK
Core Features						
CPU Core	Xtensa LX	Xtensa LX	Xtensa 6	Xtensa LX	Xtensa LX	Xtensa LX
Instr. Lengths	16/24 bits	16/24 bits	16/24 bits	16/24/64 bits	16/24/64 bits	16/24/64 bits
Pipeline Type	Uniscalar	Uniscalar	Uniscalar	Uniscalar + 3x FLIX	Uniscalar + 2x FLIX	Uniscalar + 3x FLIX
Pipeline Depth	5 stages	5 stages	5 stages	5 stages	5 stages	5 stages
GPRs	32	32	32	32	32	64
Vector Regs.	—	—	—	—	8 x 48 bits 4 x 56 bits	16 x 160 bits
DSP Engine	—	—	—	—	HiFi-2, 24 bits	Vectra LX, 18 bits
ALUs	1	1	1	3	2	3
Branch Units	1	1	1	2	1	1
Multipliers	—	1 x 16 bits	1 x 16 bits	1 x 32 bits 1 x 16 bits	1 x 24 bits	8 x 18 bits
Zero-Overhead Looping	—	Yes	Yes	Yes	Yes	Yes
Mem. Manager	RPU	RPU	MMU	RPU	RPU	RPU
Viterbi Unit	—	—	—	—	—	1
Core Freq*	233–250MHz	233–250MHz	200–233MHz	200–233MHz	200–233MHz	200–233MHz
Core Size*	0.46mm^2 47k gates	0.70mm^2 73k gates	0.80mm^2 84k gates	1.46mm^2 114k gates	1.86mm^2 142k gates	5.14mm^2 310k gates
Power/MHz*	0.11mW	0.195mW	0.212mW	0.275mW	0.255mW	0.281mW
Dhrystone 2.1	1.2DMIPS/MHz	1.3DMIPS/MHz	1.3DMIPS/MHz	1.52DMIPS/MHz	1.3DMIPS/MHz	1.3DMIPS/MHz
Instruction Extensions						
Specialized DSP Instructions	—	—	—	—	Yes (audio)	Yes (Vectra LX)
Single-Cycle MAC	—	Yes	Yes	Yes	No	No
Sign Extend	Yes	Yes	Yes	Yes	Yes	Yes
Min/Max	Yes	Yes	Yes	Yes	Yes	Yes
Normalized Shift	Yes	Yes	Yes	Yes	Yes	Yes
Viterbi	—	—	—	—	—	Yes
Caches and Local Memory						
I-Cache (Associativity)	—	8KB 2-way	16KB 4-way	16KB 2-way	4KB 2-way	—
D-Cache (Associativity)	—	8KB 2-way	16KB 4-way	16KB 2-way	8KB 2-way	—
Instr. RAM †	0–128KB	0–128KB	—	0–128KB	0–128KB	0–128KB
Data RAM †	0–128KB, dual	0–128KB, single	—	0–128KB, single	0–128KB, dual	0–128KB, dual
Datapath Width	32 bits	32 bits	32 bits	64 bits	64 bits	128 bits
Input/Output Interfaces and Load/Store Units						
System (PIF) + Bus Bridge	32 bits AHB Lite ‡	32 bits AHB Lite ‡	32 bits AHB Lite ‡	64 bits AHB Lite ‡	64 bits AHB Lite ‡	128 bits AHB Lite ‡
XLMI Bus	—	Yes	—	Yes	—	—
32-Bit I/O Ports	Yes	Yes	—	Yes	—	—
32-Bit I/O Queues	—	—	—	Yes	Yes	Yes
Load/Store Units	1 x 32 Bits	1 x 32 Bits	1 x 32 Bits	1 x 64 Bits	1 x 64 Bits	2 x 128 bits
Miscellaneous Features						
Ext. Interrupts	9	9	9	9	9	9
Timer Interrupts	3	3	3	3	3	3
S/W Interrupts	2	2	2	2	2	2
NMI	Yes	Yes	Yes	Yes	Yes	Yes
On-Chip Debug	Yes	Yes	Yes	Yes	Yes	Yes

Table 1. Most of Tensilica's new Diamond Standard Series cores use the Xtensa LX configurable-processor core, but the 232L uses the newer Xtensa 6 core, which has a memory-management unit (MMU). The Xtensa LX manages memory with a region-protection unit (RPU), which cannot support virtual-memory operating systems. All these cores are 32-bit processors with 24- and 16-bit instruction sets. *Clock frequencies and power-consumption estimates assume a generic 0.13-micron fabrication process under worst-case conditions. †User-configurable Diamond feature. ‡Optional Diamond feature.

calculates parasitic capacitance using lookup tables based on conservative models. Dynamic power, switching power, and static leakage all figure into ARC's measurements. ARC says it exercises the processor with realistic workloads during these tests. Differences between workloads and different assumptions about logic synthesis probably explain why ARC's power-consumption estimates are often lower than Tensilica's, even for processor cores with similar gate counts.

Challenging the Ubiquitous ARM7

By far the most popular 32-bit processor-IP core on the market is the ARM7TDMI, which ARM offers in both hard and soft formats. It's a small, cacheless core with a simple three-stage pipeline, and it's been an industry mainstay for 10 years. The ARM7's popularity and graybeard seniority make it an attractive target for rivals like Tensilica. In particular, Tensilica would like to win more designs in 32-bit microcontrollers, a popular vehicle for the ARM7.

Hence the Diamond 108Mini, which Tensilica positions hopefully as an ARM7 killer. Like the ARM7TDMI, the 108Mini is a small, cacheless core with few frills. By dispensing with caches, the 108Mini can operate deterministically in hard real-time systems. Instead of caches, the 108Mini has user-configurable local memories for instructions and data. Developers can add one bank of instruction memory (up to 128KB) and one or two banks of data memory (up to 128KB each). The core has one input port and one output port, each 32 bits wide, which can be subdivided into general-purpose I/O (GPIO) ports. A 32-bit AMBA-compatible AHB-Lite bridge is optional.

Without memories, the 47,000-gate 108Mini occupies a mere $0.46mm^2$ of silicon when fabricated in a generic 0.13-micron CMOS process. Its maximum worst-case clock frequency is 233–250MHz at 1.2V, and power consumption is about 0.11mW per megahertz, or 25.6mW at the maximum clock speed. (In a low-voltage 0.13-micron process, of course, the 108Mini can do a little better.) Performance is about 1.2 Dhrystone MIPS per megahertz.

The Diamond 108Mini is significantly faster than the synthesizable ARM7TDMI-S—which strains to reach 146MHz under the same conditions—but is also 84% larger and consumes 10% more power. (The 108Mini consumes almost twice as much power as the hard-core ARM7TDMI.) However, the 108Mini has several tangible advantages: three timers (the ARM7 has none), memory protection (missing from the ARM7), better I/O capabilities (GPIO and AHB-Lite), and better interrupts. The interrupt structure should be of particular interest to developers building real-time systems. Whereas the ARM7 supports only three interrupts, none of them nonmaskable, the 108Mini supports 15 interrupts and nonmaskable interrupts (NMI).

Tensilica also compares the Diamond 108Mini to the more powerful ARM968E-S, ARM's smallest ARM9-family core. In this matchup, the 108Mini consumes less power and silicon while reaching similar clock speeds, and it retains the same advantages with interrupts. But within days of Tensilica's Diamond introduction, ARM announced that it is shipping the ARM996HS, the first commercially available 32-bit processor core implemented in asynchronous (clockless) logic. This breakthrough processor consumes only about half as much power as the 108Mini and has larger configurable local memories, an MPU, dual AHB-Lite buses, NMIs, and very low electromagnetic emissions. Although the ARM996HS is about twice as large as the 108Mini, its unique properties make it a formidable new competitor.

Other horses racing against the Diamond 108Mini include ARC's preconfigured derivatives of the ARC 600. The smallest of those derivatives is the cacheless ARC 605, which reaches the same clock speeds as the 108Mini but is significantly smaller ($0.31mm^2$ vs. $0.46mm^2$) and consumes about half as much power (0.06mW per megahertz vs. 0.11mW per megahertz). Another cacheless derivative is the ARC 610D, which is larger than the 108Mini ($0.64mm^2$) but still consumes less power (0.07mW per megahertz)—and the ARC 610D has some DSP extensions that are missing from the 108Mini.

Wrestling With the ARM9

ARM9-family processor cores are nearly as popular as the ARM7TDMI and more powerful. Tensilica has two Diamond cores in the same general class: the 212GP and 232L. Both offer similar features, with competitive clock speeds and power consumption. The main differences between these processors and the 108Mini are caches and DSP extensions.

Tensilica describes the Diamond 212GP as a midrange controller core. It drops the RPU found in the 108Mini but adds L1 caches, 16-bit DSP extensions, and a special on-chip I/O interface. Each cache is 8KB and two-way set-associative; local scratchpad memories are optional and can range up to 128KB in size. DSP extensions include a 16-bit multiply-accumulate (MAC) unit and a few extra instructions. These DSP extensions aren't nearly as capable as Tensilica's Vectra LX DSP engine, but they are sufficient for light-duty signal processing and resemble the DSP extensions in most ARM9-family cores, ARC's preconfigured cores, and the MIPS32 24KE. To provide on-chip I/O, the 212GP has a 128-bit Xtensa Local Memory Interface (XLMI), which supports single- or multicycle access to on-chip memory, coprocessors, and custom logic.

At $0.70mm^2$ (0.13 micron), the Diamond 212GP is smaller than all ARM9 cores except the ARM968E-S. It consumes less power (0.195mW per megahertz) than all ARM9 cores except the asynchronous ARM996HS (0.045mW per megahertz). Maximum clock speeds are in the same range (233–250MHz). In addition, the 212GP has the same advantages of interrupts, timers, and I/O interfaces that the Diamond 108Mini enjoys over ARM7 cores. On balance, the Diamond 212GP is tough competition for the ARM9 family. It's also smaller and more power-miserly than the MIPS32 4KE. However, ARC's preconfigured cores are stiffer competition: all six ARC 600 and ARC 700 derivatives consume less power than the 212GP, and four of them are the same size or smaller.

The next-higher Diamond Series core is the 232L, which makes some interesting trade-offs against the 212GP. At $0.80mm^2$ and 0.212mW per megahertz, the 232L is only a trifle larger and more power hungry than the 212GP, but it has a feature unique to the Diamond series: an MMU. This allows the 232L to run MontaVista Linux. It also has larger caches: 16KB each for instructions and data, twice as large as the 212GP's caches. But scratchpad memory isn't an option, and Tensilica also omitted the XLMI and 32-bit I/O ports.

Otherwise, the 232L is much like the 212GP, including the same DSP extensions.

As the only Diamond processor with an MMU, the 232L competes directly with the ARC 750D, the ARM926EJ-S, and the MIPS32 4KE, which also have MMUs. Tensilica's processor is the smallest in that group, but the ARC 750D consumes less power (0.13mW per megahertz). All these cores have similar DSP extensions, and the ARM926EJ-S has ARM's Jazelle extensions for Java acceleration. The ARC 750D can reach the highest clock speed—533MHz, thanks to a deeper seven-stage pipeline—whereas the other processors are limited to 233–266MHz (0.13 micron). These four processors have so much in common that choosing among them will probably come down to evaluating their biggest differences or their smallest differences. The biggest differences are their CPU architectures; the smallest differences are things like individual DSP instructions and execution latencies for application-critical operations.

Outreaching the ARM10 and ARM11

As mentioned above, Tensilica's Diamond 570T, 330HiFi, and 545CK processors are customized versions of the Xtensa LX core, which has optional FLIX extensions. FLIX allows a compiler to pack multiple operations into a 64-bit-long instruction word. At run time, the processor can execute two or more of these operations simultaneously if they are nondependent and dispatched to different function units. Although Tensilica sometimes describes this capability as "static superscalar," the processor actually has a uniscalar pipeline, not superscalar pipelines. FLIX is more like an abbreviated version of VLIW adapted to a conventional RISC architecture. A program can modelessly mix the 64-bit FLIX instructions with normal 16- and 24-bit Xtensa RISC instructions in the same stream.

FLIX is a highly customizable option with Tensilica's processor-configuration tools, so specific implementations vary. The Diamond 570T and 545CK processors can pack three FLIX operations into a 64-bit instruction word, whereas the Diamond 330HiFi can pack two FLIX operations per word. Those differences, as well as DSP extensions and function units, are the main features distinguishing the Diamond 570T, 330HiFi, and 545CK cores from each other.

Tensilica aims the Diamond 570T squarely at the ARM10 and ARM11 families. The 570T has 16KB instruction and data caches and the same DSP extensions as the Diamond 232L. Separate scratchpad memories for instruction and data are optional (0–128KB). It's the only Diamond core with a 16- and 32-bit multiplier, which supplements the 16-bit multiplier found in the 212GP and 232L. The 570T has a wider system interface than lower-end Diamond cores (64 bits vs. 32 bits), and it has the same XLMI and 32-bit I/O interfaces as the 212GP. Like other Diamond cores based on the Xtensa LX, the 570T has special I/O queues (FIFO buffers) that help relieve bottlenecks on the 32-bit I/O port. (For a detailed description of these TIE ports and queues, see *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.")

To take advantage of FLIX, the 570T has two additional ALUs (for a total of three) and an additional branch unit (for a total of two). In combination with its dual multipliers, these function units allow the 570T to execute as many as three FLIX operations per clock cycle, which may include one DSP operation. No other licensable 32-bit embedded-processor core has these capabilities.

At 1.46mm^2 in a 0.13-micron process (excluding memories), the Diamond 570T is half the size of the ARM1136J-S (2.85mm^2). And the 570T consumes less than half as much power (0.275mW per megahertz vs. 0.6mW per megahertz). However, the ARM core has a few useful features missing from Tensilica's core, such as Java extensions, a DMA controller, and an MMU. ARM also offers the ARM1136JF-S, a slightly larger version of the same core with a vector floating-point coprocessor. Freescale Semiconductor chose to integrate that core in the i.MX31 multimedia applications processor, one of the few ARM-based processors for which there are certified EEMBC benchmark scores. Because Tensilica has benchmarked the Diamond 570T, it's possible to compare it with the i.MX31 and the ARM1026EJ-S, an ARM10-family core with certified EEMBC scores. Table 2 shows the results.

In reality, the ARM10- and ARM11-family processors can do a little better than their published EEMBC scores indicate. ARM says that by using a speedier version of the TSMC 0.13G process and Sage-HS libraries, the ARM1026EJ-S can reach 317MHz, and the ARM1136JF-S can reach 400MHz. Under those conditions, the former processor would be about 16% faster and the latter processor about 50% faster. Also, Freescale benchmarked the ARM1136JF-S after compiling the EEMBC kernels with a GNU compiler, which isn't as efficient as the C compiler in the latest version of ARM's RealView Developer Suite. According to ARM, compiling with RealView would gain another 48%.

An Audio Processor for High Fidelity

The most application-specific processor in the Diamond Standard Series is the 330HiFi, which targets digital audio.

EEMBC Suite	ARM ARM1026EJ-S (266MHz)	ARM ARM1136JF-S (266MHz)	Tensilica Diamond 570T (233MHz)
Networking 1.1	4.4	3.0	7.6
Consumer	19.5	13.7	34.0
Office Automation	202.1	151.8	244.7
Telecom	3.2	2.5	6.1
Normalized Geo Mean	1.4	1.0	2.2

Table 2. In these four EEMBC benchmark suites, Tensilica's Diamond 570T core outran the ARM1026EJ-S and ARM1136JF-S cores. ARM benchmarked the ARM1026EJ-S as a soft core, using a cycle-accurate simulator, as Tensilica did with the 570T. The ARM1136JF-S scores are from Freescale's benchmark tests of the i.MX31 multimedia applications processor, using production silicon. All scores are EEMBC "out-of-the-box" results. *MPR* has extrapolated scores for the simulated processors to their maximum worst-case clock frequencies in a 0.13-micron process. For EEMBC certification, Tensilica estimated a faster clock speed (526MHz) in a 90nm process.

It's based on the Xtensa LX core and Tensilica's HiFi-2 audio-DSP engine, which improves on the original HiFi-1 engine. (See *MPR 9/29/03-01*, "Tensilica Makes Music.")

Unlike some other audio processors, the HiFi-2 engine can process audio signals with 24 bits of precision instead of 16 bits. The extra precision helps preserve the accuracy of intermediate calculations and is commonly used for such audio-processing tasks as volume control, loudness compensation, frequency-band equalization, reverb effects, and enhanced stereo synthesis. The difference may not be audible to everyone, but it makes the 330HiFi particularly well suited for high-fidelity digital-audio systems. The 330HiFi can also process signals at 8- or 16-bit resolution for less demanding applications, such as digitized speech.

To support audio processing, the 330HiFi has two special register files, in addition to the usual set of 32 general-purpose registers. One register file has eight 48-bit registers, and the other has four 56-bit registers. These extra-wide registers store operands for vector operations and allow the 330HiFi to process audio signals without clipping the peaks. Special instructions can operate directly on 24-bit data. The 24-bit MAC unit is pipelined, so it can issue a result on every clock cycle, despite having a two-cycle execution latency. The 330HiFi supports FLIX, too, although it packs only two operations per 64-bit instruction word, not three operations per word as the 570T and 545CK do.

At 1.82mm^2 in a 0.13-micron process (excluding memories), the 330HiFi is the second-largest Diamond processor core. Nevertheless, it's smaller than a typical ARM11-family core and even some ARM9-family cores. And it consumes only 0.255mW per megahertz, which is ARM9 country. In a real-world system, the 330HiFi could

save more power than Tensilica's milliwatts-per-megahertz estimate suggests, because the powerful HiFi-2 engine can process digital audio at a lower clock frequency than an unmodified general-purpose processor can.

One foe that might give the Diamond 330HiFi a run for the money is the ARC 600 Digital Audio Platform. This hardware/software extension package combines some of ARC's DSP extensions with 16 custom instructions and software codecs. Total size, including the ARC 600 processor core, is a mere 50,000 gates, compared with 142,000 gates in the 330HiFi. (See *MPR 12/15/03-01*, "ARC Alters Trajectory.") But the 330HiFi has more special instructions and registers than the ARC 600 audio package does.

Tensilica's 'DSP' Sets a New Record

The highest-end core in Tensilica's Diamond Standard Series is the awesome 545CK. Tensilica describes it as a vector DSP, even though it's based on the same general-purpose RISC core (Xtensa LX) as the Diamond 570T and 330HiFi. Nevertheless, the description is apt. Augmented by a customized version of Tensilica's Vectra LX DSP engine, FLIX, and other extensions, the 545CK outran every licensable DSP or general-purpose processor core ever benchmarked by BDTI. Figure 1 shows BDTI's benchmark results.

The Vectra LX DSP engine is Tensilica's largest extension package for the Xtensa LX. Normally, it has four 16-bit multipliers for MAC instructions. As implemented in the Diamond 545CK, it has eight 18-bit multipliers and 16 vector registers, each 160 bits wide. Vector registers are 160 bits wide because the ALUs can add and subtract with 20-bit precision, so each register can hold eight operands. MACs have an execution latency of two cycles but are pipelined for single-cycle throughput. In addition, the 545CK has twice as many 32-bit general-purpose registers as any other Diamond core—64 in all.

The 545CK has the same DSP instructions as most other Diamond cores have plus more than 200 DSP instructions for the Vectra LX engine. The FLIX implementation in the 545CK can pack three operations into a 64-bit instruction word. As if all that weren't enough, the 545CK is the only Diamond core with a special Viterbi unit. Supported by five custom instructions, it accelerates the Viterbi error-correction algorithms commonly used in communications.

To ensure determinism, the 545CK has no instruction or data caches. Instead, it fetches instructions and data from local scratchpad memories, which are variable in size up to 128KB. Data RAM can be dual banked, just like the X and Y data memories in dedicated DSPs. There are two load/store units with 128-bit-wide I/O interfaces, and each unit can access either bank of data memory as well as anything attached to the PIF bus. As a result, the 545CK can transfer eight 16-bit operands to or from each bank of data RAM on every clock cycle while simultaneously fetching CPU, DSP, or FLIX instructions from local instruction RAM. This is a prodigious amount of on-chip bandwidth, easily exceeding the capacity of conventional 16-bit DSPs and 32-bit RISC processors with DSP extensions.
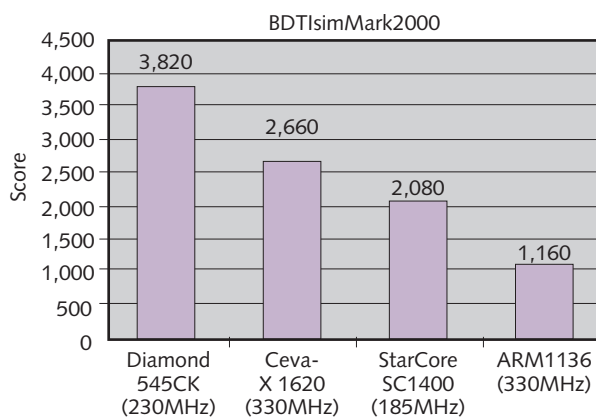
BDTIsimMark2000

Core	Score
Diamond 545CK (230MHz)	3,820
Ceva-X 1620 (330MHz)	2,660
StarCore SC1400 (185MHz)	2,080
ARM1136 (330MHz)	1,160

Figure 1. When is a CPU a DSP? When it humbles DSPs by posting better signal-processing benchmark scores. Berkeley Design Technology (BDTI) tested a cycle-accurate simulation of Tensilica's Diamond 545CK processor and found that it outperformed every other licensable DSP core, as well as other CPU cores with DSP extensions. BDTIsimMark2000 is a summary measure of signal-processing speed. All simulations use worst-case clock speeds for the TSMC CL013G process and the ARM Artisan Sage-X library. For more information and scores see *www.BDTI.com*. (Scores copyright 2006 by BDTI.)

Naturally, there's a price to pay for all those features. The 545CK is by far the largest Diamond Standard Series processor core: 310,000 gates, requiring 5.14mm^2 of silicon (excluding memories) in a generic 0.13 micron process. Maximum worst-case clock frequency in that process is about 210MHz. In TSMC's 0.13-micron LVLK-OD process, the die area shrinks to 3.7mm^2, and the maximum worst-case clock frequency is 381MHz—which demonstrates how widely the performance of a synthesizable processor can vary, depending on the target process.

Dynamic power consumption for the 545CK is surprisingly low: 0.281mW per megahertz in the generic 0.13-micron process (but 0.53mW per megahertz in the LVLK-OD process). The former estimate is lower than the power consumption of some 32-bit RISC cores that have much less capable DSP extensions. For example, the ARM1136J-S and MIPS32 24KE consume at least twice as much power as the 545CK, and their DSP extensions aren't in the same league. ARC's best preconfigured CPU/DSP, the ARC 750D, has better DSP extensions than most RISC processors and consumes only 0.13mW per megahertz, but it's still not as powerful as the 545CK.

Two factors probably explain the 545CK's parsimonious power consumption. One is that Tensilica's design tools use extensive fine-grain clock gating. Another is that Tensilica's workloads for power measurements don't vigorously exercise the Viterbi unit or all eight multipliers, which account for a significant portion of the 545CK's logic gates. Tensilica considers its test workloads realistic, but your mileage may vary.

A major advantage of all DSPs based on general-purpose processor cores is that programmers need only one tool chain. They can write DSP code using the same compiler or assembler they use for conventional code. The processor handles all the code as a common instruction stream, dispatching instructions of each type to the appropriate function units. This unified approach to software development can save time, cut costs, and reduce time to market.

Preconfigured Cores Should Be a Hit

Tensilica was founded in 1997 on the principle of configurable processor cores and pitches itself as "the configurable-processor company." But business models and marketing strategies are configurable, too. *MPR* sees the Diamond Standard Series as an extension of Tensilica's strategy, not as a departure forced by technical roadblocks or market resistance. Although Tensilica remains a privately held company with opaque finances, the configurable Xtensa cores continue to attract licensees and win designs, so we doubt the preconfigured cores were born of desperation.

Offering the option of preconfigured cores simply makes sense. A common theme of our frequent coverage of configurable-processor technology is that hardware is following

the same evolutionary path as software. Over the years, software developers have progressed from flipping toggle switches to writing assembly code to using high-level compilers. Today's programmers rely heavily on prewritten class libraries and software components. The overall trend is toward greater automation and higher levels of abstraction above the metal.

Hardware developers are tracking the same course, in their own ways. Hard-wired discrete components led to circuit-design tools, then to high-level HDLs. Tensilica's processor-configuration tools take another big step (see *MPR 7/12/04-01*, "Tensilica's Automaton Arrives"), but some developers just want something ready to use. Preconfigured cores are like class libraries. They are prewritten, preverified components, ready for integration into a development project.

If Tensilica wished, it could carry our class-library analogy much farther. The Xtensa architecture is so flexible, and the configuration tools so versatile, that Tensilica could generate hundreds, or even thousands, of preconfigured cores to meet almost every conceivable need. There could be as many processors in the Tensilica product catalog as there are classes in the Microsoft Foundation Classes. But customers would find the catalog overwhelming (not to mention the strain on Tensilica's tech writers and marketers). Six preconfigured cores are a good start. We expect to see more in the future.

When Tensilica and its foundry partners turn these preconfigured soft cores into prehardened firm cores, Tensilica will have more latitude to pursue customers in China and other developing markets, where IP is less secure. Even in established markets, some chip developers prefer to license all their IP directly from a foundry instead of dealing with individual IP vendors. Firm cores licensed by foundry partners will suit those customers, too. ARM and MIPS have successfully executed a similar strategy for years. As long as Tensilica can adequately support the number of processor cores it introduces, there is no downside to this strategy, and the upside potential is great. ◇