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FREESCALE STRENGTHENS POWER.ORG

Reunited Alliance With IBM Plans the Future of the Power Architecture

By Tom R. Halfhill {3/6/06-01}

Freescale Semiconductor's long-awaited decision to join Power.org strengthens the industry alliance and will help chart the course of the Power Architecture—just in time. Recent moves by ARM, Intel, MIPS Technologies, and Sun Microsystems are strengthening the competition, too.

Power.org is an open industry consortium with more than 40 corporate members. Its mission is to coordinate the future evolution of the Power Architecture, more commonly known as PowerPC. In 2004, when IBM formed Power.org, the most conspicuous absentee among the 15 founding members was Motorola spinoff Freescale. (See *MPR 12/27/04-02*, "Bringing Power to the People.")

IBM and Motorola jointly developed the PowerPC architecture in 1991 but drifted apart in later years as each company pursued different markets and directions. Although they collaborated on an important update to the architecture in 1999 (see *MPR 5/10/99-02*, "PowerPC Architecture Gets Makeover"), their rift seemed to grow worse afterward.

Now the companies appear to have reconciled. Freescale has joined Power.org as a "founding member" (an odd honor for a latecomer) and is also joining IBM in a new group, the Power Architecture Advisory Council (PAAC). PAAC is an invitation-only committee that so far consists of only two members: IBM and Freescale.

Actually, PAAC isn't entirely new. The organizational plan for Power.org always envisioned a group like PAAC, but IBM needed a Power architectural licensee to participate. Freescale fits the bill.

The emergence of PAAC and its exclusive membership pose a question: Is it, in effect, Superpower.org? Or, to use a United Nations analogy, is PAAC the Security Council to Power.org's General Assembly?

PAAC Controls the Core Architecture

To understand how much power Power.org will actually wield over Power, *MPR* asked Freescale to explain the Power.org org chart. It looks like this: the Power.org Technical Committee will be responsible for developing system-level standards that help promote the Power Architecture. For instance, the committee's purview includes on-chip buses, system-level programming models, and system reference platforms, which in turn influence operating systems, device drivers, and development tools.

Meanwhile, PAAC will be responsible for developing the Power instruction-set architecture (ISA) and, particularly, anything affecting the opcode map or programmer's model. Power.org can advise PAAC on these matters—there will be a formal procedure for providing input—but PAAC retains final authority over the vital parts of the ISA.

In short, the U.N. analogy is pretty close, except that PAAC currently doesn't have rotating members from Power.org as the Security Council does from the General Assembly. (Also, the members of Power.org have somewhat less history of open warfare than members of the U.N. do.)

As an example of why Power.org needs something like PAAC, consider Freescale's signal-processing extensions to the PowerPC architecture. In 2001, Freescale created a new PowerPC auxiliary processing unit (APU) known as the Signal Processing Engine (SPE). (See *MPR 7/16/01-01*, "Speedier BookE Encore," and *MPR 8/12/02-01*, "Motorola's Embedded PowerPC Story.") Don't confuse Freescale's SPE with

For More Information

For more information about the Power.org alliance, visit *www.power.org*. For more information about the Power Architecture, visit *www-128.ibm.com/developerworks/power/newto/* and *www.freescale.com/powerarchitecture*.

IBM's completely different SPE (Synergistic Processor Element) in the Cell Broadband Engine processor, which IBM introduced last year. (See *MPR 2/14/05-01*, "Cell Moves Into the Limelight.") Acronym collision is only one reason that IBM and Freescale need PAAC.

The larger reason for PAAC is architectural coordination. Freescale's SPE is a two-way SIMD engine found only in Freescale's PowerPC e200 and e500 cores. It's less capable than AltiVec, but it also requires less silicon, partly because it shares the general-purpose registers instead of defining new registers. However, Freescale's SPE defines 222 new instructions, which required a fairly large piece of the PowerPC opcode map. Although Freescale consulted with IBM to ensure that the new instructions wouldn't conflict with any IBM plans for the same opcodes, the extensions amount to a proprietary appendage to the architecture—no one else has implemented them. Both Freescale and IBM would like to cooperate more fully on future extensions. Hence the need for PAAC.

Growing Competition for PowerPC

Another good reason for détente between IBM and Freescale is the growing threat of competition from ARM, Intel, MIPS, and Sun. All four companies compete with PowerPC for some of the same territory in the embedded-processor market.

ARM, the perennial leader in low-power embedded-processor cores, is now reaching for higher performance with its Cortex-A8. This is ARM's first superscalar processor core, and it has powerful Neon media extensions. ARM designed the Cortex-A8 primarily for the demanding workloads in next-generation cellphones. (See our two-part coverage in *MPR 10/25/05-02* and *MPR 11/14/05-01*, "Cortex-A8: High Speed, Low Power.")

Although the Cortex-A8 isn't powerful enough to threaten the highest-end PowerPC processors found in servers and routers, it does extend ARM's reach into a segment of the embedded-processor market that IBM and Freescale covet. So does the powerful Feroceon processor that ARM licensee Marvell announced last year. Feroceon is the first ARM-compatible chip with out-of-order execution. (See *MPR 5/23/05-01*, "Marvell Puts ARM Out of Order.")

Intel is on the move, too. The leading PC-processor vendor is developing a new generation of lower-power x86 chips capable of competing head-to-head with embedded processors for sockets in consumer-electronics products and palmtop computers. At last fall's Intel Developer Forum, the company revealed that future embedded x86 processors will use the Intel next-generation microarchitecture (iNGM) to slash power consumption below one watt. (See *MPR 9/12/05-01*, "IDF Fall 2005: More Cores, Less Power.")

Another company introducing a new power-efficient microarchitecture is MIPS. In February, MIPS announced the MIPS32 34K—the world's first licensable processor core with simultaneous multithreading. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.") Historically, MIPS has staked out higher-performance ground than ARM has, but now both companies are introducing new power-efficient processors for strenuous embedded applications. IBM and Motorola/Freescale have been pushing PowerPC into the same spaces since at least 1993, when Motorola introduced the first PowerQUICC communications processor.

Even Sun is making interesting moves. This spring, Sun will release the complete RTL model of its new multithreaded, multicore UltraSPARC T1 (Niagara) processor to anyone who wants it. Although no one will likely use the model to produce clone chips, the open-source license could spur new interest in the lonely SPARC architecture and inspire developers to carve smaller processors out of the RTL. (On the other hand, Sun's similar release of the MicroSPARC RTL in 1999 generated few sparks.) IBM offers downloadable Open SystemC models of the PowerPC 405 and PowerPC 440 embedded-processor cores, but users must buy a conventional license to proceed with commercial development.

The Power Architecture is already pervasive in embedded systems, having made significant inroads into automotive, networking, telecommunications, wireless infrastructure, storage, industrial control, video gaming, military, and aerospace applications. But ARM is more popular in low-power systems, especially cellphones, and MIPS is strongly entrenched in consumer electronics. By working together in Power.org, Freescale and IBM can coordinate their efforts with those of numerous other companies in the Power Architecture community. And by working together in PAAC, they can develop strategic roadmaps to assure developers that the architecture isn't static or in danger of fragmenting. Now that their old alliance appears whole again, IBM and Freescale can begin the real work. ◇