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CAN ARM BEAT THE CLOCK?

ARM Ships the First Licensable, Clockless 32-Bit Microprocessor Core

By Tom R. Halfhill {2/21/06-01}

ARM has finally delivered the ARM996HS, the first commercially available 32-bit microprocessor core implemented in asynchronous (clockless) logic. ARM's development partner is Netherlands-based Handshake Solutions, which helped bring the unconventional technology to fruition. If the ARM996HS succeeds, it could spark a revolution in power-efficient processing that researchers envisioned even before microprocessors were invented.

The first ARM996HS customer prefers to remain anonymous for now, but a good guess would be Philips Semiconductors. Philips is a longtime ARM licensee with a broad line of ARM7- and ARM9-based microcontrollers. Also, Philips and Handshake Solutions have the same parent company: Royal Philips Electronics. It would make sense for them to share the risk of the first ARM996HS development project.

And make no mistake, the project still has risks. Several previous attempts to introduce a clockless 32-bit microprocessor have failed—sometimes for technical reasons, sometimes for business reasons. Even the ARM996HS, which has a better chance of succeeding than any previous clockless processor, is reaching the market a year late. ARM originally intended to deliver the core early in 2005. (See *MPR 11/29/04-02*, "ARM's Asynchronous Handshake.")

Moreover, the ARM996HS remains unproved in silicon. ARM hopes to receive the customer's first engineering samples or to produce a small test chip by the end of this year. Until then, ARM and Handshake Solutions are evaluating the processor's performance and power consumption by running gate-level simulations using a post-layout netlist. They are also running verification and compatibility tests on a synchronous simulation of the processor in an FPGA.

Using gate-level Dhrystone 2.1 tests, ARM and Handshake Solutions provide the following performance estimates. Assuming worst-case conditions (1.08V, 125°C) for a generic 0.13-micron TSMC fabrication process (Artisan Sage-X library), the ARM996HS delivers 54DMIPS. That's about the same as a synchronous ARM968E-S processor core running at 50MHz. Under nominal conditions (1.2V, 25°C), the ARM996HS delivers 83DMIPS, about the same as an ARM968E-S at 77MHz. However, the asynchronous ARM996HS consumes only 35% as much power as the synchronous ARM968E-S under nominal conditions. Note that the ARM996HS and ARM968E-S have almost identical microarchitectures, and the latter processor is clock-gated to save power. Figure 1 compares their overall power consumption and their markedly different power signatures.

Obviously, the ARM996HS is not the first choice if the goal is high throughput. When fabricated in a 0.13-micron process, the conventional ARM968E-S can deliver 264DMIPS at its maximum worst-case clock frequency of 240MHz—a level of performance the ARM996HS cannot yet reach. But the ARM996HS is a power-efficient processor with extremely low electromagnetic emissions, and it is the first of its breed. It will almost certainly improve with further refinement.

Characterizing Performance Isn't Easy

The ARM996HS project is a difficult one that has faced many challenges. ARM intended to deliver the processor in 1Q05 but postponed delivery when early simulations missed the performance targets. Handshake Solutions explains that its

engineers had concentrated on verifying the processor's correctness at the expense of performance. After a year of additional work, both companies say that performance has improved significantly. It's not unusual for a new processor—even one using conventional logic—to require months of performance tuning.

Describing the performance of this processor is difficult, too. For one thing, the ARM996HS is clockless—which, of course, means that every part of the processor runs only as fast as it needs to run at any given moment, so there's no clock frequency to quote. In other words, shorthand expressions of performance in terms of clock speed are even more meaningless with the ARM996HS than they are with conventional microprocessors.

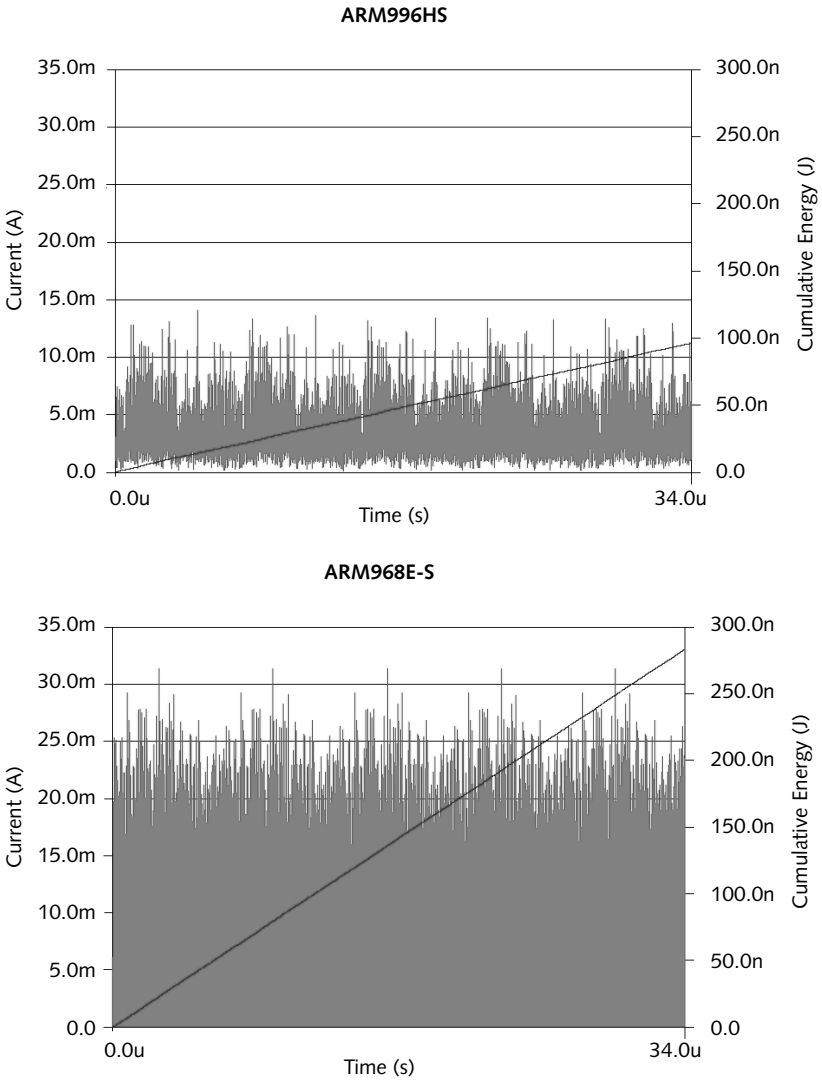

Figure 1. Development partners ARM and Handshake Solutions measured the power consumption of a clockless ARM996HS processor and a conventional ARM968E-S processor. Under typical conditions, the clockless core uses only 35% as much power overall, and its peak currents are dramatically lower. Both charts are based on post-layout gate-level simulations of the cores as synthesized for a 0.13-micron TSMC fabrication process.

Another obstacle to measuring performance is that good benchmarks (such as the EEMBC suites) run very slowly on gate-level simulators. Benchmarking the ARM996HS on higher-level simulators is impractical, because ARM doesn't deliver the core in customary soft form as a synthesizable Verilog or VHDL model. Instead, Handshake Solutions synthesizes the 89,000-gate processor using proprietary design tools created especially for clockless logic. Then ARM delivers the processor to licensees as a firm core—a gate-level netlist. The netlist works without further modification if customers use a standard-cell physical library from Artisan, such as one of the popular Sage or Advantage libraries. (ARM acquired Artisan in 2004.) If customers prefer a different library, Handshake Solutions needs a few days to resynthesize the core. Either way, after customers receive the netlist, they can use standard design-automation tools for further integration, layout, and verification.

To validate the ARM996HS, Handshake Solutions has implemented a synchronous simulation of the asynchronous processor in an FPGA, using the original functional description. (Handshake Solutions wrote the description in its own design language—called Haste—not in a standard language like Verilog or VHDL.) On every clock cycle, each link in the asynchronous logic chain can perform one handshaking event. Therefore, the datapaths of the clocked and clockless simulations are functionally equivalent, although their control circuits are different.

ARM says it has "very high confidence" in the FPGA simulation. So much confidence, in fact, that ARM is running surprising demos on the FPGA, such as ports of the PC games *Quake* and *Doom*. Of course, those 3D-graphics games aren't running at high PC frame rates. But, according to ARM, the FPGA simulation works correctly, right down to the JTAG interface, which allows the processor to generate scan tests and communicate normally with external debuggers.

Nevertheless, running and certifying EEMBC benchmark suites on the FPGA simulation or a gate-level simulator might be as excruciating as waiting for the first silicon to arrive. So for now, ARM is running smaller benchmark programs, such as the often-condemned but seemingly immortal Dhrystone. When the first ARM996HS-based chips become available, ARM plans to run some EEMBC benchmark kernels, although the company hasn't committed to certifying and publishing the scores. (Under EEMBC rules, vendors can't publicize uncertified scores, although vendors can share the scores with customers under nondisclosure agreements.)

ARM rarely publishes EEMBC scores for its other processors. *MPR* encourages ARM to be more forthcoming with the ARM996HS, because it's a unique and potentially revolutionary microprocessor. We believe the industry will remain skeptical of using asynchronous logic in mainstream designs until a clockless processor clearly proves itself in silicon and reduces the fear factor.

ARM996HS Resembles ARM968E-S

In most respects, the clockless ARM996HS resembles the ARM968E-S, a conventional ARM9E-family processor core introduced in 2004. As Table 1 shows, the ARM996HS also bears a family resemblance to the ARM966E-S, ARM946E-S, and ARM926EJ-S, all of which support the ARMv5TE or ARMv5TEJ instruction-set architectures (ISA). However, there are differences between the ARM996HS and other ARM9E-family processors that will matter to developers.

ARMv5TE is version 5 of the 32-bit ARM architecture. It's binary compatible with earlier ARM ISAs going back to the early 1990s. The "TE" suffix indicates support for ARM's subset of 16-bit Thumb instructions (unofficially known as Thumb-1 to distinguish it from the more recent Thumb-2) and 16-bit fixed-point DSP extensions. DSP extensions include a single-cycle 32- × 16-bit multiply-accumulate (MAC) unit and related instructions useful for saturating arithmetic and signal processing. Although the ARM996HS fully supports ARMv5TE, it doesn't support the newer ARMv5TEJ ISA, which adds ARM's Jazelle extensions for accelerating Java execution. Currently, the only ARM9 processor supporting ARMv5TEJ is the ARM926EJ-S. However, the ARM996HS supports some memory features of the newer ARMv6 ISA, such as 32-byte memory regions.

Unlike most other members of the ARM9E family, the ARM996HS lacks a coprocessor interface. Therefore, it can't use ARM's vector floating-point (VFP) coprocessor. The VFP coprocessor supports single- and double-precision floating-point math and complies with the IEEE 754 standard. VFP is an option for the ARM966E-S, ARM946E-S, and ARM926EJ-S.

There's no support in the ARM996HS for instruction or data caches, either, but that's not unusual for ARM9E processors—only the ARM926EJ-S and ARM946E-S have optional caches. Instead, the ARM996HS offers the option of tightly coupled memory (TCM) for instructions and data. TCMs serve essentially the same purpose as caches but are managed explicitly in software, not automatically by the processor. As a result, TCMs are more deterministic than caches and are better for real-time systems. Developers can add TCMs to the ARM996HS without using glue logic, and the core communicates with the memories using four-phase handshake signals.

The ARM996HS is only the second processor in the ARM9E family with a Harvard bus architecture. As the block diagram in Figure 2 shows, the ARM996HS has two separate AMBA AHB-Lite interfaces, each 32 bits wide. This allows the ARM996HS to simultaneously fetch instructions and data while avoiding bus conflicts. The only other core in

Feature	ARM996HS	ARM968E-S	ARM966E-S	ARM946E-S	ARM926EJ-S	ARM922T
ARM ISA	ARMv5TE	ARMv5TE	ARMv5TE	ARMv5TE	ARMv5TEJ	ARMv4T
Core Logic	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous	Synchronous
Core Freq*	n/a	240MHz	250MHz	210MHz	266MHz	250MHz
Core Type	Firm	Soft	Soft	Soft	Soft	Hard
Pipeline Depth	5 stages	5 stages	5 stages	5 stages	5 stages	5 stages
Thumb-1	Yes	Yes	Yes	Yes	Yes	Yes
DSP Extensions	Yes	Yes	Yes	Yes	Yes	—
VFP9 FPU	—	—	Optional	Optional	Optional	Optional
Java Extensions	—	—	—	—	Yes	—
HW Divider	Yes	—	—	—	—	—
Nonmaskable Int.	Yes	—	—	—	—	—
Cache (Instr)	—	—	—	4–128K	4–128K	8K
Cache (Data)	—	—	—	4–128K	4–128K	8K
TCM (Instr)	0–4MB	0–4MB	0–64MB	0–1MB	0–1MB	—
TCM (Data)	0–4MB	0–4MB	0–64MB	0–1MB	0–1MB	—
Memory Mgmt	MPU	AHB-Lite DMA	—	MPU	MMU	MMU
Bus Arch.	Harvard	von Neumann	von Neumann	von Neumann	Harvard	von Neumann
Main I/O Bus	2 x AHB-Lite	1 x AHB-Lite	1 x AHB	1 x AHB	2 x AHB	1 x AHB
Total Bus Width	64 bits	32 bits	32 bits	32 bits	64 bits	32 bits
Coprocessor I/F	—	—	Yes	Yes	Yes	Yes
Die Area†	0.9mm²	0.59mm²	1.0mm²	1.96mm²	1.68mm²	3.2mm²
Power†	0.045mW/MHz ‡	0.13mW/MHz	0.25mW/MHz	0.3mW/MHz	0.3mW/MHz	0.25mW/MHz
Introduction	2006	2004	1999	1999	2001	2000

Table 1. When compared with other members of the ARM9E family, the clockless ARM996HS has several similarities and differences—besides the stark differences of asynchronous logic and an indeterminate clock speed. This table also includes the ARM922T, a hard core related to the ARM9E family. TCM refers to tightly coupled memory, a deterministic substitute for caches. (*Maximum worst-case clock frequency in a generic 0.13-micron fabrication process. †Die area and power consumption assumes a core without caches or TCMs [except for the ARM922T] in a generic 0.13-micron process; the die area listed for the ARM996HS is an *MPR* estimate based on an 89,000-gate firm core. ‡ARM estimate. n/a = not applicable.)

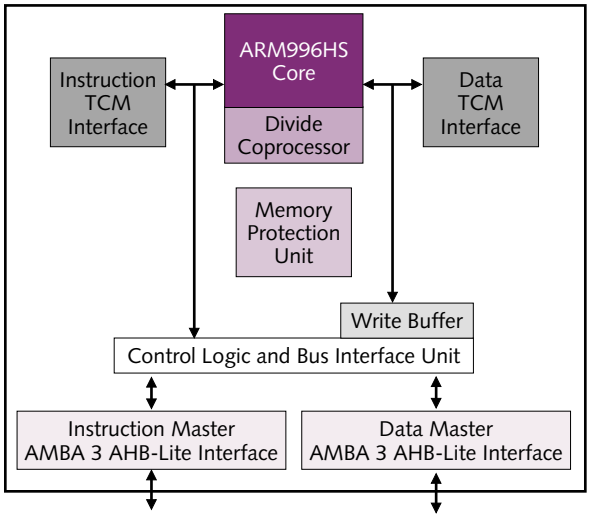

Figure 2. ARM996HS block diagram. Notice the Harvard-architecture memory bus with dual AHB-Lite interfaces, tightly coupled memories (TCM) instead of instruction and data caches, a new integer-division unit, and a memory protection unit (MPU). However, the ARM996HS lacks an interface for external coprocessors.

the ARM9E family with a Harvard bus architecture is the ARM926EJ-S; all the other cores have a von Neumann bus architecture with a single 32-bit AHB interface to main memory. Note that the AHB-Lite interfaces in the ARM996HS run synchronously to an external clock signal in the normal fashion.

Memory Protection Improves Reliability

Memory management is another feature that varies in the ARM9E family. One processor, the ARM926EJ-S, has a memory-management unit (MMU) capable of managing virtual memory with sophisticated operating systems, such as Windows CE and Linux. Other members of the ARM9E family have a less capable memory-protection unit (MPU) or no memory-management hardware at all. The ARM996HS falls in the middle of the pack. It has an enhanced MPU capable of supporting memory protection for a real-time operating system (RTOS) such as VxWorks, but it can't run Windows CE or full-fledged versions of Linux requiring virtual memory.

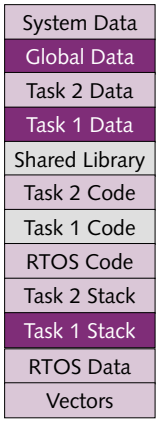

Figure 3. The ARM996HS has an enhanced MPU that protects the operating system from user tasks, separates multiple user tasks from each other, and keeps the data and stacks from different programs in their own regions of memory.

As the simplified memory map in Figure 3 shows, the MPU can manage separate regions of protected memory for multiple application programs, including their code, data, and stacks. At the same time, it can protect various regions of memory for the RTOS, system data, global data, and interrupt-vector tables. Because the ARM996HS has some memory features of the ARMv6 ISA, the MPU can protect memory regions as small as 32 bytes. Some regions can overlap, allowing them to share access among multiple tasks.

Last, the ARM996HS has two new features not found in any other ARM9E core: nonmaskable interrupts (NMI) and an integer-division unit. ARM imported NMIs from the future, so to speak—they're part of the newer ARMv6 ISA with TrustZone security extensions. (See *MPR 8/25/03-01*, "ARM Dons Armor.") Although the ARM996HS doesn't have TrustZone, it can prevent programs from masking what ARM calls fast interrupts (FIQ). FIQs are faster and higher-priority interrupts than regular interrupt requests (IRQ), because they always jump to the last entry in the interrupt-vector table, which bypasses the branch instructions in other entries of the table. The ARM996HS can stop a process from masking an FIQ.

This feature makes the ARM996HS more suitable for embedded-control applications requiring high reliability or availability. For example, an NMI could allow an imminent battery failure to interrupt the software and either alert the user or switch to another power source. In addition, the ARM996HS can suspend all operations and wait for an interrupt without consuming any active standby power. Unlike a clocked processor, it doesn't need to periodically poll for interrupts. Instead, the interrupt activates control logic that wakes up the processor.

The new division unit manipulates signed and unsigned 32-bit integers and is a substitute for slower calls to a math library. Semantically, the division operations resemble those in the latest ARMv7 ISA. However, to preserve strict compatibility with ARMv5TE, the ARM996HS implements the division unit as an internal coprocessor instead of altering the instruction set. The divider uses the common SRT algorithm and requires 16 iterations to perform a typical operation. It runs in parallel with the regular integer pipeline, hiding the latency of nondependent operations. A divide requiring 36 clock cycles in other ARM9E processors needs the equivalent of only 13 cycles in the ARM996HS. That total includes reading and writing the divider's registers, so it's even less if the registers already contain one or both operands.

Lower Peaks Reduce Electromagnetic Noise

Low power consumption is only one reason for using asynchronous logic. Another is to reduce electromagnetic emissions. A processor running on self-timed logic instead of a global clock signal generates much less noise in the radio-frequency spectrum than a conventional processor does. Low noise can be as important as low power in tightly packed embedded systems that locate the processor near sensitive analog components and circuits.

Conventional processors radiate electromagnetic noise at their clock frequency and at higher harmonics of that frequency. In embedded systems running at common embedded-processor clock speeds, those emissions may interfere with the FM radio band, which ranges from 88MHz to 108MHz. That interference can be a particular problem with FM radios in automotive systems and portable consumer-electronics products. Electromagnetic interference is also troublesome for wireless communications devices—another application for which a low-power processor like the ARM996HS is ideally suited.

According to tests by ARM and Handshake Solutions, the ARM996HS's peak currents are 2.4 times lower than those in the ARM968E-S. That's significant, because peak currents cause spikes in electromagnetic emissions. ARM says the ARM996HS virtually eliminates microprocessor-based interference in the FM radio band and reduces emissions by 25dB in bands from 800MHz to 2.5GHz. Figure 4 compares the electromagnetic emissions of the ARM996HS with those of the ARM968E-S over the full radio-frequency spectrum.

The unique power signature of the ARM996HS may become a more important selling point than its overall power consumption. Other licensable 32-bit processor cores implemented in conventional logic can boast of competitive power numbers, but their power signatures are probably less favorable.

For instance, the base configurations of Tensilica's Xtensa LX and Xtensa 6 processors consume only 0.04mW per megahertz. A similar configuration of ARC International's ARC 600 consumes about 0.06mW per megahertz. Those estimates from ARC and Tensilica exclude memories and assume fabrication in a common 0.13-micron process, which would yield 0.045mW per megahertz with the ARM996HS. In applications requiring low electromagnetic emissions, however, the ARM996HS would almost certainly enjoy the advantage. And its overall power consumption would probably be lower, too, because typical implementations of the configurable ARC and Tensilica processors are much larger than their stripped-down base configurations are.

Is the Long Wait Nearly Over?

As we noted in our first report on the ARM996HS in 2004, researchers all over the world have been working on the concept of asynchronous logic since the 1950s, long before microprocessors were invented. The University of Manchester in England was a pioneer in the technology and has worked with ARM in the past. Manchester began building an asynchronous computer in 1969 and designed three asynchronous ARM-compatible processors—the Amulet 1, Amulet 2, and Amulet 3e—in the early 1990s. Manchester based those processors on Ivan Sutherland's asynchronous-logic technology, and ARM supported their development. (See *MPR 2/25/02-01*, "Technology 2001: On a Clear Day You Can See Forever.") For various reasons, none of the Amulet processors ever reached the market.

Now, ARM is finally on the verge of realizing a long-held dream. Delivering the first commercially available

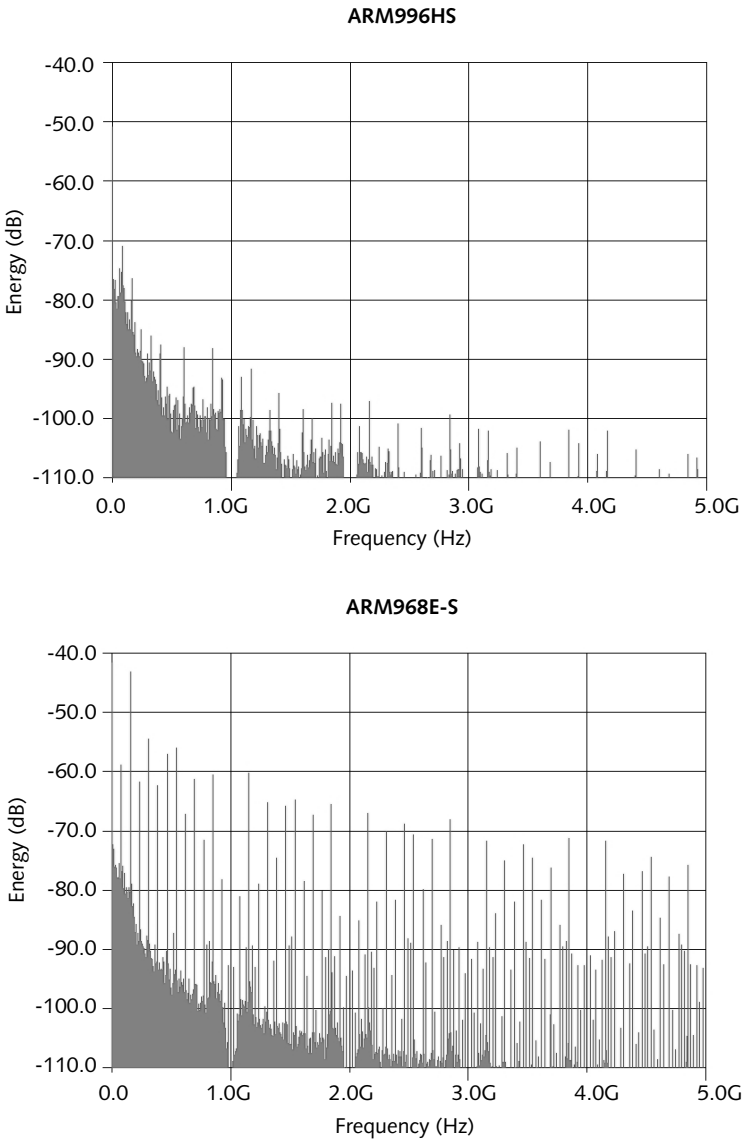

Figure 4. The clockless ARM996HS processor has lower peak currents than the conventionally clocked ARM968E-S, so it emits less electromagnetic noise. These charts plot electromagnetic emissions across the full radio-frequency spectrum from 0.0Hz to 5.0GHz.

Price & Availability

ARM is licensing the ARM996HS 32-bit processor core now. ARM delivers the processor as a firm core—a gate-level netlist synthesized for Artisan physical-IP libraries targeting popular fabrication processes at independent foundries. ARM and Handshake Solutions will synthesize the core for other libraries and processes on request. ARM doesn't disclose up-front licensing fees or chip royalties, which are negotiable. There is currently no information about the ARM996HS on ARM's website; for more background about the processor and asynchronous logic, see *MPR 11/29/04-02*, "ARM's Asynchronous Handshake."

Handshake Solutions separately licenses its proprietary Haste design language and design tools to other companies for asynchronous-logic development. For more information, visit *www.handshakesolutions.com*.

clockless 32-bit microprocessor core to a customer is a historic milestone. The yearlong delay since ARM's announcement in 2004 is insignificant compared with the decades of research invested in the technology.

But despite the optimistic results of gate-level simulations and an FPGA implementation, the real results won't be known until the first chips return from the foundry later this year. There might be more setbacks that require multiple passes of silicon to resolve. Many chip designs less risky than the ARM996HS look great in simulation, then suffer frustrating glitches when translated into transistors.

ARM deserves credit for openly talking about an extremely difficult project whose outcome isn't guaranteed. Other companies in ARM's situation might maintain total secrecy until either succeeding or quietly giving up. Now, ARM and Handshake Solutions are tantalizingly close to making a genuine breakthrough in microprocessor design. *MPR* wishes them luck, and we eagerly await proof of their success.