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CAVIUM EXPANDS OCTEON FAMILY

Single- and Dual-Core Chips Supplement High-End Network Processors

By Tom R. Halfhill {2/6/06-01}

Cavium Networks is expanding its family of Octeon network/communications processors with chips that have one or two MIPS64 processor cores, instead of as many as 16 cores found in higher-end members of the family. But the new parts aren't simply chopped-down layouts. Their features, performance, power consumption, and prices vary according to their target applications, and they introduce some entirely new Octeon features, such as USB 2.0 and voice-over-IP (VoIP) interfaces.

In all, Cavium has announced 10 new Octeon chips scheduled for sampling in 1Q06 and 2Q06. Seven are single-core processors, and three have dual cores. All use Cavium's custom-designed cnMIPS64 processor core, so they are binary compatible with software written for existing Octeons, including the Octeon NSP and EXP series. (See *MPR 9/6/05-01*, "Cavium: Security Optional.")

Although the new parts are "low-end" members of the Octeon family, they are still powerful network/communications processors by any measure, having one or two 64-bit MIPS-compatible processor cores and hardware acceleration for packet processing, quality-of-service (QoS) filtering, and TCP termination. Some of the new chips also retain the acceleration engines for cryptography, pattern matching, compression, and decompression that distinguish higher-end Octeons from other network/communications processors.

Instead of targeting the most demanding applications, such as core routers and switches, the latest chips are intended for smaller routers in LANs and WLANs, network-access gateways, line aggregators, security appliances, network storage subsystems, and similar applications. Prices start at $19 for 50,000-unit quantities of the smallest single-core chip and range upward to $125 for 10,000-unit quantities of the best dual-core chip. Cavium says all the new parts will enter production one quarter after samples are available.

Untangling the Feature Matrix

The Octeon family is growing so fast that understanding which parts have which features is a challenge for anyone who doesn't work in Cavium product marketing. Original members of the Octeon family are now called the Octeon NSP series. Cavium coined the term "network services processor" to describe these highly integrated devices, which have 2 to 16 processor cores per chip plus hardware acceleration for packet routing, filtering, and security. (See *MPR 10/5/04-01*, "Cavium Branches Out.")

Last summer, Cavium announced the Octeon EXP series, which is nearly identical to the NSP series but omits the cryptography engine and related security features. (See *MPR 9/6/05-01*, "Cavium: Security Optional.")

Hardware Acceleration	Cavium Octeon CP	Cavium Octeon SCP	Cavium Octeon EXP	Cavium Octeon NSP
Packet & TCP Termination	Yes	Yes	Yes	Yes
Security & True RND Numb	—	Yes	—	Yes
Reg-Ex, Data Comp/Decomp	—	—	Yes	Yes

Table 1. Two new series of Octeons (CP and SCP) expand the existing Octeon family, which already includes the original NSP and recent EXP series. There are numerous smaller differences among the chips in each series.

The latest members of the Octeon family create two new series and expand the original NSP series. The new series are Octeon CP (communications processors) and Octeon SCP (secure communications processors). As those names imply, the main difference is security: SCP chips have it; CP chips don't. Table 1 presents a quick summary of the major features distinguishing the Octeon CP, SCP, EXP, and NSP series.

Notice that both the Octeon CP and EXP series lack security features. But they aren't redundant. There are many small differences between these series that become apparent only after studiously comparing their specifications. A simpler way to think about them is that Octeon EXP chips are near-identical derivatives of their Octeon NSP forebears, whereas Octeon CP chips show evidence of fresh design work. Cavium has added some new features—such as USB 2.0 and VoIP interfaces—while removing other things. We will describe all those differences shortly, but sorting out the 10 newborn members of the Octeon CP, SCP, and NSP series is the first order of business.

As Table 2 shows, there are multiple versions of four basic models, adding up to 10 parts in all. The CN3005, at the bottom of the family, is a single-core processor available as a SCP or CP version, depending on whether it includes cryptography engines and a true random-number generator.

Feature	Cavium Octeon CN3005 CP, SCP	Cavium Octeon CN3010 CP, SCP	Cavium Octeon CN3110 CP, SCP, NSP	Cavium Octeon CN3120 CP, SCP, NSP
CPU Architecture	MIPS64-R2	MIPS64-R2	MIPS64-R2	MIPS64-R2
Architecture Width	64 bits	64 bits	64 bits	64 bits
CPU Cores	1	1	1	2
Core Frequency	300–400MHz	300–500MHz	300–550MHz	300–550MHz
Superscalar Issue	2-way	2-way	2-way	2-way
ALU Pipeline Depth	5 stages	5 stages	5 stages	5 stages
ALU Instr Per Sec	600–800 million	600 million–1 billion	600 million–1.1 billion	1.2–2.2 billion
Instruction Cache	16K, 2-way	16K, 2-way	32K, 4-way	32K, 4-way
Data Cache	8K, 64-way	8K, 64-way	8K, 64-way	8K, 64-way
L2 Cache	64KB	128KB	256KB	256KB
TLB	32-entry	32-entry	32-entry	32-entry
FPU	—	—	—	—
Main Memory Controller	DDR2 533MHz 16b, 1-channel	DDR2 533MHz 32b, 1-channel, ECC	DDR2 667MHz 64b, 1-channel, ECC	DDR2 667MHz 64b, 1-channel, ECC
Max DRAM Bandwidth	1.0GB/s	2.0GB/s	5.2GB/s	5.2GB/s
Max DRAM Memory	2GB	2GB	4GB	4GB
RLDRAM/FCRAM*	—	—	—	—
Aux DRAM Controller	—	—	16b DDR2 (NSP only)	16b DDR2 (NSP only)
Packet I/O Interfaces †	2 x RGMII/MII or 1 x GMII	3 x RGMII/MII or 1 x RGMII/MII + 1 x GMII	3 x RGMII or 1 x RGMII + 1 x GMII	3 x RGMII or 1 x RGMII + 1 x GMII
PCI/PCI-X Controller	PCI 32-bit 66MHz Host/slave	PCI 32-bit 66MHz Host/slave	PCI-X 32-bit 100MHz Host/slave	PCI-X 32-bit 100MHz Host/slave
PCI Express	—	—	—	—
HyperTransport	—	—	—	—
USB 2.0 HS Host	1 x MAC + PHY	1 x MAC + PHY	1 x MAC + PHY	1 x MAC + PHY
TDM/PCM Interface	—	Yes	Yes	Yes
Other I/O	Flash, UARTs, MDIO, GPIO	Flash, UARTs, MDIO, GPIO	Flash, UARTs, MDIO, GPIO	Flash, UARTs, MDIO, GPIO
TCP Offload Engine	Yes	Yes	Yes	Yes
ZIP Compress Engine	—	—	NSP only	NSP only
Reg-Expression Engine	—	—	NSP only	NSP only
Crypto Engines	SCP only	SCP only	SCP & NSP only	SCP & NSP only
True RND Generator	SCP only	SCP only	SCP & NSP only	SCP & NSP only
Memory-Alloc Engine	Yes	Yes	Yes	Yes
Fabrication Process	TSMC 0.13µm	TSMC 0.13µm	TSMC 0.13µm	TSMC 0.13µm
Packaging	BGA-350	BGA-525	BGA-868	BGA-868
Power (Worst-Case)	2W–3W	3W–4W	4W–7W	4W–7W
Price (Units)	$19 (50k)	$39 (50k)	$49 (10k)	$125 (10k)
Availability	Samples 2Q06; Production 3Q06	Samples 2Q06; Production 3Q06	Samples 1Q06; Production 2Q06	Samples 1Q06; Production 2Q06

Table 2. Counting the CP (communications processor), SCP (secure communications processor), and NSP (network services processor) variations, there are 10 new Octeon chips. Differences include the number of processor cores, their clock speeds, speeds and widths of their main-memory interfaces, the variety of other I/O interfaces, and security features. Note that prices of the lower-end chips are based on 50,000 units, whereas prices of the higher-end chips are based on 10,000 units—Cavium's pricing is based on likely volumes in different market segments. *RLDRAM and FCRAM interfaces are available only on higher-end Octeon chips; the CN3110 and CN3120 substitute an auxiliary DRAM interface. †MII: Media-Independent Interface; GMII: Gigabit MII; RGMII: Reduced GMII.

Next comes the single-core CN3010, which—like the CN3005—is available as an SCP or CP, with or without security features. Compared with the CN3005, the CN3010 offers a higher maximum clock frequency (500MHz vs. 400MHz), a larger L2 cache (128KB vs. 64KB), a wider main-memory controller (32 bits vs. 16 bits), ECC protection for main memory, an additional packet I/O interface, and a TDM/PCM interface for VoIP (more on this later).

Further up the ladder, the next chip is the single-core CN3110, which is available as a CP, SCP, or NSP. Compared with the CN3010, the CN3110 has a slightly higher maximum clock frequency (550MHz vs. 500MHz), a larger L2 cache (256KB vs. 128KB), a faster main-memory controller (64-bit 667MHz vs. 32-bit 533MHz), and a faster PCI controller (100MHz PCI-X vs. 66MHz PCI 2.1). The SCP version of the CN3110 has the cryptography engines and a random-number generator.

The Octeon CN3110 NSP has everything in the SCP version plus three more features: an auxiliary DDR2 DRAM controller, a regular-expression engine, and a data-compression/decompression engine. Note that the auxiliary DRAM controller (which has a 16-bit, 533MHz DDR2 interface) is a substitute for the RLDRAM/FCRAM controller in existing Octeon NSP chips. These auxiliary memory controllers relieve pressure on main memory by supporting dedicated memory for pattern-matching operations and bypassing the caches for lower latency. To accelerate those operations, which allow deep packet filtering, the NSP version of the CN3110 can use its regular-expression engine to examine packets stored in main memory or auxiliary memory. If the packets contain compressed data—such as ZIP, GZIP, or PKZIP file attachments—the CN3110 NSP has an engine for accelerating their decompression and recompression.

Rounding out the Octeon family is the CN3120, which will be available as a CP, SCP, or NSP. Unlike the single-core chips described above, the CN3120 has two cnMIPS64 processor cores. Otherwise, it's identical to the CN3110.

New Features Expand Octeon's Scope

Instead of merely subtracting features to create these lower-end Octeons, Cavium invested additional design effort, in some cases adding features entirely new to the Octeon family. As one might expect, those features are appropriate for the target applications.

USB 2.0 is a good example. High-end network processors for core routers may have little use for a USB controller, but small routers and network gateways for homes and small businesses definitely can take advantage of USB. Among other things, USB provides an easy way to attach a printer or mass-storage device to a small network. All 10 of the new Octeon CP, SCP, and NSP chips have a USB 2.0 High Speed (480Mb/s) host controller, plus an integrated physical-layer (PHY) interface—an unusual frill that eliminates the need for an external (albeit inexpensive) PHY chip.

Another addition is the aforementioned TDM/PCM interface, common to all the new Octeons except the lowest-end CN3005 CP and SCP. TDM/PCM stands for time-division multiplexing/pulse-code modulation, but that doesn't adequately describe the purpose of this interface. It's there to support VoIP services, which transmit digitized telephone conversations over the Internet in TCP/IP packets.

As Figure 1 shows, the new Octeon processors can encode or decode voice packets and use the TDM/PCM interface to exchange the data with an external chip called a SLIC (subscriber line interface circuit). The SLIC performs the final analog/digital conversions and handles other telephony functions, such as ring signaling. For installations having one or two phone lines, the new Octeons have enough processing power to encode or decode VoIP without extra help. For larger installations, the TDM/PCM interface connects to an external DSP that runs the audio codecs, and the DSP connects to the SLIC.

Cavium did some trimming on the new Octeons, too. The most obvious difference between the new chips and existing Octeons is the number of processor cores: one or two instead of two to sixteen. As described above, none of the new Octeons have the auxiliary RLDRAM controller, although two devices (the CN3110 NSP and CN3120 NSP) substitute an auxiliary DDR2 DRAM controller. Cavium removed the ternary content-addressable memory (TCAM) controller found in existing Octeon chips because TCAM is more appropriate for higher-end routers, which often use it to store tables of packet headers. In the CN3110 and CN3120, Cavium made the PCI-X interface narrower (32 bits vs. 64 bits) and slower (100MHz vs. 133MHz) than PCI-X in existing Octeons. In the CN3005 and CN3010, Cavium replaced PCI-X with PCI.

All the main-memory interfaces in the new chips are narrower (16–64 bits vs. 64–128 bits) and slower (533–667MHz vs. 800MHz) than those in existing Octeons, and the CN3005 dispenses with ECC protection for main memory. All the L2 caches are smaller (64–256KB instead of

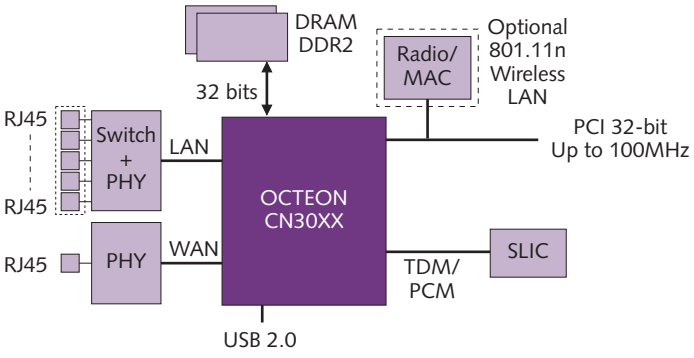

Figure 1. This system-level diagram of an 802.11n broadband wireless gateway shows how most of the new Octeon processors can support VoIP phones with their TDM/PCM interfaces. The interface connects to an external SLIC (subscriber line interface circuit) chip, which performs the final analog/digital conversions, allowing users to attach ordinary telephones.

Price & Availability

Samples of the Octeon CN3110 CP, CN3110 SCP, CN3110 NSP, CN3120 CP, CN3120 SCP, and CN3120 NSP will be available this quarter, and production is scheduled to begin in 2Q06. Prices will range from $49 to $125 in 10,000-unit quantities. Samples of the Octeon CN3005 CP, CN3005 SCP, CN3010 CP, and CN3010 SCP will be available in 2Q06, with production scheduled to begin in 3Q06. Prices will range from $19 to $39 in 50,000-unit quantities. For more information, visit *www.caviumnetworks.com*.

1MB). The new chips also have fewer packet I/O interfaces, supporting only two or three Ethernet controllers instead of the four or eight controllers in higher-end Octeons.

Although Cavium removed or reduced quite a few features, the resulting chips are well suited for their applications. In particular, eliminating some unneeded I/O interfaces and downsizing others has reduced the pin counts, which simplifies the chip packaging and cuts costs. Of course, some of the new interfaces required additional pins. But overall, the new Octeons have fewer pins, smaller packages, and lower prices than their predecessors. They also consume less power: 2W to 7W compared with 5W to 25W for the full-featured Octeons.

Low Prices for 64 Bits and High Integration

The new Octeons will compete against many similar network/communications processors from other vendors, especially AMD, Broadcom, Freescale, Intel, and PMC-Sierra. Although AMD, Broadcom, Cavium, and PMC-Sierra are MIPS licensees, they use different MIPS-compatible cores, each with its own advantages and disadvantages.

Cavium's cnMIPS64 is the newest MIPS-compatible core in this group. It supports the latest MIPS64-R2 instruction-set architecture, has two-way superscalar pipelines, and has enhanced prefetching for both instructions and data. The pipeline is only five stages long, which reduces complexity and saves power but restricts the maximum clock frequency.

AMD's Alchemy processors have a 32-bit MIPS-compatible core that's less powerful than Cavium's 64-bit core. However, the difference matters less in the lower-end applications for which the new Octeon chips are intended. Broadcom's best network processors use a powerful MIPS64 core acquired with SiByte in 2000. Although the SiByte SB-1 core is five years older than Cavium's core, it's a four-way superscalar design that has twice as many pipelines. Those pipelines are seven stages deep—two stages deeper than Cavium's—which allows the SB-1 to reach higher clock speeds. (See *MPR 6/26/00-04*, "SiByte Reveals 64-Bit Core for NPUs.")

Freescale and Intel don't use the popular MIPS architecture for their network/communications processors. Freescale's vast PowerQUICC family relies on 32-bit PowerPC cores and auxiliary coprocessors with proprietary architectures. Intel's competing chips are based on the ARM-compatible XScale 32-bit processor core, which also gets help from proprietary coprocessors. (See *MPR 9/13/99-01*, "Intel Network Processor Targets Routers.")

Comparisons tend to favor the newest products; keep in mind that Cavium's new Octeons aren't shipping yet. However, some observations are in order. The new Octeons will drop the price of 64-bit communications processors with L2 caches below $20, which appears to be a new low for chips with their degree of integration. The Octeons tend to support more Gigabit Ethernet interfaces than similarly priced processors, and they have High-Speed USB 2.0 host controllers with integrated PHYs—a rare, if not unique, feature. Their TDM/PCM interface also sets them apart from most other chips (Intel's IXP465 is an exception), largely because VoIP wasn't important until recently. *MPR* expects future communications processors from all vendors to add more support for VoIP.

Cavium's dual-core CN3120 is the highest priced among the new Octeons, but it's still relatively affordable at $125. Shoppers will be hard pressed to find a less expensive dual-core communications processor with similar integration. However, two new PowerQUICC chips scheduled to ship this quarter deserve a close look: the MPC8358E and MPC8360E.

Although the MPC8358E and MPC8360E are generally considered single-core processors, they supplement their PowerPC e300 cores with two of Freescale's new QUICC Engine auxiliary processors. The QUICC Engine is significantly more powerful than the CPM auxiliary processor in previous PowerQUICC chips. Enhanced programmability elevates the status of the QUICC Engines, making the MPC8358E and MPC8360E more like heterogeneous triple-core processors. Both are highly integrated devices with numerous I/O interfaces and security features. Their prices will start at $34 for the MPC8358E and $44 for the MPC8360E, landing them squarely in the same price range as the new Octeons. (See *MPR 3/21/05-01*, "Freescale Quickens PowerQUICC.")

Fortunately for Cavium, the new Octeons are close cousins of existing Octeon NSPs, which means they inherit some of the industry's best genes. Most of the new Octeons retain the extensive custom logic for packet processing and security that have made Octeon NSPs the processors to beat for the past year. After entering the market in 2002 with its Nitrox security coprocessors, Cavium has exploded on the scene with more than a dozen state-of-the-art network/communications processors, scoring more than 240 design wins. The new Octeons should reap their share. ◇