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ACTEL RELEASES FIRST FUSION CHIP

Highly Integrated Mixed-Signal FPGA With Flash Is an Instant SoC

By Tom R. Halfhill {12/19/05-02}

Just because ASIC and system-on-chip (SoC) projects are becoming prohibitively expensive for many developers doesn't mean there's less demand for custom chips. Product differentiation and integration still matter. Hence, the rush toward alternatives to full-custom silicon, such as FPGAs, structured ASICs, and reconfigurable processors.

Actel's latest alternative is the Fusion Programmable System Chip (PSC)—a new breed of FPGA that can replace SoCs with a single off-the-shelf do-it-all chip. Fusion FPGAs combine reprogrammable logic with analog and digital peripherals, analog and digital I/O, SRAM, flash memory, and optional soft processor cores (a license-free ARM7TDMI-S or 8051). The analog I/O includes five to ten "analog quads," each containing three analog inputs and a MOSFET gate driver.

With their nonvolatile flash memory and instant-on capability, Fusion FPGAs can safely store program code and data while powered down, and they can independently boot the system when powered up. Their mixed-signal I/O eliminates the need for many external I/O devices. Their flash-based reprogrammable gate arrays allow developers to embed high-performance application-specific logic. And developers can encrypt the logic to protect their proprietary intellectual property (IP). (See *MPR 8/15/05-01*, "Actel Mixes Signals on FPGAs.")

On December 12, Actel announced delivery of the first Fusion PSC, to be followed by smaller and larger versions of the chips next year. In addition, Actel has released specifications for the first four devices in the family, along with new development tools. Depending on the amount of programmable logic and other features, chip prices will range from about $5 to $50 for quantities of 250,000 units, or from about $10 to $100 for quantities of 10,000 units. Although Fusion FPGAs cost more than conventional FPGAs, including those from Actel, they can integrate the functions of several chips and reduce overall system costs.

Estimating Capacities of Programmable Logic

Our previous article on Fusion (cited above) covered the basic capabilities of these innovative devices, so this time we'll focus on their specific features and the differences among the first four chips in the family. The range of their features and prices will be so wide that Actel clearly hopes to capture a broad swath of the market, not just a narrow segment. Fusion FPGAs will be suitable for numerous applications in industrial machinery, motor control, automotives, aeronautics, communications, and consumer electronics.

The first Fusion device to sample is the AFS600, destined to be a high-end member of the family. It's second only to the AFS1500, scheduled to ship in 2H06. Below it will be the AFS090, also scheduled for delivery in 2H06, and the AFS250, which should debut in 2Q06.

Fortunately, interpreting Actel's part numbers doesn't require a Captain Midnight decoder ring: they indicate the number of programmable system gates on chip. For example, the AFS600 has 600,000 system gates; the low-end AFS090 will have 90,000 gates; and the high-end AFS1500 will have 1.5 million gates. Unfortunately, interpreting the precise meaning of a "system gate" and comparing it with an ASIC-equivalent logic gate or the programmable gates in other types of FPGAs *does* require a decoder ring.

FPGA developers know the drill. Programmable gates aren't directly comparable to the fixed logic gates in ASICs, because even the best FPGA development tools can't map a logic design onto programmable gates as efficiently as modern synthesis tools can generate fixed logic. A design requiring 100,000 fixed gates in an ASIC might require 25% to 100% more gates in programmable logic. Comparing programmable gates among FPGAs from different vendors is dicey, too, because the vendors use different technology and terminology.

Actel's Fusion and ProASIC3 families of FPGAs use flash-based reprogrammable logic, not the SRAM-based logic in FPGAs sold by market leaders Xilinx and Altera. Actel suggests using a conversion factor that equates 100 system gates to a four-bit lookup table (LUT4). That's a conservative estimate, because the programmable logic in Fusion devices consist of "tiles" that can function as three-bit lookup tables (LUT3) or D flip-flops. Each tile has about 40 system gates. Therefore, the first Fusion chip—the AFS600—has 600,000 system gates in 13,824 tiles, which are roughly equivalent to 6,000 LUT4 cells in a Xilinx or Altera FPGA.

License-Free Soft Processors Are Optional

Perhaps a better way to visualize the capacity of Fusion devices is to relate it to an ARM7TDMI-S processor core. Fusion devices and their ProASIC3 cousins are the first FPGAs allowed to incorporate a synthesizable ARM processor for commercial deployment, not just for prototyping. ARM and Actel have adapted the ARM7TDMI-S processor—the most popular ARM microarchitecture—for synthesis in Actel's reprogrammable fabric.

This is a real coup for Actel. Previously, ARM forbade licensees to deploy ARM processors in FPGAs, fearing that hackers would steal the IP. Actel's flash-based FPGAs have a feature called FlashLock that encrypts proprietary IP in the programmable logic using the Advanced Encryption Standard (AES) cipher with 128-bit keys.

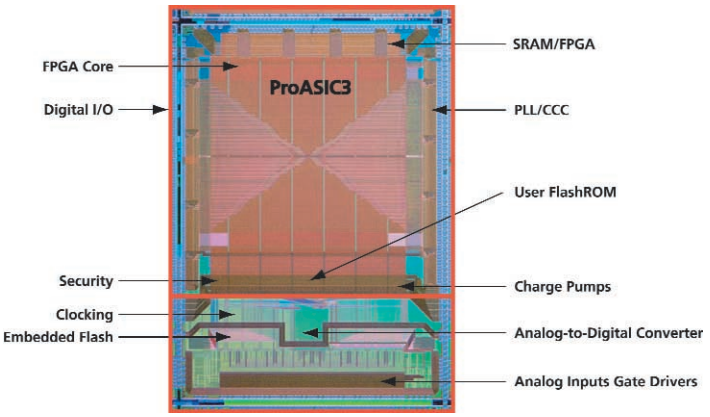

Figure 1. The first Fusion chip is the AFS600, which uses the same flash-based reprogrammable-logic core as Actel's ProASIC3 FPGAs. Additional flash memory, flash ROM, SRAM, mixed-signal I/O, and an optional ARM7TDMI-S processor core make Fusion devices unique among programmable-logic devices.

Actel refers to its specially optimized ARM7TDMI-S processor as the CoreMP7. Not only does ARM allow Actel's customers to deploy the CoreMP7 in Fusion and ProASIC3 FPGAs, but ARM doesn't charge them a farthing for the privilege. Developers needn't buy an expensive ARM license or pay chip royalties to either ARM or Actel. Actel provides the CoreMP7 to customers for the cost of the device, which in volume is about $2 higher than the price of a device without the processor. In effect, the cost of the ARM license (which can range from hundreds of thousands of dollars to millions of dollars) and the royalties are built into the prices of the chips.

This is a fantastic deal for Fusion customers. However, not all Fusion devices have enough programmable logic to implement the CoreMP7 or even the eight-bit 8051-compatible processor that Actel offers as an alternative. The smallest Fusion AFS090 is simply too small for either processor. The next-largest member of the Fusion family, the AFS250, has enough capacity for the 8051 or a minimal configuration of the CoreMP7, but there's little extra room for adding soft peripherals or application-specific logic. The AFS600—and, more so, the AFS1500—can comfortably accommodate the CoreMP7 with useful amounts of additional logic.

Developers familiar with implementing the ARM7TDMI-S in fixed logic can use the CoreMP7 as a yardstick to estimate how much additional logic will fit inside a particular Fusion FPGA.

Integrated Features Are Impressive

Actel advertises Fusion as the first true mixed-signal FPGA. Although some other devices from Actel, Altera, Xilinx, and Lattice have simple mixed-signal components—such as PLLs for generating clock signals—Fusion devices are the first FPGAs combining programmable logic with significant analog and digital I/O capabilities. Mixed-signal handling allows Fusion to integrate many system functions on a single chip.

Fusion FPGAs have one or two PLLs; an on-chip 100MHz resistor-capacitor oscillator, accurate to within 1%; I/O inputs for an external crystal oscillator (32kHz–20MHz); a configurable analog-to-digital converter (ADC) with up to 12-bit resolution; an internal temperature monitor; a current monitor (requiring only a small external resistor in series with the power source); a configurable 32-to-1 analog input multiplexer to feed the ADC; and five to ten analog quads. Each quad is an I/O block with three analog inputs and a high-current MOSFET gate driver. Developers can configure the quads for various functions, such as temperature monitoring, current monitoring, voltage monitoring, digital I/O, and prescaler circuits. The analog inputs tolerate an astonishingly high voltage (±12V), eliminating the need for a voltage converter in many cases.

The advantages of mixed-signal integration go beyond reducing the system's total chip count and bill of materials. Integrating multiple analog functions on a single chip also provides a more consistent noise floor and

minimizes other variances (such as thermal drift) that plague system designers wrestling with dozens of discrete analog components. Actel promotes Fusion as the ideal solution for mixed-signal applications needing the flexibility of software programmability and reprogrammable logic. One example might be a microcontroller for gasoline pumps at a service station. A Fusion FPGA with a soft processor could handle the digital and analog functions of the pump and adapt to multiple geographic regions that use different currencies and volume measures.

Actel hasn't stinted on other features, either. Fusion FPGAs have 256KB to 1MB of embedded flash memory, arranged in one to four blocks, for nonvolatile storage of program code and data. There's also 1Kb of write-once flash ROM for device serialization or secure data storage. The chips have 27Kb to 270Kb of dual-ported SRAM, which can be organized into several different-size blocks. The SRAM provides fast memory for executable code and frequently accessed data. Figure 1 shows a die photo of the Fusion AFS600, and Table 1 compares the features of the four Fusion devices Actel has announced so far.

Fusion FPGAs have various sleep modes for low-power applications. They can awaken on demand or periodically, thanks to an internal 40-bit real-time counter. In Rip van Winkle mode, the chip can slumber for as long as a year before the alarm clock goes off. When the chip does wake up, it can independently boot the system without help from an external PROM or microprocessor. The flash memory automatically reloads the SRAM with all context information saved when the chip was last powered down or put to sleep. These autonomous capabilities make Fusion FPGAs suitable for replacing standalone ASICs and SoCs in embedded systems.

Wanted: Fusion Applets

Introducing a highly integrated mixed-signal FPGA with free processor cores is a significant achievement for Actel, but it's not enough. The chips are merely blank slates. To make good use of these devices in real-world embedded systems, developers need libraries of off-the-shelf IP, and they need sophisticated development tools to create their own application-specific IP. Fusion devices must also allow developers to connect all that IP together with the embedded processor core to enable efficient on-chip communications. All together, it's a tall order, and Actel is working on the solutions.

Much of Actel's soft IP for ProASIC3 FPGAs is compatible with Fusion, because both families are based on the same programmable fabric. Actel offers nearly a hundred DirectCore and CompanionCore IP cores for these families.

As described in our previous article, Actel has introduced a new model for soft IP that developers can use to rapidly implement SoC designs in Fusion devices. "Fusion applets" are self-contained, configurable, and reusable function blocks written in HDL for the programmable-gate fabric, or written in software for the embedded-processor core (if present). An example of a Fusion applet might be a finite impulse response

Feature	Actel Fusion			
	AFS090	AFS250	AFS600	AFS1500
General Features				
Architecture	Fusion FPGA	Fusion FPGA	Fusion FPGA	Fusion FPGA
FPGA Type	CMOS-Flash	CMOS-Flash	CMOS-Flash	CMOS-Flash
Frequency	350MHz	350MHz	350MHz	350MHz
System Gates	90K	250K	600K	1,500K
Tiles (D Flip-Flops)	2,304	6,144	13,824	38,400
Secure Gate Logic	128b AES	128b AES	128b AES	128b AES
PLLs	1	1	2	2
Globals	18	18	18	18
CoreMP7 Soft CPU	—	Optional	Optional	Optional
8051 Soft CPU	—	Optional	Optional	Optional
Supply Voltage	3.3V	3.3V	3.3V	3.3V
Digital I/O Voltage	1.5V–3.3V	1.5V–3.3V	1.5V–3.3V	1.5V–3.3V
Analog I/O Voltage	± 12V	± 12V	± 12V	± 12V
IC Process	0.13µm 7LM	0.13µm 7LM	0.13µm 7LM	0.13µm 7LM
Memory				
SRAM (Kbits)	27Kb	36Kb	108Kb	270Kb
512 x 9b Blocks	6	8	24	60
Flash ROM (Kbits)	1Kb	1Kb	1Kb	1Kb
Embedded Flash	256KB	256KB	512KB	1024KB
E-Flash Blocks	1	1	2	4
Analog Components				
Analog Quads	5	6	10	10
Analog Inputs	15	18	30	30
FET Drivers	5	6	10	10
Temp Monitor	Yes	Yes	Yes	Yes
Current Monitor	Yes	Yes	Yes	Yes
ADC	8-, 10-, 12b	8-, 10-, 12b	8-, 10-, 12b	8-, 10-, 12b
Input / Output				
I/O Types*	Analog LVDS Standard+	Analog LVDS Standard+	Analog LVDS Pro	Analog LVDS Pro
I/O Banks (+JTAG)	4	4	5	5
Digital I/O Pins (max)	90	116	172	228
Analog I/O Pins	20	24	40	40
PCI	64b 66MHz	64b 66MHz	64b 66MHz	64b 66MHz
Digital / Analog I/O Pins By Package Type				
QN-180	53 / 20	62 / 24	—	—
PQ-208	90 / 20	95 / 24	95 / 40	95 / 40
FG-256	—	116 / 24	119 / 40	119 / 40
FG-484	—	—	172 / 40	228 / 40
Pricing & Availability				
Price (250K Units)	$4.95	n/a	<$20	<$50
Production	2H06	2Q06	Now	2H06

Table 1. The first four FPGAs in Actel's Fusion family span a wide range of prices and capabilities. Their most distinguishing feature is the amount of reprogrammable logic, as specified by the numbers of system gates and tiles. Actel offers two synthesizable processor cores for Fusion: the CoreMP7, a specially optimized version of the ARM7TDMI-S; and an 8051-compatible core. All Fusion devices in this table except the AFS090 have enough programmable logic for these cores. (*LVDS: low-voltage differential standard; Standard+ and Pro: I/O types carried over from other Actel FPGAs. n/a: data not available.)

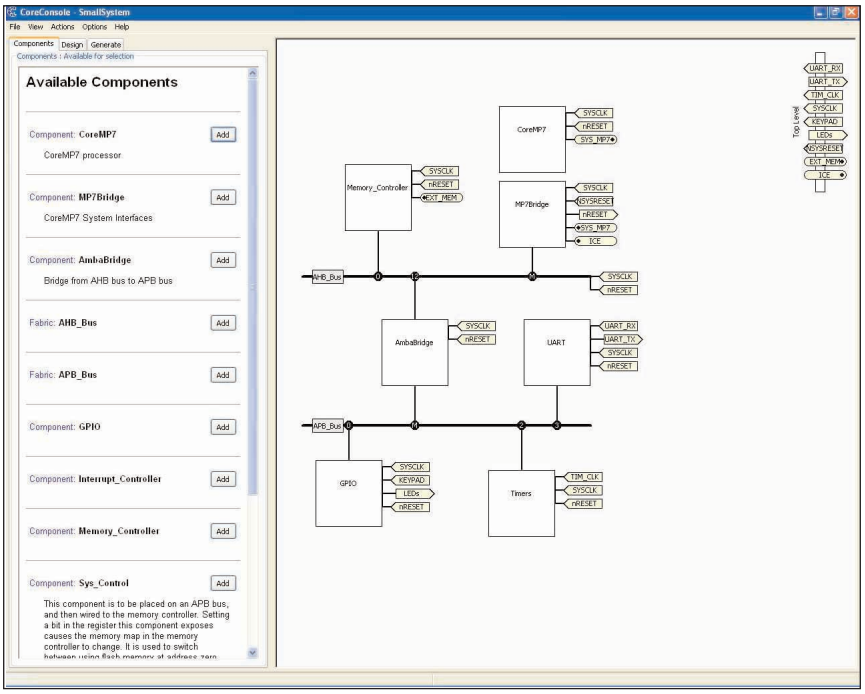

Figure 2. CoreConsole is a new soft-IP integration tool for Fusion FPGAs. Developers can choose Fusion applets and other components from an IP library and stitch them together to create application-specific designs. Notably, the tool's IP library is open to third-party IP providers, using a secure licensing scheme. This screen shows a developer integrating the CoreMP7 (Actel's version of the ARM7TDMI-S processor core) into a design with an AMBA high-speed bus (AHB) and AMBA peripheral bus (APB). CoreConsole automatically generates a Verilog or VHDL model of the finished design, plus test benches.

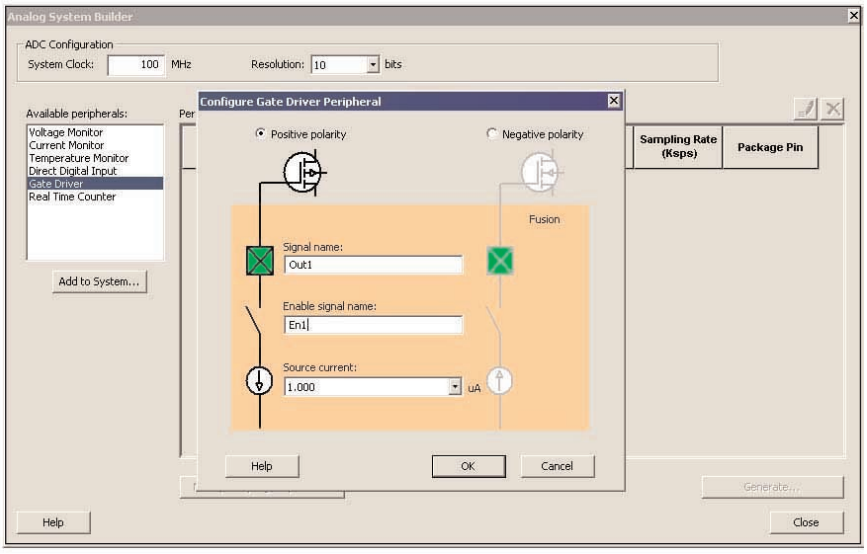

Figure 3. SmartGen is a new peripheral-configuration tool for Fusion FPGAs. It allows Fusion developers to configure peripherals and function blocks, whether built into the chip (such as the ADC) or added with the CoreConsole tool. SmartGen automatically connects peripherals to Fusion's smart backbone, an on-chip bus synthesized in the programmable fabric.

(FIR) filter for motor control. Another might be a function block that uses the built-in temperature monitor or an external monitor to control a cooling fan.

Ideally, Fusion developers will be able to choose from vast libraries of such applets to rapidly build application-specific solutions. Today, however, Actel offers only a few applets. The company hopes third parties will largely fill the void by developing and marketing their own applets, much like the lively trade in plug-in filters for Adobe Photoshop.

Jump-starting a third-party IP market is easier said than done. A few years ago, ARC International tried to interest third parties in providing synthesizable IP for its configurable processor cores, but largely failed. (See *MPR 6/19/00-03*, "ARC Cores Encourages 'Plug-Ins.'") An even more relevant example was Triscend, which sold a unique line of ARM7- and 8051-based microcontrollers that integrated some programmable logic for implementing application-specific function blocks and peripherals. Despite having good technology, Triscend struggled for customers and never inspired much third-party support. Last year, Triscend was almost acquired by ARM before being snatched by Xilinx at the last minute. (See *MPR 3/15/04-02*, "Xilinx Reconfigures Triscend.")

One problem is that developers creating IP for their own applications usually want to keep it proprietary, for competitive purposes. Another problem is that the universe of customers for something like a Fusion FPGA rarely grows large enough to attract much attention from companies in the business of providing third-party IP. Fusion could prove to be the exception. But if a third-party development community doesn't take root, Actel will probably end up developing more Fusion applets itself or subsidizing their outside development.

Even if ready-made Fusion applets are scarce for a while, it's not a show-stopper. Developing Fusion applets isn't more difficult than creating equivalent hard-wired function blocks or software for ASICs and SoCs. Fusion applets are potentially more reusable than hard-wired blocks are, and the applets are certainly more flexible, because the programmable fabric of a Fusion FPGA is fast

enough to reconfigure them on the fly. To ease development, Actel is introducing two new tools, as the screen shots in Figure 2 and Figure 3 show. CoreConsole is a soft-IP integration tool, and SmartGen is a peripheral-configuration tool. Both tools work with Libero 7.0, an enhanced version of Actel's integrated development environment (IDE) for programming the FPGA fabric.

Efficiency of Smart Backbone Is Crucial

In our previous article on Fusion, we wondered whether Actel would provide the standard AMBA bus for connecting the ARM7 processor core to on-chip peripherals, and we questioned whether Actel's on-chip smart backbone would be efficient enough to support complex SoC-class designs. Actel has answered the first question in the affirmative; the second question remains open.

Fusion customers using the CoreMP7 processor will also get the AMBA bus IP at no additional charge. Peripherals—such as timers, UARTs, and memory controllers—are also available at no extra cost. Getting the AMBA IP as part of the deal is good news, because otherwise, customers (or Actel) would have to develop bus wrappers to connect the processor to whatever alterative on-chip bus Actel saw fit to provide. When Actel first announced Fusion, *MPR* was concerned that Actel's smart backbone or something equally unfamiliar to ARM developers would be the only alternative.

Instead, the smart backbone (also free) is more like a global on-chip bus that also performs some higher-level functions. Its most basic purpose is to work like a global multidrop bus connecting Fusion applets to each other and to the on-chip peripherals and memory. If the chip design includes an 8051 or ARM7 processor core, then the processor and its local buses and peripherals are a subsystem connected to the smart backbone. In addition, the smart backbone works like a microsequencer and management tool for on-chip resources. It can automatically manage a peripheral's flags, buffers, and performance parameters, and it can save contexts of peripheral configurations for restoration after a reboot. The smart backbone can reconfigure on-chip resources as often as every clock cycle, so Fusion chips can instantly adapt to changing conditions and workloads.

The open question is whether the smart backbone, a synthesized structure in programmable logic, is scalable to large, complex designs. Some of today's ASICs and SoCs are getting awfully complicated. They integrate multiple processor cores, scores of on-chip peripherals, large amounts of memory, and extensive custom logic. A synthesized bus like Actel's smart backbone isn't as efficient as a carefully crafted hard-wired bus, nor as efficient as a comparable bus synthesized in fixed logic. Much will depend on the ability of Actel's automated routing tools to intelligently distribute the smart backbone throughout the chip's programmable-logic fabric. Alternatively, it's possible to connect the analog and memory interfaces directly to the processor's AMBA bus or to a firm-wired bus.

For modest designs, we anticipate no problems. To offer a genuine alternative to designing a highly complex ASIC or SoC—clearly the ambition for Fusion—Actel will need to convince skeptics with examples of successful designs.

Truly Innovative and Unique

Fortunately, Actel has some time to refine its tools and smart-backbone technology before developers run into limitations with Fusion. The initial Fusion devices don't have enough programmable logic to support really large designs on the scale of the biggest custom chips, anyway. The largest Fusion part, the AFS1500, won't appear until 2H06. Eventually, Actel will need to introduce even bigger devices to compete in the arms race with SoCs. In the meantime, Actel can work on improving its development tools and interconnect technology.

But enough nitpicking. *MPR* considers Fusion one of the most innovative products of the year. It's a significant new alternative to spinning custom silicon and an important advance for FPGAs. It certainly heats up the debate over the future of reconfigurable logic. (See *MPR 5/3/04-01*, "Microprocessor Sunset," and *MPR 5/10/04-01*, "Reconfigurable 'Illogic.'") And the ability to embed a soft ARM processor for commercial deployment gives Fusion a strategic advantage over other FPGAs.

These days, introducing a truly unique product of any kind is almost unique. Yet despite its uniqueness, Fusion doesn't veer as far from the FPGA path as the equally interesting Triscend technology that has vanished into Xilinx. Fusion's relative familiarity might make it more acceptable to mainstream SoC developers. ◇

Price & Availability

Actel's first Fusion FPGA, the AFS600, is available now and costs less than $20 in 250,000-unit volumes. The next device in the family to ship will be the AFS250 in 2Q06; Actel will announce pricing later. The two remaining parts that Actel has announced so far—the AFS090 and AFS1500—are scheduled to ship in 2H06. The AFS090 will cost $4.95 and the AFS1500 will cost less than $50, both in 250,000-unit volumes. (All prices roughly double in 10,000-unit volumes.) The optional ARM7-compatible CoreMP7 soft processor will add about $2 to the cost of the chips in 250,000-unit volumes. For more information about Fusion, visit *www.actel.com/products/fusion/*.