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PHILIPS TRIMEDIA GOES MOBILE

New TM3270 Is the First Low-Power TriMedia Processor Core

By Tom R. Halfhill {12/5/05-01}

In 1994, when most microprocessor architects were only beginning to turn their attention toward the new demands of multimedia, Philips Semiconductors announced the innovative TriMedia architecture. "TriMedia" referred to the combination of high-resolution graphics, high-fidelity audio, and full-motion video that Philips believed would dominate future processing workloads.

From today's perspective, the Philips TriMedia architects seem like psychics. Although multimedia was an industry buzzword before 1994, Intel was still two years away from introducing its first MMX extensions, which began a long overhaul of the x86 architecture that led to MMX2, SSE, SSE2, and SSE3—and hasn't stopped yet. During the same period, almost every other CPU architecture was similarly retrofitted. In the past year alone, *Microprocessor Report* has covered new audio/video extensions or media-processor cores from ARC International, ARM, Elixent, Imagination Technologies, MIPS Technologies, Silicon Hive, Tensilica, and Videantis. And don't forget the new PowerPC-based processors designed for next-generation videogame consoles from Microsoft, Nintendo, and Sony.

The future that Philips anticipated in 1994 is finally here. Unfortunately, the company's foresight hasn't translated into equally impressive market success. TriMedia has survived for 11 years, but Philips has stopped trying to broadly license the architecture. Today, TriMedia processor cores are found in some Nexperia-brand media processors that Philips sells as standard parts and uses in its own successful consumer-electronics products. There's nothing wrong with that. But like other media-processor architectures launched with great hopes in the 1990s, TriMedia has faced tough competition from general-purpose processors whose multimedia extensions it helped inspire.

Now, Philips is pushing TriMedia in a new direction. In early November, Philips announced the TM3270, the first low-power TriMedia core for mobile applications. (This was a core announcement, not a chip announcement; the company plans to announce TM3270-based Nexperia standard parts in 2006.)

The TM3270 is an important addition to the TriMedia family. Other TriMedia cores deliver high performance but consume too much power for the new wave of portable consumer-electronics products, such as Apple's video iPod. The TM3270 uses multiple techniques to cut power consumption and has new instructions and other features targeting digital video. As a result, it supports all the latest audio/video software codecs and can fully decode D1-resolution H.264 video streams while typically consuming less than 100mW.

This time, Philips isn't years ahead of the pack. In recent months, several competing companies have announced low-power processor cores, extensions, or coprocessors for accelerating digital video. Prospective customers will have many alternatives to TM3270-based Nexperia chips. Nevertheless, the TM3270 is another innovative design based on the powerful TriMedia architecture, and it's definitely a smart move for Philips.

New Microarchitecture Requires Recompilation

Philips derived the new TM3270 from the existing TM3260 core and the two-year-old TM5250, which won our *MPR* Analysts' Choice Award for Best Media Processor of 2003.

(See *MPR 2/9/04-14*, "Best Media Processor: TriMedia TM5250.") The TM3270 is upwardly source-code compatible with all TriMedia processors based on the DSPCPU32 instruction-set architecture (ISA), which made its debut in 1994. This pioneering VLIW architecture has an even longer history in research work, dating back to 1987. (See *MPR 12/5/94-03*, "Philips Hopes to Displace DSPs with VLIW," and *MPR* 8/8/90, "Philips Gives LIFE to VLIW.")

Traditional VLIW architectures rarely maintain binary compatibility from one microarchitecture to another, because their instruction words are formatted for specific complements of function units. The TM3270 is no exception. Software for the existing TM3260 will run on the TM3270 without source-code modifications, but the programs do require recompilation. To take advantage of the TM3270's newest features, programmers must rewrite some existing source code. Even without such optimizations, significant performance gains are possible simply by recompiling. (Note that the TM3270 is not compatible with the 64-bit DSPCPU64 ISA announced in 1998—which doesn't matter, because Philips never implemented that ISA.)

Feature	TriMedia TM3270	TriMedia TM3260	TriMedia TM5250
Architecture	DSPCPU32	DSPCPU32	DSPCPU32
Architecture Width	32-bit	32-bit	32-bit
Core Freq (worst-case)	350MHz	240MHz	500MHz
Memory Bus Freq	To 350MHz	200MHz	200MHz
DDR Bus Freq*	To 700MHz	200MHz	400MHz
Pipeline Depth	7–12 stages	5–7 stages	11–16 stages
Function Units	32 total	27 total	29 total
Constant	5	5	4
Shifter	5	2	3
Simple ALU	—	—	4
ALU	5	5	3
Branch	3	3	3
DSP ALU	3	2	3
DSP Multiplier	2	2	2
Floating-Point ALU	2	2	2
Floating-Point Mul	2	2	2
Floating-Point Div	1	1	1
Floating-Point CMP	1	1	1
Load/Store	2	2	1
CABAC Decoder	1	—	—
IEEE-754 Floating Point	Yes	Yes	Yes
SIMD Capabilities	1 x 32 bits 2 x 16 bits 4 x 8 bits	1 x 32 bits 2 x 16 bits 4 x 8 bits	1 x 32 bits 2 x 16 bits 4 x 8 bits
Two-Slot Operations	Yes	—	—
Collapsed Loads	Yes	—	—
CABAC Decoding	Yes	—	—
Mul (Round, Scale, Clip)	Yes	—	—
Enhanced Prefetch	Yes	—	Yes
Enhanced Data Cache	Yes	—	Yes
L1 Cache (I/D)	64K/128K	32K/16K	64K/16K
L2 Cache	—	—	128K
L2 Cache Freq	—	—	250MHz
Process	90nm	0.13µm 6LM	0.13µm 6LM
Die Size	8.08mm^2	11.4mm^2	19.8mm^2
Core Voltage	1.1V	1.2V	1.2V
Power (typical)	~100mW†	384mW	1.25W
MediaStone Score	424	208	425
EEMBC ConsumerMark ‡	—	23.3 OTB	51.3 OTB
EEMBC ConsumerMark ‡	—	110 OPT	284.6 OPT
Availability	2006	Now	Now

Table 1. The new Philips TriMedia TM3270 processor core is a direct descendant of the TM3260, but it also inherits features from the award-winning TM5250 while adding wholly new features of its own. Key differences include the pipelines, caches, function units, and new instructions optimized for digital video. (*Effective bus frequency using DDR-SDRAM; †Philips estimate; ‡OTB: unoptimized out-of-the-box score; OPT: optimized score.)

Among the features inherited from the TM5250 are an improved load/store unit, an enhanced L1 data cache, and versatile capabilities for prefetching data from memory. The TM3270's load/store unit can read or write unaligned data as fast as it reads or writes aligned data, and it can do so using only one instruction. That's a valuable feature for a media processor, because audio and video data aren't always aligned on memory boundaries.

To compensate for the lack of an L2 cache—a sacrifice for low power—the TM3270's L1 data cache is much larger than the L1 data caches in other TriMedia processor cores: 128KB versus 16KB. (Smaller cache configurations are possible, but performance suffers; more on this later.) The 128KB data cache is four-way set-associative and organized into 128-byte lines. It supports the new allocate-on-write miss policy introduced with the TM5250, which reduces the write-miss penalty and saves power by requiring fewer memory accesses. The TM3270's data cache also supports the improved prefetching scheme introduced with the TM5250. That scheme allows programmers to define up to four memory regions, each with its own starting address, ending address, and memory stride. (See *MPR 11/3/03-01*, "Philips Powers Up for Video.")

Surprisingly, in view of its lower power consumption, the TM3270 has more function units than any other TriMedia processor core. In all, the TM3270 has 32 function units, including a wealth of arithmetic/logic units, two DSP units, and multiple FPUs supporting single-precision IEEE 754 floating-point operations. In contrast, the TM5250 has 29 function units, and the older TM3260 has 27.

To reduce power consumption without sacrificing potential for high clock frequencies, Philips reworked the TM3270 pipeline. Depending on the type of instruction, the pipeline varies in depth from 7 to 12 stages. That's noticeably deeper than the TM3260 pipeline (5 to 7 stages), but not as deep as the TM5250 pipeline (11 to 16 stages). Consequently, the TM3270 can reach higher clock speeds than the TM3260, but the TM5250 remains the speed demon of the TriMedia family, even when fabricated in an older CMOS process. Table 1 summarizes the features of the TM3270, TM3260, and TM5250.

Boosting Performance While Saving Power

It's clear that the TM3270 isn't simply a downsized version of an existing TriMedia core, ruthlessly defeatured to save

power. Philips had to improve performance at the same time. Although the TriMedia architecture was designed from inception for multimedia processing, those workloads have grown more demanding in the past 11 years.

Consider the evolution of digital-video codecs, which divide video frames into blocks of pixels and record any motion in those blocks between frames. MPEG-2 encodes a motion vector in every 16 × 16 block of pixels. MPEG-4 can encode a motion vector in every 8 × 8 block of pixels. H.264 Advanced Video Coding (AVC)—the new codec adopted by both of the next-generation high-definition DVD standards (HD-DVD and Blu-Ray)—can encode a motion vector in every 4 × 4 block of pixels. Meanwhile, as the number of pixel blocks has increased, so have the video resolution and compression ratios of the bitstreams.

Philips uses several techniques to reduce power consumption in the TM3270. Certainly, the shorter pipeline helps, as does eliminating the L2 cache. Another factor is clock gating, which divides the core into individually controllable power domains. The TM3270 has 170 domains, compared with 49 domains in the TM3260. Every pipeline stage in every function unit is gated, so they shut down when not needed.

Another power saver is the 90nm CMOS fabrication process that Philips will use to build Nexperia chips around the TM3270. This process employs transistors with a relatively high threshold voltage (V_t), which reduces static current leakage at the expense of some clock-frequency headroom. To reduce active power, the chips can dynamically scale their 1.2V (typical) supply voltage to lower voltages, all the way down to a guaranteed minimum of 0.8V. Of course, the chip must also reduce its clock speed in step with the lower voltages, but power-management software can control the voltage/frequency scaling to match performance requirements. The TM3270's ability to operate at 33% less voltage is important, because voltage is a squared term in the power-consumption equation ($P = CV^2f$).

Philips TriMedia TIM3270 Module	Die Area (mm^2)	Power @ 1.2V (mW/MHz)	Power @ 0.8V (mW/MHz)
Instruction Fetch Unit	1.46	0.272	0.121
Instruction Decoder	0.05	0.022	0.010
Register File I/O	0.97	0.107	0.048
Execution (All Units)	1.53	0.255	0.113
Load/Store Unit	3.6	0.266	0.118
Bus Interface Unit	0.24	0.002	0.001
Memory-Mapped I/O Peripherals	0.23	0.012	0.005
TOTAL	8.08	0.936	0.416

Table 2. Philips measured the TM3270's power consumption on a simulation of the synthesized core while running an MP3 audio decoder on a 384Kb/s bitstream (44.1kHz stereo). The processor's typical operating voltage in a 90nm CMOS process is 1.2V, but it can run on as little as 0.8V. Decoding this MP3 stream requires about 8MHz of processor overhead, so active power consumption is only about 7.5mW at 1.2V and 3.3mW at 0.8V for this workload.

There's no custom-circuit design in the TM3270. It's a fully static, fully synthesized core. Except for hand-placing the cache memories, Philips used standard place-and-route tools. Therefore, the design should be easily portable to other fabrication processes. To test power consumption, Philips used the Synopsys Power Compiler with a gate-level model simulated at 1.2V and 0.8V. The simulator ran an MP3 audio decoder at a high-fidelity bit rate (384Kb/s, 44.1kHz stereo), which greatly exceeds the quality of most

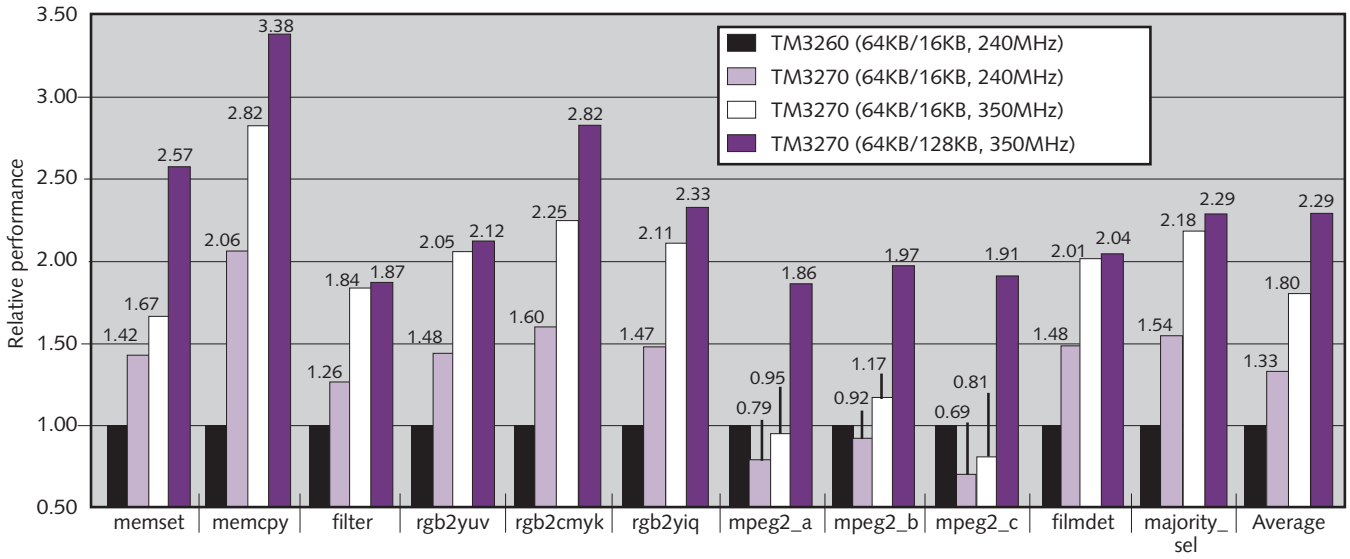

Figure 1. Even at the same clock frequency and with a data cache downsized to match the existing TM3260, the new TM3270 is a faster processor—and it consumes less power, too. Increasing the clock speed to the maximum worst-case specification and enlarging the data cache to 128KB produces bigger gains. Overall, the TM3270 is about 2.3 times faster than its predecessor when running the same source code without optimizations. If programmers optimize the source code with new instructions, Philips estimates the TM3270 will be two to four times faster than the TM3260.

downloaded MP3 files. (Bit rates of 64Kb/s to 160Kb/s are most common.) Table 2 shows the results, with breakdowns for each major part of the processor core.

To demonstrate that reducing power needn't reduce throughput, Philips tested three different simulations of the TM3270, using internal benchmark programs and kernels from EEMBC benchmark suites. Philips simulated one TM3270 at 240MHz with a 64KB instruction cache and a 16KB data cache—the same specifications as its predecessor, the TM3260. The second simulation boosted the TM3270 to its maximum worst-case clock frequency of 350MHz. The third simulation enlarged the TM3270's data cache to its normal 128KB. For all these tests, Philips recompiled the existing TM3260 source code without optimizing it for the TM3270's new features. In most cases, even at the same clock frequency, the TM3270 outran the TM3260. As expected, the 350MHz simulation with the full-size data cache chalked up the best scores. Figure 1 shows the benchmark results.

New Instructions Optimized for Video

Although the TM3270 requires programmers to recompile existing TriMedia software for upward compatibility, it conforms to the same basic instruction format of previous TriMedia processors. Each instruction word contains as many as five operations, and each operation can be up to 42 bits long. To save memory and I/O bandwidth, TriMedia instruction words aren't fixed in length, as some other VLIW formats are. Each instruction word begins with a 10-bit template that indicates which issue slots in the following word have useful operations. When the compiler can't match a slot with an available function unit, it encodes the template to indicate a NOP (no operation) in that slot. NOPs are so compact that instruction words can require as few as 16 bits (five NOPs, plus the template). The longest TriMedia instruction words can be 224 bits long (five 42-bit operations, plus the template).

Philips has added about 40 new operations to the TM3270's instruction set, mostly to improve digital-video decoding. The most interesting new operations fall into three groups: "super" two-slot operations, collapsed loads, and special operations for decoding bitstreams compressed with Context-based Adaptive Binary Arithmetic Coding (CABAC, a compute-intensive compression algorithm integral to H.264).

Two-slot operations are resurrected from the aforementioned TriMedia DSPCPU64 ISA, never implemented by Philips. (See *MPR 10/26/98-07*, "Philips Advances TriMedia Architecture.") They form a single operation spanning two of the five VLIW issue slots, and they execute in two different function units associated with those slots. In effect, two-slot operations are single instructions that do the work of two instructions, somewhat like the fused multiply-add (MADD) instructions in some RISC architectures. Because two-slot operations execute in two different function units, and because each function unit has its own ports to the register file, these operations can manipulate up to four 32-bit source operands and store results in two 32-bit destination registers. That's twice as much register bandwidth as a typical 32-bit RISC instruction, which can manipulate only two source operands and store the result in a single destination register.

For instance, the new super_dualimix operation (most two-slot mnemonics begin with "super") performs a pairwise two-taps filter on four 16-bit signed operands. It finds the smallest and largest operands within a signed 32-bit range and returns each result to a separate destination register. In all, super_dualimix performs four 16-bit multiplies and two 32-bit additions, and clips the results to the desired range—in only four clock cycles. Without super_dualimix, the same computations would require three separate operations and six clock cycles. These operations are useful for calculating pixel motion.

Some two-slot operations are loads. The super_ld32r operation loads two consecutive 32-bit values from memory and copies them into any pair of registers. Normally, loading two 32-bit values would require two separate operations in a TriMedia processor—and still does, if the sources aren't in consecutive memory locations. Much of the data in video bitstreams is likely to be consecutive. Although some other processors have 64-bit load instructions for retrieving consecutive 32-bit values from memory, they must copy the values into consecutive registers, which becomes a resource-dependency problem if those registers aren't available.

CABAC Operations and Collapsed Loads

CABAC decoding deserves special attention because it's a highly effective but compute-intensive compression method. CABAC bitstreams are sequential streams of data that expose little or no parallelism to SIMD instructions in RISC processors. Indeed, CABAC decoding is so difficult that some digital-video decoders don't even attempt to tackle it, instead offloading the heavy lifting to a separate stream processor.

Not so the manly TM3270. It has two new operations specifically for CABAC decoding: super_cabac_ctx and super_cabac_str. The first operation fetches four input operands from the registers and stores results in two destination registers. The second operation fetches three input operands and also stores results in two destination registers. Even with so many input operands, these CABAC operations must pack multiple 16-bit values into 32-bit registers to provide all the inputs this wickedly complicated algorithm requires. Remarkably, these two-slot operations have an execution latency of only four clock cycles. According to internal Philips benchmarks, the new CABAC operations help the TM3270 decode a D1-PAL video stream (720 × 576 pixels, 25 frames per second) 1.5 to 1.7 times faster than a program written without them.

The new collapsed loads are similar to the two-slot operations in that they combine multiple operations into one. However, collapsed loads don't require two issue slots. They are also very specific: they always combine a load with a linear interpolation function. A representative example is ld_frac8, which replaces at least two 32-bit loads and the two or more arithmetic instructions needed by a typical DSP. As

Figure 2 shows, ld_frac8 loads five consecutive bytes from memory (two unaligned loads), performs a pairwise interpolation based on a specified fractional position, and returns four interpolated byte values in a single destination register. (It's useful for horizontal pixel interpolation in digital video.)

Critics might accuse Philips of using the new TM3270 instructions to reinvent CISC. It's true that the two-slot operations perform tasks complex enough to require microcoded instructions in a CISC architecture, like the rarely used string instructions in the x86. It's also true that TriMedia operations are variable in length, like CISC instructions. Also like most CISC instructions, the TM3270's new operations typically have longer execution latencies (four to six clock cycles). And the collapsed loads are reminiscent of the old CISC load/store model, which often combined arithmetic operations with loads and stores. However, the TM3270's new instructions are so useful for video processing that only a RISC or VLIW purist would assign guilt by association.

Competitors, They Are Legion

In theory, the TM3270 competes with three other video-decoder cores or processor extensions recently analyzed by *MPR*, as well as with licensable processor cores, extensions, and accelerators from other intellectual-property (IP) providers.

At Fall Processor Forum in October, ARC International, Tensilica, and Videantis all presented similar technology. ARC revealed its new audio/video extensions for the ARC 700 configurable-processor core (see *MPR 11/21/05-01*, "ARC Shows SIMD Extensions"); Tensilica gave the audience a peek at its new dual-core video decoder (see *MPR 11/28/05-01*, "Tensilica Previews Video Engine"); and German startup Videantis introduced two licensable video decoders, including one for low-power mobile applications (see *MPR 11/7/05-01*, "Videantis Chases Digital Video").

In addition, ARM presented its new superscalar Cortex-A8 processor core with optional Neon extensions at FPF. (See *MPR 10/25/05-02*, "Cortex-A8: High Speed, Low Power.") Last year, ARM introduced a licensable coprocessor core that developers can configure for digital video. (See *MPR 6/7/04-01*, "ARM's Configurable OptimoDE.") At Spring Processor Forum 2005, MIPS introduced its new 24KE processors with DSP extensions (see *MPR 5/31/05-01*, "The MIPS 24KE Family") and more recently announced a deal that will bring Sarnoff Corp.'s synthesizable video accelerators to the MIPS architecture.

Everything described above is synthesizable IP licensed to chip designers, mainly for SoCs. Philips is willing to license the TM3270 likewise, even though the TriMedia IP spin-off came to naught. (See *MPR 5/19/03-03*, "TriMedia Comes Home.") However, Philips isn't aggressively marketing the TM3270 as licensable IP and will sell it only to customers considered noncompetitive with Philips's own products. That caveat would seem to severely limit the number of possible customers, because Royal Philips Electronics is a huge consumer-electronics company with many digital-video products.

Therefore, the TM3270 will find its place mainly in Nexperia media processors introduced in 2006 as standard parts. Philips already sells several Nexperia media processors built on previous TriMedia cores, including the latest PNX1700, which contains the TM5250 core. (See *MPR 4/18/05-02*, "Philips Debuts Media Processor.") As off-the-shelf chips, Nexperia processors offer a big advantage over licensable IP: the hardest work is already done. There's no need to launch an SoC or ASIC project, which would cost several million dollars, take 12–18 months, and entail a great deal of development risk. The time-to-market advantage of a standard part is obvious.

The disadvantages of using a standard part, of course, are that off-the-shelf chips aren't tailored for specific applications and are available to everyone. Developers can optimize custom chips for specific products and achieve greater differentiation. A compromise is to use standard parts for first-generation products while developing custom parts for following products, if the product line is successful. That's what Apple might be doing with its new video iPod. Teardowns suggest that the iPod has a standard-part video-decoder chip (Broadcom's VideoCore II BCM2722) whose functions could be merged with the ARM-based control processor in a future SoC.

Sizing Up the Competition

In some ways, future Nexperia chips based on the TM3270 might compete with Nexperia chips already available from Philips. "Nexperia" is an umbrella brand for Philips media processors and isn't specific to any CPU architecture. Some Nexperia chips have ARM, MIPS, or DSP cores, and some

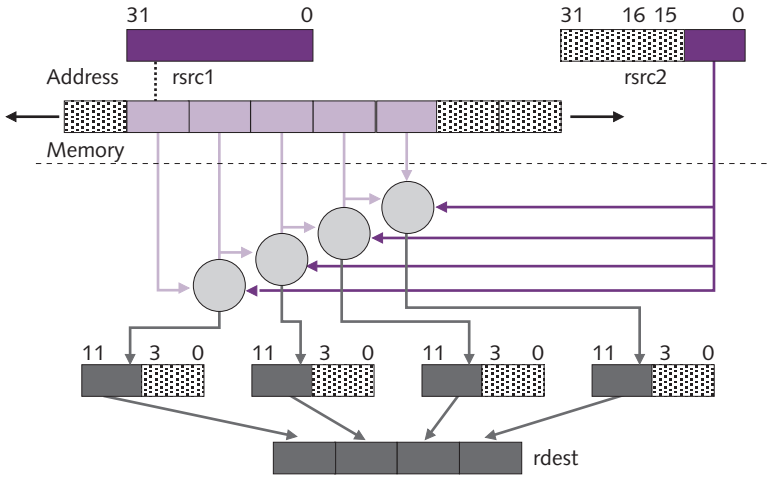

Figure 2. Among the approximately 40 new instructions in the TM3270 is ld_frac8, a collapsed-load operation that loads five bytes from memory and performs a linear interpolation on them before saving the four-byte result in a single 32-bit register. In all, it performs eight multiply-adds, four subtracts, and four divides in six clock cycles. This instruction can load unaligned data and is fully pipelined, so the processor can start a new operation every cycle.

Price & Availability

Philips Semiconductors will license the TriMedia TM3270 processor core as synthesizable IP to customers that don't compete directly with other products from Royal Philips Electronics, but IP licensing isn't the main goal. In 2006, Philips plans to introduce Nexperia media processors using the TM3270 core. Those standard parts will be announced later. For more information about the TM3270 core, visit *www.semiconductors.philips.com/news/content/file_1199.html*.

For more information about CABAC, see "Context-Based Adaptive Binary Arithmetic Coding in the H.264/AVC Video Compression Standard," published in *IEEE Transactions on Circuits and Systems for Video Technology*, July 2003.

are intended for low-power applications, as the TM3270-based Nexperia chips will be. However, the TM3270 appears to deliver more video-processing power per watt than the cores in existing Nexperia devices. Unlike an existing ARM- or MIPS-based Nexperia processor, the TM3270 can decode CABAC bitstreams and meet the other demands of H.264 video at D1 resolution while conserving enough power to be viable for a portable video player running on batteries.

When judged solely as a video-processor core, the TM3270 compares favorably with other synthesizable video processors, although the default configuration is a little larger, after accounting for the advantage of a smaller fabrication process. For instance, ARC's presentation at FPF showed a floor plan of a low-power video decoder built around an ARC 750D configurable-processor core and new SIMD extensions. It requires 9mm^2 of silicon when fabricated in TSMC's 0.13-micron LVLK-OD process, and the worst-case clock frequency is 500MHz. ARC's design includes L1 instruction and data caches for the processor, plus separate instruction and data memories for the SIMD unit—a total of 106KB of SRAM. The default configuration of the TM3270 with a 64KB instruction cache and a 128KB data cache (192KB total SRAM) requires about 8mm^2 of silicon and has a worst-case clock frequency of about 350MHz, even when fabricated in a more advanced 90nm process.

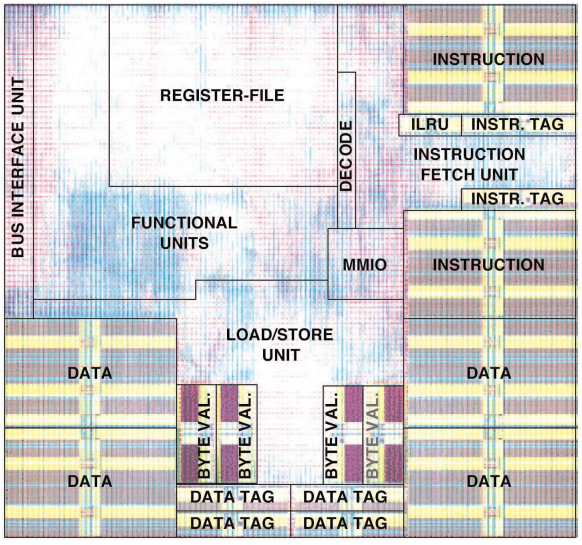

Figure 3. This floor plan shows the default configuration of the TM3270 core with a full-size 64KB instruction cache and 128KB data cache. After place and route, it occupies 8mm^2 of silicon in a low-power 90nm CMOS process. Smaller designs are possible by shrinking the caches and sacrificing some performance. The TM3270 is fully synthesized; only the cache memories were placed manually.

If the ARC 750D processor with SIMD extensions and memories is fabricated in a generic 90nm process, ARC says typical power consumption is 80mW at 533MHz. That would be much lower than the power consumption of a TM3270 at any similar clock speed, according to the Philips data in Table 2. But ARC's estimate is vague "typical" power consumption, not power for a specific workload, as Philips has provided.

Philips notes that the TM3270 targets a special low-power 90nm process. If ported to a high-speed 90nm process, the TM3270 could run at twice the clock speed—about 700MHz. But there's no reason to aim for such a high clock frequency, because the processor would use more power, and it's already fast enough for its intended applications.

Tensilica's dual-core video decoder won't be much larger than ARC's single-core design, judging from their gate counts. Tensilica estimates 10.5mm^2, including memories, in a generic 0.13-micron process. According to Tensilica's internal benchmarking, the video engine needn't run faster than 200MHz, even when decoding H.264 video at D1 resolution. That will reduce power consumption, especially at lower voltages. Both the ARC and Tensilica video decoders are capable of CABAC decoding, like the TM3270. In Tensilica's case, one Xtensa LX core is the stream processor, and a differently configured Xtensa LX core is the pixel processor. ARC's video decoder performs both tasks on a single processor core running at a higher clock speed.

The new v-MP2000M video-decoder engine from Videantis doesn't do CABAC; it requires a separate stream processor. In compensation, the v-MP2000M occupies only 2.61mm^2 in a 0.13-micron process, including memories. Its maximum worst-case clock frequency is 300MHz, but it needn't run faster than 150MHz while decoding H.264 video at D1 resolution. Videantis says typical power consumption for that task is 90mW. Even with the addition of a stream processor, a video decoder built with the v-MP2000M should require a little less silicon than the TM3270 does.

Weighing Capability vs. Size and Power

One criticism of VLIW is that it uses silicon less efficiently than RISC does; all the other cores described above are RISC

architectures. However, these comparisons amount to splitting hairs. The differences may add up to one or two square millimeters of silicon. Besides, Philips says that smaller configurations of the TM3270 can match the capabilities of video processors from companies like ARC, Tensilica, and Videantis while sacrificing only a little performance.

As Figure 1 shows, a TM3270 with a 16KB data cache performs almost as well on most benchmark tests as a TM3270 with a full-size 128KB data cache. It's also possible to shrink the instruction cache to 32KB instead of using the default size of 64KB. Depending on the cache configuration, Philips says the die-size range of the TM3270 is 3.36mm^2 to 5.6mm^2 before place and route, and 4.8mm^2 to 8mm^2 after place and route. Figure 3 shows the floor plan of the core layout with full-size caches. Even though it requires significantly more silicon, Philips favors the default configuration, which saves power by minimizing cache misses and off-chip memory accesses.

Furthermore, Philips argues that the TM3270 is a better all-around processor core than dedicated video engines (like the v-MP2000M) and video engines based on extended RISC architectures (like the ARC 750D and Tensilica Xtensa LX). The TM3270 is suitable for more applications and can easily handle audio/video encoding and transcoding (simultaneous decoding/encoding between two different standards). At standard resolution, the TM3270 can encode MPEG-2, MPEG-4, H.264, and DivX video streams. It can apply some video-enhancement algorithms—such as advanced deinterlacing—while decoding video. ARC says its 750D-based video engine will be capable of encoding some video codecs, at the cost of higher clock speeds and power consumption. Tensilica says its video engine will require additional custom extensions and two more processor cores (for a total of four) to tackle video encoding.

The TM3270-based Nexperia chips appearing next year may have other features, such as integrated peripherals, that make them more attractive in the context of a whole system design. And, of course, the Nexperia chips will be available off the shelf at least a year before any video decoders using the new licensable-IP cores hit the market. For some customers, that's the difference that matters.