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MICROPROCESSOR REPORT

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VIDEANTIS CHASES DIGITAL VIDEO

Synthesizable Video Coprocessors Pursue Emerging Applications

By Tom R. Halfhill {11/7/05-01}

Gil Scott-Heron famously said the revolution will not be televised, but now it's looking like television *is* the revolution. TV is appearing everywhere, it's affecting everyone's lives, everyone is watching it, and it's watching everyone. In other revolutions, heads roll; in this one, heads talk.

Video is moving beyond the living room and into vehicles, phones, and pockets. It travels by terrestrial broadcasts, satellites, downloads, and discs. Only the oldest delivery methods are analog, and their days are numbered. Some applications, like big-screen TVs, are relatively insensitive to cost and power consumption. In other applications, like mobile phones and Apple's new video iPod, every cent and milliwatt matters. Little wonder we're seeing feverish new development in fixed-function video chips, programmable media processors, licensable processor cores with video capabilities, media extensions for general-purpose microprocessors, DSPs, ASSPs, and FPGAs.

Into this maelstrom jumps Videantis, a startup based in Hannover, Germany. At **Fall Processor Forum 2005**, Videantis CEO Hans-Joachim Stolberg unveiled two synthesizable video-coprocessor modules based on the same proprietary processor core. Videantis wants to license the modules and optimized software to designers building programmable video chips for high-definition television (HDTV) and mobile consumer electronics.

Despite a burgeoning market, finding customers won't be a snap. Videantis competes directly with numerous other companies licensing processor cores for video applications, as well as with consumer-electronics giants in Europe, Japan, Korea, Taiwan, and China that frequently use their own custom processors. Videantis hopes to convince them that licensing a configurable video-processor module as synthesizable intellectual property (IP) will save many months of custom design work.

To reach both ends of the video market, Videantis is offering two synthesizable modules: the low-power v-MP2000M for mobile video and the higher-performance v-MP2000HD for home HDTV. Both are based on the v-MP2 processor core from Videantis. The v-MP2, not licensed separately, is a second-generation design optimized for the latest digital video codecs. Videantis also provides optimized codecs and software-development tools.

Making Trade-Offs for Digital Video

Fixed-function ASICs generally provide the best performance in any application, including video, but they lack flexibility. Digital-video standards are evolving rapidly, and standards vary in different parts of the world. For those reasons, product developers often favor programmable chips, despite their lower performance. ASSPs, DSPs, media processors, and general-purpose processors with media extensions are programmable and readily available off the shelf, but they may not be suitable for a particular product design—especially cutting-edge products that chip vendors didn't anticipate. FPGAs offer the ultimate in flexibility but are relatively expensive.

Occupying the middle ground are programmable processor cores designed for integration in custom chips. Some are licensable as hard macros or soft IP. Some are

configurable at design time to a greater or lesser degree. All are relatively flexible and capable of delivering good performance in video applications. Their main disadvantage is they require spinning custom silicon, which is expensive, risky, and time-consuming. Nevertheless, Videantis believes that a programmable, configurable, and synthesizable video-processor core is the best overall solution, especially while standards are in flux.

Last year, Videantis introduced its first video core, the v-MP1, and the first coprocessor module based on it, the v-MP1000M. The v-MP1000M is for low-power mobile video applications, especially those using MPEG-4 Simple Profile (SP) and Advanced Simple Profile (ASP). Since then, the H.264 video codec has become a rising star. H.264 (officially known as MPEG-4 Part 10 Advanced Video Coding) delivers noticeably better video quality than MPEG-2 at equivalent bit rates, but it's more computationally demanding. So is MPEG-4 (officially known as MPEG-4 Part 2). To meet the higher performance requirements of these codecs, Videantis created the v-MP2 core.

The core architecture is little changed. Both the v-MP1 and v-MP2 are based on a proprietary dual-issue VLIW architecture that Videantis defined specifically for video. The v-MP2 instruction set expands on the v-MP1's instructions, so it's compatible with existing v-MP1 software. (Videantis doesn't publicly disclose the instruction set.) In addition to having new instructions, the v-MP2 is configurable with two vector units instead of one, and it's designed to enable multicore implementations. As a result of these improvements, Videantis says the v-MP2 core is about twice as fast as the v-MP1.

Although Videantis describes the architecture as VLIW, the instruction words are only 64 bits long, which hardly qualifies as "very long." Each of the v-MP2's 64-bit words may contain two vector instructions, two scalar instructions, or one instruction of each type. Vector and scalar instructions have independent datapaths, complete with their own instruction decoders and register files. When configured with two vector units—which are actually groups of subunits for executing common vector functions—the v-MP2 can execute two vector instructions in parallel. Like the SIMD extensions for most RISC and CISC architectures, these vector units can handle multiple datatypes: 2×32 bits, 4×16 bits, and 8×8 bits. Figure 1 shows a block diagram of the v-MP2 core.

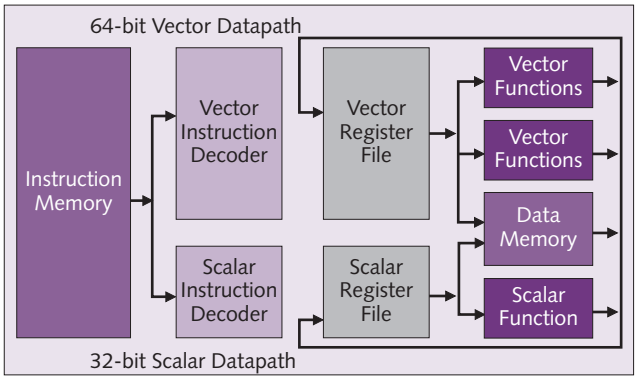

Figure 1. This block diagram of the v-MP2 core illustrates the dual datapaths for scalar and vector instructions. Although both datapaths fetch words from the same instruction memory, they have their own instruction decoders and register files. The blocks labeled "Vector Functions" and "Scalar Functions" are actually groups of subunits that perform various arithmetic and logical operations, such as integer math, shifts, and multiply-accummulate (MAC) operations. The v-MP2 core is configurable with one or two blocks for vector functions.

All function units in the v-MP2 are pipelined for single-cycle instruction throughput. The scalar units have five-stage pipelines, and the vector units have six stages. Internal datapaths allow the scalar units and vector units to exchange operands between their register files in a single clock cycle. Some vector instructions can fetch four source operands from the vector register file and store the results in two destination registers in a single cycle. To allow this, the vector register file has four read ports and two write ports, whereas the scalar register file has two read ports and one write port.

Configurable Features, Scalable Performance

Videantis offers customers a few configuration options for the v-MP2. Customers can choose either one vector unit or two and specify the size of the vector register file (32×64 bits or 64×64 bits), instruction memory (16–32KB), and data memory (4–8KB). In addition, Videantis preconfigures the instruction set, depending on the customer's target application. For low-power mobile applications, the v-MP2 has a somewhat smaller instruction set capable of handling H.264, MPEG-4, and Real Video up to D1/VGA resolution. For higher-performance home applications, Videantis adds more instructions for handling H.264, Windows Media, and MPEG-2 codecs at 1080i resolution.

These configuration options fall well short of the flexibility offered by some competitors, notably ARC International, MIPS Technologies, and Tensilica. Although the synthesizable cores licensed by those companies are general-purpose RISC processors, not video processors, they have optional audio/video extensions and DSP extensions, and they allow customers to define their own instructions, among other features. (See *MPR 6/21/04-01*, "ARC 700 Secrets Revealed," and *MPR 7/12/04-01*, "Tensilica's Automaton Arrives.") MIPS processors are somewhat less configurable than those from ARC and Tensilica, but they are more configurable than the Videantis v-MP2. (See *MPR 5/31/05-01*, "The MIPS32 24KE Core Family.") ARM's processor cores aren't very configurable, but ARM does license the OptimoDE data engine, a configurable coprocessor suitable for media applications. (See *MPR 6/7/04-01*, "ARM's Configurable OptimoDE.")

Instead of trying to match the broad configurability offered by those competitors, Videantis created the v-MP2 as a special-purpose core that, from the start, is optimized for

video. Videantis sees general-purpose RISC cores as useful stream-control processors for which the v-MP2 is a muscular coprocessor. The v-MP2 needs no custom extensions to serve the video applications for which it was designed, and it may be less intimidating for some chip designers because Videantis configures the core before delivering it. Indeed, Videantis won't even license the v-MP2 core as a discrete block. Videantis packages the core as a synthesizable coprocessor module preconfigured to customer specifications for either low-power video or high-performance video. Designers needing more flexibility can find it elsewhere, if they don't mind getting their hands dirty with processor-configuration tools.

Videantis licenses two coprocessor modules based on the v-MP2 core: the v-MP2000M for low-power mobile video and the v-MP2000HD for home HDTV. The v-MP2000M is a single-core coprocessor that communicates with a stream processor through shared on-chip memory and with other on-chip components over a 32- or 64-bit AMBA Advanced High-speed Bus (AHB). Videantis provides this coprocessor with a generic memory interface to an intercore memory that customers must integrate into the stream processor's memory map. The v-MP2000M also has a DMA controller for moving data in and out of shared memory. Figure 2 shows a block diagram of the v-MP2000M.

The fully synthesizable v-MP2000M has about 120,000 logic gates and occupies 2.61mm^2 of silicon in a 0.13-micron CMOS process. The die area includes instruction and data memories configured for their minimum sizes (16KB for instructions, 4KB for data). The v-MP2000M can reach 300MHz (worst-case) in a 0.13-micron process and typically consumes 90mW while decoding H.264 Baseline Profile (BP) video at D1 resolution (720 × 480 pixels NTSC, 720 × 576 pixels PAL).

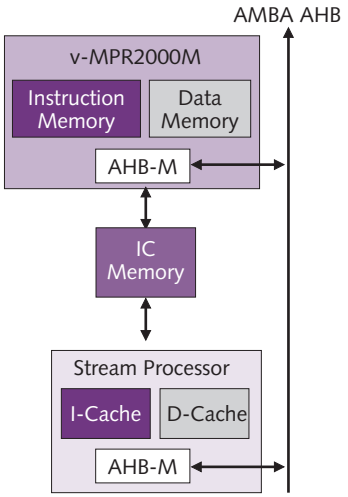

Figure 2. The v-MP2000M video coprocessor module includes the v-MP2 processor core with instruction and data memories, plus a 32/64-bit AMBA AHB interface and a 32/64-bit generic intercore memory interface for sharing on-chip SRAM with the stream-control processor. Instruction memory has one read port and one write port, both 64 bits wide. Data memory has two read/write ports of the same width.

Multicore Processor for High-End Video

To provide the higher performance required for HDTV—bit rates can soar from 20Mb/s to 40Mb/s—the v-MP2000HD coprocessor module integrates three v-MP2 cores with a multilayer AMBA bus, shared intercore memories, and local scratchpad memory. Obviously, this larger coprocessor is intended for tethered video applications, not low-power mobile products. Figure 3 shows a block diagram of the v-MP2000HD.

The fully synthesizable v-MP2000HD has about 450,000 logic gates. Although Videantis hasn't yet fabricated a test chip, the company estimates that the v-MP2000HD will occupy 11mm^2 of silicon in a 0.13-micron CMOS process and reach 300MHz. To verify performance, Videantis has implemented the v-MP2000HD in an FPGA.

Making good use of three cores requires clever task partitioning. Videantis says the v-MP2000HD can simultaneously process an H.264 video stream on all three cores by assigning different tasks to different cores, according to the type of "slice." A slice is part of a video frame containing a variable number of macroblocks, which are variable-size blocks of pixels. H.264 has three types of slices: I-slices, for intraframe-predicted macroblocks; P-slices, for interframe-predicted macroblocks; and B-slices, for making interframe predictions based on more than one reference frame. (A common technique in codecs like H.264 is predicting how blocks of pixels will change from one video frame to another.)

Partitioning a complex task in this manner requires clever programming. There's no multiprocessing operating system to automatically divide the labor among multiple cores, because the v-MP2000HD (and the single-core v-MP2000M)

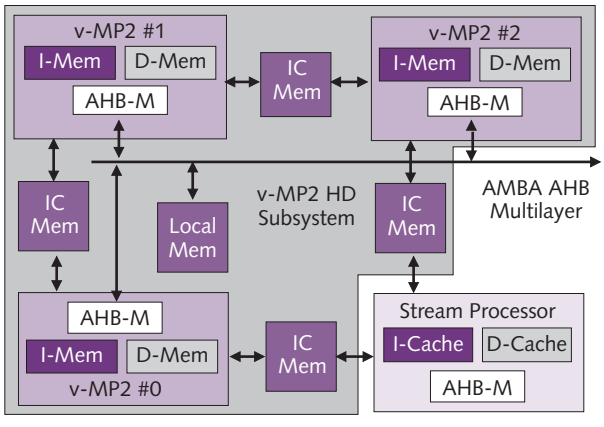

Figure 3. The v-MP2000HD video coprocessor module has three v-MP2 cores instead of one. The v-MP2 cores communicate with each other via shared intercore memories and a multilayer AMBA AHB bus. Two of the cores communicate with a stream processor through additional shared memories. An on-chip scratchpad memory (16KB) hangs off the AHB and is accessible by all the cores.

is strictly a video coprocessor—only the RISC control processor runs an operating system. Fortunately, Videantis provides optimized codecs for its processors. These are application-level codec packages, not merely low-level function libraries. Invoking the codecs requires relatively little effort on the part of programmers—for the most part, they simply pass the required parameters using wrapper code also furnished by Videantis. For programmers who want to modify the codecs, Videantis supplies a macro assembler and is working on a C compiler. To assist verification, Videantis offers a cycle-accurate simulator and a test suite. Of course, developers can also test the cores and their software in an FPGA.

Videantis hasn't benchmarked the v-MP2000M or v-MP2000HD using the new digital entertainment suite from EEMBC, which includes tests for MPEG-2 and MPEG-4, but not for H.264. (See *MPR 2/22/05-01*, "EEMBC Expands Benchmarks.") However, in response to a request from *MPR*, Videantis provided the performance data in Table 1.

Competitors Multiply Like Cable Channels

Videantis faces mountainous competition, because almost everyone wants a piece of the video market. With the transitions to digital TV and HDTV finally gaining momentum—driven by government regulatory pressure—hundreds of millions of analog TV sets may soon become obsolete or will require a digital receiver to work. At the same time, plunging prices of flat-screen technologies are making bulky picture-tube TVs seem as old-fashioned as wooden cabinet radios. Digital video recorders like TiVo are changing the way people watch TV. Mobile video is becoming a mania, and downloading video over the Internet will soon become as commonplace as downloading music.

Video Type	Videantis v-MP2000M	Videantis v-MP2000HD
MPEG-4		
Simple Profile Decoder VGA, 30 fps	60MHz	—
Advanced Simple Profile Decoder D1, 30 fps	150MHz	—
Simple Profile Encoder D1, 30 fps	130MHz	—
H.264 Advanced Video Coding (AVC)		
Baseline Profile Decoder VGA, 30 fps	150MHz	—
Baseline Profile Encoder D1, 30 fps	250MHz	—
High Profile Decoder 1080i, 60 fps	—	300MHz
Windows Media 9		
VC-1 Decoder 1080i, 60 fps	—	250MHz
MPEG-2		
Decoder 1080i, 60 fps	—	200MHz

Table 1. Using FPGA implementations of the v-MP2000M and v-MP2000HD, Videantis has estimated the minimum clock frequencies required for each video coprocessor to run the codecs in this table. Note that the H.264 High Profile Decoder doesn't include context-adaptive binary arithmetic coding (CABAC), which Videantis expects will be performed on the stream processor, not on the v-MP2000HD coprocessor.

One big obstacle for Videantis or any newcomer to this market is the not-invented-here syndrome. All the major consumer-electronics companies either design their own video processors or have relationships with partners designing the chips or supplying the cores. For instance, Sony codesigned the PowerPC-based Cell processor with IBM Microelectronics and Toshiba—and Sony plans to use the chips for other products, as well as for the PlayStation 3. (See *MPR 2/14/05-01*, "Cell Moves Into the Limelight.") IBM is already finding other customers for Cell, most recently inking a deal with Mercury Computer Systems to use the multicore processor for medical imaging and other specialized applications. (See *MPR 2/28/05-01*, "Editorial: Cutting Through Cell's Hype.")

Another example of in-house processor development is Matsushita's new scalable media architecture, which includes the Instruction Parallel Processor (IPP) and Data Parallel Processor (DPP). The purpose of this architecture is reduce the proliferation of different CPU architectures in the vast number of consumer products that Matsushita designs and sells under its Panasonic brand. However, Matsushita's media architecture may still require some extra horsepower for video processing. (See *MPR 6/20/05-02*, "Matsushita's Own Media Platform.")

Even when the big product companies do venture outside their walls for processors, they often select a major vendor capable of supplying chips off the shelf. A prominent example is Apple's video iPod. According to teardown reports, the iPod's video coprocessor is Broadcom's VideoCore II BCM2722, which encodes and decodes MPEG-4 at very low power levels and saved Apple the trouble of designing a custom chip, at least for the first-generation product. Videantis probably stands a better chance of getting into a leading-edge product like the iPod by courting a chip supplier like Broadcom rather than a product company like Apple. Note that Broadcom acquired the VideoCore technology by purchasing Alphamosaic last year.

Plenty of IP Competitors, Too

In addition to competing with consumer-product companies and large chip vendors, Videantis is going head-to-head with other processor-IP providers. Indeed, during the same FPF session in which Videantis presented the v-MP2, ARC and Tensilica introduced new audio/video extensions for their configurable processor cores. These extensions significantly boost performance, and both processors lend themselves to multicore designs.

MIPS, which introduced the MIPS32 24KE at Spring Processor Forum, probably has more design wins in video than ARC and Tensilica put together. (See *MPR 5/31/05-01*, "The MIPS32 24KE Core Family.") Silicon Hive's new Avispa-IM1 pixel processor is another contender (see *MPR*

6/20/05-01, "Busy Bees at Silicon Hive"), as is Elixent's D-Fabrix v2.0 configurable processor (see *MPR 6/27/05-02*, "Elixent Improves D-Fabrix"). One advantage for Videantis is that by focusing exclusively on video, and by limiting configuration options, the v-MP2000M and v-MP2000HD should require fewer logic gates than do more-exotic architectures and extended general-purpose processors.

Another competitor for Videantis is Imagination Technologies, whose PowerVR division licenses processor cores and optimized software libraries for video and graphics. Imagination's PowerVR M2VX and PowerVR MVED1 cores accelerate many of the same codecs as the Videantis processors and are especially suitable for mobile applications. PowerVR licensees include Freescale, Intel, NEC, Philips, Renesas, Samsung, Sega, Sharp, STMicroelectronics, and Texas Instruments—an impressive fan club. Imagination also has a long-running strategic relationship with ARM, the leading provider of 32-bit embedded-processor cores, which opens many doors for PowerVR. In favor of Videantis, the v-MP2000M and v-MP2000HD are fully programmable, unlike the PowerVR cores, and they are more optimized for video, whereas PowerVR is primarily intended for graphics. In addition, the triple-core v-MP2000HD is more suitable for HDTV than PowerVR is.

Although the challenge for a small startup like Videantis looks overwhelming, it's not hopeless. Rapidly growing markets often have windows of opportunity that don't close until the market consolidates. For a few years, at least, Videantis has a chance to win designs with equally opportunistic companies that haven't committed to a different solution. To win those designs, Videantis needs to get its foot in the door and assure prospective customers that it has enough staying power to fend off larger competitors.

Price & Availability

Both the v-MP2000M video coprocessor module for mobile applications and the v-MP2000HD video coprocessor module for HDTV are available for licensing now. The v-MP2 processor core, on which both modules are based, isn't licensed separately. The coprocessor modules include synthesizable VHDL or a presynthesized Verilog netlist, a macro assembler, and optimized video codecs. A cycle-accurate simulator is also available. Videantis doesn't publicly disclose upfront licensing fees or chip royalties.

For more information about the first-generation v-MP1 core, refer to a paper delivered by the University of Hannover at the International Solid-State Circuits Conference (ISSCC) in 2004: "An SoC with Two Multimedia DSPs and a RISC Core for Video Compression Applications" (session 18.3). For more information about Videantis, visit *www.videantis.com*.