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PREVIEW: FALL PROCESSOR FORUM 2005

Multicore Processing Dominates 18th Annual Conference

By Tom R. Halfhill {9/26/05-01}

Not since the days when RISC and VLIW challenged the CISC orthodoxy has there been such an upheaval in microprocessor design. Every major company in every major market—PCs, servers, and embedded systems—is converging on multicore processing. Reacting to the limits of high clock frequencies and torrid power consumption, multicore processors are the unavoidable future for new CPU architectures as well as for staid old architectures like the x86. And, like RISC and VLIW, multicore processing requires a fresh approach to programming and software-development tools.

Microprocessor Report has provided front-line coverage of the multicore revolution since its beginnings in the 1990s. Processor vendors have introduced numerous multicore chips at our semiannual forums. Now it's time to pull everything together for an event that covers all dimensions of multicore processing. The theme of **Fall Processor Forum 2005**, our 18th annual fall conference, will be "The Road to Multicore." FPF will offer technical presentations on new multicore processors, licensable intellectual property (IP) for multicore designs, on-chip interconnect technology for multicore chips, system software for multicore architectures, and software-development tools for parallel processing. FPF 2005 is the one-stop shop for engineers, engineering managers, project leaders, strategic planners, and marketers who need to quickly ramp up their knowledge of this fast-breaking technology.

The two-day conference will be held on Tuesday, October 25, and Wednesday, October 26, at the Doubletree Hotel in San Jose, California. (The Doubletree is conveniently located near San Jose International Airport and has plenty of free parking.) In addition to presentations on multicore technology, the conference will cover other topics, such as ARM's first superscalar embedded-processor core and a new single-transistor embedded-memory cell for microprocessors. Tuesday's sessions will be followed by the customary exposition and evening reception.

Participating companies include AMD, ARM, ARC International, Azul Systems, Broadcom, Cadence Design Systems, Freescale Semiconductor, Fujitsu, Fulcrum Microsystems, Green Hills Software, IBM Microelectronics, Innovative Silicon, Microsoft, P.A. Semi, Sonics, StarCore, Tensilica, Texas Instruments, Videantis, and XenSource.

Bracketing the two-day conference are daylong seminars for deep dives into specific technologies. On Monday, October 24, In-Stat principal analyst Max Baron will present a seminar entitled "Implementing Low-Power SoC Configurations." Baron will explain how system-on-chip vendors use architecture, microarchitecture, software, and power management to obtain the high performance required for mobile markets while achieving the best combination of power consumption, level of integration, and flexibility. This seminar will analyze and compare more than 25 cores, chips, and SoCs, including the latest introductions for cellphones, digicams, PDAs, and other low-power systems. As part of the seminar, UMC will give a foundry's point of view by presenting a section on low-power SoC technologies.

On Thursday, October 27, Baron will lead another seminar, "A Briefing on DSP Technology Presented by the Leaders." Technical experts from Analog Devices, Ceva,

StarCore, and Texas Instruments will present the latest information on digital-signal processing. Both all-day seminars are priced separately from the two-day conference. For FPF registration and pricing information, see the "For More Information" box or visit *www.in-stat.com/fpf/05/*.

Day One: New Multicore Processors

The conference kicks off with a keynote address by Mike Fister, president and CEO of **Cadence Design Systems**. Before joining Cadence, Fister spent 17 years at Intel, where he was most recently senior vice president and general manager of the Enterprise Platforms Group. Fister's keynote is entitled, "The Customers' Paradox: The Next Big Challenge in IC and Systems Design." He will encourage engineers to think beyond their immediate projects and start anticipating long-term trends that will shake up the semiconductor and consumer-electronics industries.

Following the keynote, *MPR* editor in chief Kevin Krewell will host an extraordinarily busy session for introductions of new multicore processors. In all, there will be six presentations, enough to fill the entire morning until lunch. These processors span a range of applications: high-performance servers, portable media devices, digital-signal processing, and general high-performance processing. Most of these presentations will be the first public disclosures.

Broadcom begins with "BMIPS4350: A Concurrent Multithreaded Core for Highly Integrated SoCs," by Kimming So, the architect of Broadcom's embedded-processor technology. Broadcom will introduce a MIPS32-based design with multiple thread processors that can operate asymmetrically in a master-slave configuration or symmetrically for shared-memory multiprocessing. The presentation will describe the organization of the concurrent multithreaded core and explain how the thread processors manage on-chip resources. In addition, the presentation will include data about the core's implementation and performance.

Fujitsu follows with "SPARC64 VI/VI+ Next-Generation Processor," by Takumi Maruyama, manager of enterprise server development. Fujitsu will describe vertical multithreading and reliability/availability/serviceability (RAS) features built into the dual-core SPARC64 VI and will evaluate the processor's performance. The SPARC64 VI is scheduled to debut in 2006. In addition, Fujitsu will discuss the future quad-core SPARC64 VI+ processor. (See *MPR 10/25/04-02*, "SPARC Turns 90nm.")


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IBM Microelectronics comes next with two back-to-back presentations. The first is "IBM's PowerPC 970MP: A New Low-Power High-Performance Dual-Core Processor," by Norman Rohrer, an IBM distinguished engineer who is the technology liaison and lead circuit designer for PowerPC processors. The PowerPC 970MP is a dual-core version of the PowerPC 970 chips used in Apple's G5-class Macintoshes. (See *MPR 10/28/02-02*, "IBM Trims Power4, Adds AltiVec.") IBM's second presentation, "Application-Customized CPU Design for the Microsoft Xbox 360," is by Jeffrey D. Brown, another IBM distinguished engineer, from IBM Engineering and Technology Services. Brown will reveal new technical details about the triple-core PowerPC chip designed for Microsoft's next-generation home videogame machine. (See *MPR 7/18/05-02*, "Powering Next-Gen Game Consoles.")

P.A. Semi will close the Tuesday morning session by breaking out of stealth mode. This Palo Alto–based startup, the subject of many rumors for the past two years, will publicly reveal its new processors for the first time in a presentation entitled, "A Power-Efficient, Scalable Processor Family." The presenter is Jim Keller, vice president of engineering for P.A. Semi's Architecture Group. P.A. Semi is the company led by Dan Dobberpuhl, the ex-Alpha designer who created the StrongARM and SiByte MIPS64 processor cores. Other P.A. Semi engineers were key designers of the Opteron, Itanium, and UltraSPARC processors. Will the rumors about a radical new multicore processor turn out to be true? Come to FPF and see.

Day One: Innovative IP and Multicore IP

After lunch is a special presentation, "Unshackling Innovation Through Multicore Architectures," by Scott Sellers, CTO of **Azul Systems**. This isn't a new-product introduction; it's a technical overview of the reasons that multicore designs are imperative for the future evolution of microprocessors and systems. Sellers is well qualified to speak on this topic because his startup company has designed specialized server processors with 24 processor cores on a single chip. (See *MPR 5/31/05-02*, "Multicore Showdown," and *MPR 2/14/05-02*, "Are Instruction Sets Irrelevant?")

Following the Sellers talk is a session entitled simply, "Innovative IP." Two companies will describe new products not specifically related to multicore design but sure to be interesting.

ARM begins with its presentation, "ARM's First Low-Power Superscalar Processor," which will introduce the long-awaited processor core code-named Tiger. Although ARM plans to officially unveil Tiger at its own developers' conference in early October, the company is saving important technical information about Tiger's microarchitecture for

FPF. ARM will reveal details about Tiger's superscalar pipelines and Neon media extensions, as well as some performance data. The speaker is David Williamson, the coarchitect and validation lead of the Tiger processor.

Innovative Silicon will deliver the second presentation in this session, "Using the Cinderella Effect to Integrate Z-RAM in Microprocessors." Mark-Eric Jones, president and CEO, will explain Innovative Silicon's new approach to embedding memory in processors and SoCs. Z-RAM memory cells require only one transistor and no capacitor, and they add no masks or steps to standard silicon-on-insulator (SOI) fabrication processes. Because Z-RAM lacks the deep trenches of embedded DRAM (eDRAM), it's easier to manufacture and readily scales to process geometries below 90nm.

Tuesday's final session, "Processor IP for Multicore," returns to the theme of this year's forum. Three companies will introduce licensable IP for single- or multicore chip designs.

ARC International begins with "ARC's New Multi-Standard Multimedia Subsystem," by Nigel Topham, the company's chief architect. ARC will disclose new extensions for the ARCompact instruction-set architecture that are optimized for algorithms in audio/video applications and codecs. This is a major extension package for the ARC 700 processor core, targeting low-power multimedia devices. (See *MPR 6/21/04-01*, "ARC 700 Secrets Revealed.")

Tensilica follows with its presentation, "A Programmable, High-Performance Video Engine With Multiple Processor Cores," by Gulbin A. Ezer, hardware-design manager. Tensilica will preview a dual-core derivative of its Xtensa LX processor that's optimized for video applications. It uses many of the bells and whistles in the Xtensa architecture, including new instructions created with Tensilica Instruction Extension (TIE) language, TIE queues, and Flexible-Length Instruction eXtensions (FLIX). (See *MPR 5/31/04-01*, Tensilica Tackles Bottlenecks.")

Videantis wraps up the session with "A Next-Generation Scalable Video Processor Core," by Hans-Joachim Stolberg, CEO. This German company will introduce its new VLIW core and two highly integrated multicore designs based on the core. One multicore design is optimized for mobile video applications, and the other targets high-definition video. Both multicore designs and the video-processor core will be available as synthesizable, licensable IP.

As is customary, the first day of the conference ends with an exposition and reception in the hotel ballroom. Admission is free for registered conference attendees; expo-only passes for others are $95.

Day Two: High-Level Multicore Design

The second day of the conference shifts gears and examines multicore processing from a higher level, including system design, system software, and software development. There will also be afternoon sessions about high-performance DSPs and on-chip interconnects.

Microsoft begins the day with a keynote address, "Software and the Concurrency Revolution," by Herb Sutter, software architect of the Microsoft Developer Division. Sutter will discuss the difficulties of developing software for multicore systems, including the new requirements for development tools and programmers. After Microsoft's keynote, *MPR* analysts Kevin Krewell and Jim McGregor will host the first session, "Building Systems With Multicore Processors."

AMD launches the session with a presentation entitled, "Pacifica: x86 Architectural Enhancements to Facilitate Virtualization." AMD Fellow Kevin McGrath—chief architect of the 64-bit x86 extensions—will describe these latest x86 extensions, which enable multiple software environments to run concurrently and independently. In particular, McGrath will describe the way virtualization works on future multicore server processors from AMD. This presentation is packed with previously undisclosed technical information.

Freescale Semiconductor will present "Asymmetric Multiprocessing in a Dual-Core Processor," by Toby Foster, system architect. Foster will discuss the trade-offs of asymmetric versus symmetric multiprocessing, using Freescale's new MPC8641D dual-core PowerPC processor as an example. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.") Important factors include cache coherency, atomic read-modify-write operations, resource sharing, interrupt handling, and the limits of multicore processing predicted by Amdahl's law.

Green Hills Software follows with "Facing the Software Challenges of Multicore Designs," by Neil Puthuff, director of hardware engineering. *MPR* invited Green Hills to FPF because designing a multicore processor is only the first step toward building a multiprocessing system, and Green Hills has a proven track record in multicore system software. After outlining the unpleasant realities of multicore software development and debugging, Puthuff will discuss some solutions, including the use of high-bandwidth debug ports as alternatives to conventional trace ports.

IBM comes next with a special presentation, "Design Considerations for the Cell Processor," by Dr. Alex Chow

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For More Information

For the latest information about pricing or to register online, visit *www.in-stat.com/fpf/05/*. Early-bird admission (before October 1) is only $995 for the conference and $795 for each seminar, with discounts for various conference-and-seminar packages. Conference attendees get free admission to the Tuesday night expo; otherwise, an expo pass is $95. For information about group discounts and answers to other event-related questions, please call Elaine Potter at (480) 483-4441 or write to *epotter@reedbusiness.com*.

and David Krolak. Chow is manager of the S-T-I (Sony-Toshiba-IBM) Design Center in the IBM Systems and Technology Group. Krolak is a development engineer with IBM Engineering and Technology Services. Their presentation will discuss software-design issues when programming for Cell processors.

XenSource wraps up this session with "Xen and the Art of Virtualizing Multicore Platforms," by Simon Crosby, vice president of strategy and corporate development. A rising star in virtualization, XenSource wants to unify the industry around a common open-source virtualization standard, implemented in the Xen hypervisor. XenSource's presentation will explain its virtualization technology, including Xen's ability to optimize workloads for multicore processors. In addition, XenSource will argue the case for adopting an open-source standard for virtualization instead of using a proprietary hypervisor.

Day Two: DSPs and On-Chip Interconnects

In-Stat principal analyst Max Baron hosts the next session on Wednesday afternoon: "High-Performance DSPs." This will be a short session, with only two presentations, followed by another brief session with two more presentations.

StarCore begins with "The StarCore V5 Architecture," by Amnon Rom, CTO and vice president of engineering. StarCore will introduce the newest version of its DSP architecture, which has many new instructions, deeper pipelining, improved power management, and other features.

Texas Instruments ends this session with "TMS320c672x DSP Brings High Floating-Point Performance for Mainstream Audio," presented by Amitabh Menon, an SoC architecture technology manager for TI in Stafford, Texas. A new family of DSPs designed for audio applications will have an improved memory architecture and floating-point enhancements. TI will disclose technical details about the on-chip megamodule and new floating-point instructions, in addition to presenting benchmark data.

The final session of the conference is "On-Chip Interconnects for Multicore." Both presentations in this session provide overviews of chip-level interconnect technology applicable to both single- and multicore designs.

Fulcrum Microsystems will present "GALS Interconnect: Delivering Transparent Connectivity for Multicore SoCs," by Uri Cummings, vice president of product development. GALS (globally asynchronous, locally synchronous) describes Fulcrum's unique on-chip interconnect technology, which uses asynchronous logic to link multiple processor cores and their peripherals together into a chip-level network. The asynchronous logic reduces bottlenecks between the higher-speed and lower-speed blocks of conventional synchronous logic.

Sonics ends the session and the two-day conference portion of FPF with "Advanced Dataflow Services for Heterogeneous Multicore SoCs," by Drew Wingard, CTO. Sonics has specialized in this technology since the company was founded in 1997, and customers include Broadcom, Flextronics, Fujitsu, Hitachi, Hughes, Intel, NASA, NEC, Nokia, Samsung, TI, and Toshiba. Wingard will describe the way synthesizable on-chip interconnect technology can simplify the design of complex SoCs having many processor cores and peripherals. (See *MPR 6/28/04-03*, "Interconnects Target SoC Design," and *MPR 12/22/03-01*, "Sonics Gains Acceptance.")

By offering technical presentations on many different dimensions of multicore processing—including microarchitecture design, coherency models, performance evaluation, concurrent operating systems, software development, and on-chip interconnects—FPF promises to be a worthwhile and educational event for engineers and others who need to come up to speed on this important technology.