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ACTEL MIXES SIGNALS ON FPGAS

Programmable Chips Will Integrate Analog, Digital, and Memory

By Tom R. Halfhill {8/15/05-01}

As design costs soar like housing prices, ASIC alternatives are multiplying like Realtors. Programmable-logic vendors gleefully show PowerPoint slides comparing the falling prices of FPGAs to the rising costs of zillion-dollar ASICs. Meanwhile, new varieties of structured ASICs, microprocessors with reconfigurable logic, and FPGAs with embedded processors are crowding into the market.

Actel—a second-tier FPGA vendor, behind market leaders Xilinx and Altera—is proving to be unusually creative at exploiting this opportunity. Earlier this year, Actel announced a new line of FPGAs with embedded ARM7-TDMI-S processor cores specially optimized for programmable logic. It's the first time ARM has agreed to license and optimize a synthesizable processor core for FPGA integration. (See *MPR 4/4/05-02*, "ARM-Based MCUs Flex Muscles.")

Now Actel is announcing a technology called Fusion that, for the first time, can integrate mixed-signal logic with an embedded-processor core, flash memory, and SRAM in the same programmable-logic device. With Fusion, a single FPGA could perform some or all of the analog- and digital-processing functions in an embedded system. In addition, Fusion chips will be run-time reconfigurable, capable of reprogramming some of their functions as often as every clock cycle.

To support Fusion, Actel will introduce new extensions for its Libero development tools. Those extensions will allow designers to program and configure the chips using little or no hardware description language (HDL). Libero's graphical screens will allow designers to integrate common analog and digital components provided by Actel or third parties as soft intellectual property (IP), and the IP will be reusable across multiple projects. Of course, designers can use HDL to create their own application-specific logic as well.

Actel plans to release the first Fusion FPGAs and tools in 1H06. The obvious benefits of these do-it-all chips will be higher levels of system integration, faster product cycles, and lower costs for projects whose volumes don't justify spinning an ASIC.

However, Actel faces some formidable challenges. One is integrating mixed-signal components, an embedded-processor core, and memory in a single FPGA without compromising performance. Another is providing development and verification tools equal to the task of designing a self-contained system on a single chip. Finally, Actel's pricing—yet to be announced—will be crucial. Fusion devices will compete against other FPGAs that can use external flash memory and against lower-priced standard-part microcontrollers.

High Voltage Enables Mixed Signals

FPGAs are popular in wireless base stations and other communications systems that convert analog radio-frequency signals into digital bitstreams and vice versa. To convert and process signals across the analog and digital domains, the system usually needs to surround the host processor and DSP with discrete analog components, plus some flash memory for program storage and DRAM or SRAM for data. Combining most or all those functions on one chip could cut costs, save power, and conserve board space. ASICs can deliver higher performance and are more economical than FPGAs

in larger volumes, but many communications systems aren't large-volume products, and rapidly evolving communications protocols tend to favor programmable chips that can change with the times.

Actel makes a plausible argument that its FPGAs are well suited for SoC integration. Actel is the leading supplier of flash-based FPGAs, which weave the programmable-logic fabric out of nonvolatile flash-memory cells. It's easy for the same chips to allocate additional flash cells for nonvolatile embedded memory, which is useful for storing program code that's upgradable in the field. Actel fabricates the FPGAs in a 0.13-micron process that combines flash-memory cells with conventional CMOS, so the chips can also incorporate high-performance SRAM for caching frequently used program code and data. These chips operate at clock speeds up to 350MHz.

Unlike some other FPGAs, Actel's flash-memory cells use high-voltage transistors that lend themselves to mixed-signal applications. Reprogramming the logic transistors requires 17V, which is generated on chip from an external 3.3V power supply. Such a high voltage tolerance allows the chips to accept input directly from analog circuits and to drive analog circuits without external voltage-scaling components. In addition, the transistors have a triple-well structure that tucks a flash-memory cell inside a p-well inside an n-well. The third well helps isolate the analog and digital signals from each other, reducing circuit noise.

With reprogrammable digital logic, nonvolatile flash memory, high-speed SRAM, and analog capabilities all integrated in the same chip, just about the only thing missing is a general-purpose processor—and Fusion FPGAs will make that feature optional. Initially, Actel will offer 32-bit ARM7TDMI-S and 8-bit 8051-compatible cores, possibly followed by other processors. Neither core will require a license from the core-IP vendor. In effect, the customary up-front license fee and manufacturing royalties are factored into the prices of the chips.

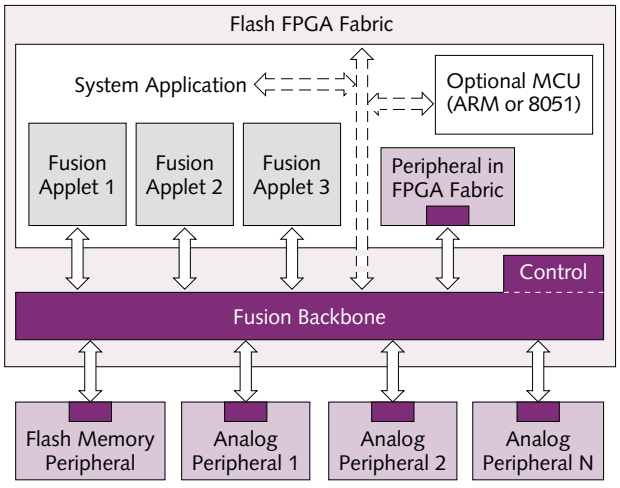

Figure 1. Actel's Fusion will integrate hard-wired analog peripherals with hard and soft intellectual-property (IP) cores in an FPGA. A soft embedded-processor core is optional. Tying everything together is the Fusion backbone, which consists of a multidrop bus and microsequencer implemented in programmable logic. The backbone is a possible bottleneck, but it can be bypassed by connecting a Fusion applet directly to an on-chip peripheral.

The Fusion ARM7TDMI-S core is a cacheless implementation, and—like the optional 8051-compatible core—it will be synthesized in the programmable-logic fabric, not etched into silicon as a hard core. Although soft cores implemented in this fashion occupy thousands of programmable gates and deliver significantly less performance than an embedded hard core does, they have proved much more popular than hard cores in FPGAs. Both Altera and Xilinx offer soft processor cores for their programmable-logic devices. (See *MPR 5/17/05-02*, "MicroBlaze Can Float," and *MPR 6/28/04-02*, "Altera's New CPU for FPGAs.")

Fusion's underlying technology is interesting, but the larger story is the way Actel is using the technology to integrate analog and digital functions on a single chip. Success will depend on how efficiently the various components communicate with each other through the fabric and how easily the development tools allow engineers to create and verify their designs.

Soft-Gate Backbone Ties Everything Together

Figure 1 is a block diagram of a Fusion FPGA, which is necessarily more complex than a conventional programmable device. Analog peripherals will be hard-wired on the chip, not implemented in the programmable fabric, but Actel says most will have user-configurable parameters. Other peripherals can be implemented in programmable logic or emulated in software running on an embedded-processor core, if one is present. The channelized peripherals can share resources among different tasks.

For now, Actel isn't disclosing the peripherals it will offer on Fusion devices. Most likely, they will be basic general-purpose components, such as PLLs, analog-to-digital converters (ADC), digital-to-analog converters (DAC), and voltage monitors. One clue is that Actel plans to make several different types of Fusion FPGAs, ranging from small to large devices. Small chips will be economical enough for multimillion-unit applications. Large chips will have enough programmable gates to embed a soft 32-bit processor, such as the ARM7TDMI-S, while sparing enough gates for the customer's application-specific logic.

Digital IP for Fusion FPGAs can be hard or soft. Actel refers to the soft-IP cores as Fusion applets: low-level self-contained function blocks designed to perform application-specific tasks or to support analog peripherals. An example of a Fusion applet might be a finite impulse response (FIR) filter or a function block that monitors a power-supply channel.

Fusion applets are reusable building blocks for embedded applications, and they have open I/O interfaces. Actel will provide some applets when introducing Fusion FPGAs, but the company hopes to seed a community of third-party suppliers, much like the ecosystems that have sprouted in the

open-source community. Developers can create Fusion applets by writing HDL for the programmable fabric or by writing software for the optional embedded-processor core.

To free system designers from low-level peripheral management, Fusion FPGAs have a smart backbone implemented in programmable logic. The backbone connects together any number of Fusion applets and peripherals. It can automatically set and clear a peripheral's flags, manage its buffers, and adjust performance parameters. In addition, the backbone can save a particular set of peripheral configurations for instant restoration after a reboot, and it can swap different sets of configurations as often as every clock cycle, allowing the chip to rapidly change its personality. All Fusion peripherals have an open, standard I/O interface to the backbone, easing third-party development.

One question yet to be answered is how efficiently a backbone implemented in programmable gates can operate. Obviously, the backbone won't be as fast as a custom-designed straight-wire interconnect on an ASIC. Actel's design tools will have to use clever automated routing to keep the backbone from resembling a maze, especially when numerous Fusion applets and peripherals must be wired together. Another unanswered question is whether a Fusion chip with an ARM7 processor core will have an AMBA-compatible Fusion backbone. For now, Actel says only that the ARM7 processor will be able to communicate normally with on-chip peripherals. Although the processor will run ARM7-compatible embedded operating systems, some customizing will be required to adapt the system software to the chip's peripheral configuration.

Actel's ambition for Fusion is to enable high-level system design on FPGAs. Ideally, customers will be able to construct an application-specific SoC simply by assembling the building blocks of Fusion peripherals and applets—without writing any HDL of their own and without designing a custom ASIC. To realize that ambition, however, Actel must provide sophisticated development tools and succeed in fostering a third-party development community around Fusion, because the company probably lacks the resources to single-handedly create an extensive library of ready-made IP.

Fusion Extends Actel's Libero Tools

It's the quality of the development tools that will likely determine whether Fusion lives up to Actel's grandest promises. Like Altera and Xilinx, Actel is gradually evolving beyond its traditional role as a fabless semiconductor vendor of programmable-logic devices. FPGAs are still the core business, but development tools and licensable IP are becoming bigger attractions. Inexorably, FPGA vendors are morphing into electronic-design automation (EDA) companies and IP providers. Unlike traditional EDA companies, they also happen to sell something more tangible: chips that allow customers to rapidly deploy the designs.

Actel's central development tool is the Libero integrated design environment (IDE), a proprietary tool chain originally created for programming the gates in Actel FPGAs. Libero will be significantly extended for the new Fusion FPGAs. At the HDL level, Libero's standard development flow will allow designers to create Fusion applets, peripherals, and other functional components in Verilog or VHDL. Designers can also use System C and similar languages with Actel's tools. At a higher level of hardware abstraction, designers can use Libero to build an application-specific SoC by assembling previously created Fusion components or by importing them from an earlier design. Actel says component integration won't require writing HDL. Fill-in-the-blank screen forms will allow designers to configure each component's parameters.

New features for hardware/software partitioning will make it easier to divide application functions among the FPGA's programmable logic, a soft processor core embedded in the fabric, and the system's host CPU. Libero supports a framework that allows customers and third parties to use their own utilities with the IDE.

These days, verification often takes longer than the initial development phase, so the Fusion extensions for Libero will have new debug-and-verify features. Actel says Libero and third-party simulation tools will be able to model all the resources on Fusion chips, including the analog functions. Designers can embed logic analyzers in the programmable-logic fabric and the Fusion backbone to monitor the behavior of application components and peripherals. For software debugging, a third-party co-simulation tool will allow programmers to run an instruction-set simulator of the optional embedded-processor core.

Unfortunately, the Fusion extensions for Libero and third-party tools cannot be fairly evaluated at this point, because they are months away from release. Actel was unable to provide example screen shots for this article because the user interfaces are still evolving. When the first Fusion FPGAs and tools ship next year, early adopters should take care to thoroughly evaluate Libero and the third-party tools. These tools will be critical to developing successful projects, and there will be few alternatives.

Actel Strives to Be Different

The unique ability to integrate mixed-signal analog and digital components with SRAM and flash memory in a single programmable-logic device will set Actel apart from competitors like Altera and Xilinx. And so far, Actel is the only FPGA vendor that ARM has blessed with a license-free processor core optimized for programmable logic. If Actel can deliver everything it promises in the coming year, the company will be in a stronger position against its larger competitors.

Actel's Fusion is reminiscent of the reconfigurable microcontrollers formerly sold by Triscend. Both companies have promoted their devices as flexible, fast-to-market alternatives to conventional ASICs. Both companies' chips were able to integrate an ARM7TDMI processor core or an 8051-compatible core. Both kinds of chips allowed designers to add application-specific function blocks and peripherals to a programmable-logic fabric. And both companies have

Price & Availability

Actel says the first Fusion FPGAs and enhanced Libero development tools will ship in 1Q06. The company hasn't announced prices but says Fusion devices will duplicate the range of Actel's existing FPGA product line, with some chips priced low enough for multimillion-unit applications. For more information, visit *www.actel.com/products/fusion*.

trumpeted their graphical hardware-development tools, which allow designers to select ready-made peripherals and function blocks from a library of soft IP. (See *MPR 9/15/03-02*, "Triscend Revs Up for Motors.")

The similarities end there. Triscend's chips had no on-chip flash memory—a vital feature of Fusion. In addition, Fusion chips are fundamentally programmable-logic devices, whereas Triscend's chips were relatively expensive microcontrollers with some integrated peripherals and relatively small amounts of programmable logic. The ARM7 or 8051-compatible processor core and most peripherals were permanently etched into Triscend's chips, not synthesized in programmable gates. Another big difference, especially for Actel, is survival—Triscend was swallowed last year by Xilinx, which promptly folded the company and discontinued its product line. (See *MPR 3/15/04-02*, "Xilinx Reconfigures Triscend.")

Nevertheless, Actel has a chance to do something important that Triscend attempted but failed to do—consolidate the huge microcontroller market around a smaller number of reconfigurable chips that can absorb all or most embedded-system functions. Today, customers are overwhelmed by thick catalogs of microcontrollers that differ from each other by only a minor feature or two. And microcontroller vendors are overwhelmed by the number of similar chips they must offer to satisfy every possible customer and application. A few reconfigurable devices could replace many of those microcontrollers, at least in lower-volume applications at first.

MPR believes ARM perceived this opportunity, too, when it tried to acquire Triscend last year, before being outbid by Xilinx. ARM's recent cooperation with Actel on the Fusion project and the FPGA-optimized ARM7 core may signal that Actel is ARM's new proxy for executing its microcontroller strategy. But if Actel is serious about offering Fusion as an alternative to standard-part microcontrollers, not just as an alternative to custom ASICs, the pricing will have to be aggressive. So far, Actel is mum about prices of Fusion chips.

If Fusion prices range much above $5, Actel will compete against low-cost FPGAs from Altera (Cyclone II) and Xilinx (Spartan3) that can be augmented with soft processor cores and external flash chips. For around $5 or less, customers can also find a variety of ARM7-based microcontrollers, including some with on-chip or packaged flash memory. (See *MPR 4/4/05-02*, "ARM-Based MCUs Flex Muscles," and *MPR 5/19/03-01*, "Philips Shows Flashy MCUs.")

Competitive Field Growing Crowded

In addition to competing with conventional microcontrollers, Fusion will do battle with structured ASICs and new reconfigurable alternatives that have some things in common with Fusion. One example of the latter is the Stretch S5000-family chips, which combine a Tensilica Xtensa 32-bit processor core with programmable logic and SRAM. Designers can optimize these off-the-shelf chips for target applications by adding custom instruction extensions in the programmable fabric. Normally, Tensilica's customers must spin custom silicon to extend the Xtensa core.

However, Stretch's chips, like Triscend's, are embedded processors with some programmable logic, not FPGAs. Stretch's programmable fabric exists mainly to help programmers accelerate software; it's not for logic designers adding peripherals at the gate level. Although the hardened Xtensa processor core in an S5000 chip will almost certainly outperform the optional soft processor in a Fusion chip, a similarly priced Fusion FPGA will have nonvolatile flash memory and probably more programmable logic than an S5000. (See *MPR 4/26/04-01*, "Stretching Performance.")

Another reconfigurable alternative is the STMicroelectronics STW21000 (code-named Greenfield), the company's first commercial chip combining a 32-bit microcontroller with programmable logic. The STW21000 has a powerful ARM926EJ-S processor core, an array of integrated peripherals (two Ethernet controllers, two UARTs, six 10-bit ADCs, three 10-bit DACs, a real-time clock, and more), 150,000 gates of programmable logic, and 16Mb of embedded DRAM. These devices should outperform Fusion chips, and their peripheral integration is particularly impressive.

The STW21000 is fundamentally an integrated embedded processor enhanced with some programmable logic, however, not an FPGA enhanced with flash memory and mixed-signal capabilities. The STW21000 is probably better for its specific target applications (primarily base stations) than a Fusion chip is, but it's less adaptable for other applications. (See *MPR 4/4/05-01*, "ST's Reconfigurable Greenfield.")

The biggest news for embedded-system developers is that more alternatives to ASICs and conventional microcontrollers keep emerging, and most of the alternatives have some kind of reconfigurable logic. Whether the logic is configurable only at design time or also at run time, these chips offer new versatility and the opportunity to save millions of dollars by avoiding an ASIC project.