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China's Emerging Microprocessors

'MIPS-Like' Godson Chips Echo the Past, Foreshadow the Future

By Tom R. Halfhill {7/25/05-01}

Beyond the land of the rising sun is the rising Godson, a growing family of microprocessors designed and manufactured in China by Chinese engineers for the Chinese domestic market. Intended for low-cost desktop computers, servers, and embedded systems, these 32- and 64-bit chips are rapidly becoming as sophisticated as any designs in the world, falling short in performance only because Chinese fabrication technology lags behind the rest of the industry by two process generations.

Microprocessor Report briefly described the 32-bit Godson-1 in 2002, but few technical details have trickled out of China until now. (See *MPR 12/2/02-03*, "China Unveils MIPS-Like CPU.") All Godson processors are designed by engineers at the Institute of Computing Technology (ICT), part of the Chinese Academy of Sciences in Beijing. In 2002, ICT and Chinese entrepreneurs founded a Beijing-based fabless semiconductor company, BLX IC Design Corporation Ltd., to bring Godson processors to market and support them with software-development tools and product-reference designs.

In December 2003, Advanced Micro Devices and BLX IC Design announced a relationship and opened the AMD/BLX Computing Client Development Center in Beijing. BLX IC Design is creating reference designs for thin clients and other computing products using AMD and BLX IC Design processors. The first two products are thin clients powered by AMD's MIPS32-compatible Alchemy Au1500 processor and BLX IC Design's Godson-1. The creators of the Godson-1 say its architecture is "MIPS-like"—a description that annoys MIPS Technologies, which doesn't authorize the Godson architecture or license any intellectual property to ICT or BLX IC Design. AMD, which is a MIPS licensee, says it encourages BLX IC Design and MIPS to resolve their licensing issues.

This spring, ICT introduced the Godson-2, another "MIPS-like" processor. Considerably more advanced than the Godson-1, it has a 64-bit architecture, four-way superscalar pipelines, dynamic branch prediction, out-of-order execution, and other powerful features. China's Semiconductor Manufacturing International Corporation (SMIC) fabricates Godson-2 chips in a 0.18-micron CMOS process, and ICT is porting the design to a 0.13-micron process. ICT is also beginning work on the next-generation Godson-3, which may sprout multiple processor cores and hardware-assisted simultaneous multithreading.

It's clear that China wants to produce general-purpose microprocessors as advanced as any in the world. The Godson family (also known as Dragon) is only one fruit of China's National 863 Program, a government-funded research and development project to create homegrown technology for Chinese high-tech industries. (The 863 Program derives its name from the month and year of its inception: March 1986.) For now, Godson processors are solely for China's domestic market, but exports to world markets are possible in the future.

In June, *MPR* interviewed Godson's chief architect, Weiwu Hu, a professor at ICT in Beijing. Weiwu described the Godson-1 and Godson-2 in unprecedented detail and revealed some of his ambitions for the Godson-3. In addition, Weiwu provided an English-language white paper on the Godson-2 microarchitecture recently published in the *Journal of Computer Science & Technology*.

After analyzing this information, *MPR* believes the Chinese already are capable of designing world-class microprocessors, assuming they have access to world-class fabrication technology. Although Chinese fabs are about two process generations behind the curve, China's technology is rapidly accelerating. China could also outsource some chip manufacturing to foreign foundries—perhaps even to crosstown rivals on the opposite side of the Taiwan Strait. (Irony knows no borders.)

Following is our analysis of the Godson processors, including comparisons with similar MIPS architectures and microarchitectures. For excerpts from our interview with Weiwu, see the sidebar, "A Conversation With Godson's Father."

"MIPS-Like": Almost MIPS Compatible

ICT appears to have settled on the MIPS architecture as the template for its Godson architecture, despite the reported popularity of ARM in China and some early news reports that Godson chips would be x86 compatible. (See the sidebar, "China Likes the x86, Too.") *EDN China* recently surveyed its subscribers and found that ARM accounts for 63% of Chinese embedded-system development, followed by the x86 at 21%, PowerPC at 9%, MIPS at 6%, and Hitachi's SuperH at 1%.

Nevertheless, the MIPS architecture was a logical starting point for ICT. It's an efficient, well-understood RISC architecture used as a teaching tool in universities all over the globe. It's suited for a wide variety of applications, from servers and workstations to embedded systems. It's popular in networking and communications equipment, and it's richly supported by software-development tools and operating systems. The MIPS architecture has 32- and 64-bit implementations, and some embedded MIPS processors have a subset of 16-bit instructions for greater code density, making them suitable for even very low power applications, such as smartcards.

Although imitation may be the sincerest form of flattery, MIPS Technologies isn't smiling. MIPS has no connection with ICT, BLX IC Design, or the Godson architecture. MIPS objects to the term "MIPS-like," calling it an improper derivation of the MIPS trademark and an inaccurate description that could mislead customers. The company's position is that only MIPS licensees can fully access the rich ecosystem of MIPS-compatible software and development tools. MIPS says it takes the protection of its intellectual property (IP) "extremely seriously" and rigorously protects its patents, trademarks, and trade secrets. Of course, IP issues are a touchy subject in almost any business discussion about China.

MIPS is definitely interested in the Chinese market. Last March, the company opened a sales office and research-and-development lab in Shanghai to sign up new licensees and qualify MIPS processor cores at Chinese foundries. One of those foundries is SMIC, where BLX IC Design manufactures the Godson chips. MIPS has licensed the MIPS32 4Kc hard core to Huaya Microelectronics of Shanghai and recently announced another licensing deal with Actions Semiconductor of Beijing for the 4KEc Pro and M4K Pro. MIPS prefers to license hard cores in China because they require less development effort than synthesizable cores and provide more protection for the company's treasured IP.

Since MIPS was founded in 1984, it has accumulated numerous patents on its architecture and related technology. In particular, MIPS has patented some load and store instructions that access data not aligned on word boundaries in memory, as well as technology for reducing the loss of precision while performing arithmetic operations in single-instruction, multiple-data (SIMD) format. In 1999, those patents and a MIPS lawsuit tripped Lexra, a rival IP vendor based in Massachusetts. After years of legal wrangling, Lexra stopped licensing its own "MIPS-like" processor cores and became a bona fide MIPS licensee in 2001, but it folded soon afterward. (See *MPR 12/6/99-03*, "MIPS vs. Lexra: Definitely Not Aligned.")

Most MIPS patents are registered in the United States, Europe, and Japan, with a limited but growing number in China. It's unclear whether Godson processors could use the patented instructions if China restricts the chips to its own domestic market. However, Weiwu Hu says the Godson architecture doesn't support the patented load/store instructions and implements an original subset of SIMD instructions for media processing.

Without the patented instructions, Godson processors are not truly MIPS compatible, but they are close. Very close. In fact, ICT has created a utility that can patch MIPS-compatible executable files to run on Godson processors without recompiling the source code. Although Weiwu says the utility can't successfully patch every executable, it's useful for quickly converting software for which source code is not available. Weiwu says the utility has successfully patched some parts of embedded operating systems, and that the MIPS versions of Red Hat Linux, VxWorks, Windows CE, and the Mozilla web browser will run on Godson processors with minor modifications.

Rapid Architectural Evolution

ICT is making great leaps forward with each Godson generation. The Godson-1, introduced in 2002, is a fairly simple 32-bit processor patterned after the MIPS III instruction-set architecture (ISA). In many respects, it's a cross between the MIPS R3000 (introduced in 1988) and the R4000 (1991).

All three of those processors have uniscalar pipelines: seven stages in the Godson-1, five stages in the R3000, and eight stages in the R4000. However, the R3000 implements the earlier MIPS I ISA and lacks an integrated FPU, branch prediction, and out-of-order execution. The Godson-1 has those features and implements almost all of the MIPS III ISA, but it's a 32-bit processor, unlike the R4000, which was the first 64-bit processor from MIPS.

The Godson-1's L1 caches are small: only 8KB each for instructions and data, whereas even the MIPS R3000 had

32KB caches. Neither the Godson-1 nor the R3000 has any provision for an L2 cache. Fabricated in an SMIC 0.18-micron CMOS process with six layers of metal, the Godson-1 reaches 266MHz and typically consumes less than 500mW. Another restraint on its performance, besides the trailing-edge fabrication process, is that ICT used an ASIC design flow with macro-cell libraries and automated place-and-route tools. There is virtually no custom circuit design in the Godson-1.

Perhaps the biggest contrast between the R3000 and Godson-1 is that they're intended for completely different classes of applications. In 1988, the R3000 was a state-of-the-art RISC processor for powerful workstations and servers, whereas the Godson-1 is designed primarily for low-cost embedded systems, such as industrial controllers. Nevertheless, the Godson-1 achieved an important milestone: it was China's first high-performance general-purpose microprocessor.

The Godson-2 is a much more sophisticated chip, one of the most advanced designs ever patterned after the MIPS architecture. Longtime *MPR* readers may recall the 1990s race between so-called speed-demon and brainiac processors. Speed demons, exemplified by the DEC Alpha, pursued high throughput by optimizing the fabrication process to wring out the highest possible clock frequency. Brainiacs, typified by IBM's Power processors, sought high throughput by using complex microarchitectures to achieve wide instruction-level and data-level parallelism. The two philosophies have never been mutually exclusive, but they represent opposite poles as starting points for a microprocessor design. With the Godson-2, ICT gravitated toward the brainiac pole, most likely because China's fabrication technology rules out the speed-demon approach, at least for now.

Five Function Units for High Throughput

Aiming for larger applications as well as higher performance, the Godson-2 is a 64-bit processor, with 64-bit-wide integer datapaths and 64-bit general-purpose registers. (The FPU was already 64 bits wide in the Godson-1.) The Godson-2 is patterned after the MIPS IV ISA instead of MIPS III, and its closest cousin is the MIPS R10000, which was the first single-chip superscalar processor from MIPS when introduced in 1995. Both the R10000 and Godson-2 can issue four instructions per clock cycle from five pipelined function units, and both have extensive internal resources for dynamic branch prediction and out-of-order execution. (See *MPR 10/24/94-03*, "MIPS R10000 Uses Decoupled Architecture.") They also have memory-management units (MMU) with translation lookaside buffers (TLB), and the Godson-2 supplements the TLB with a 16-entry instruction TLB (iTLB).

As the block diagram in Figure 1 shows, the Godson-2 has two ALUs, an address-generation unit (AGU), and two FPUs. ALU 1 can execute adds, subtracts, shifts, compares,

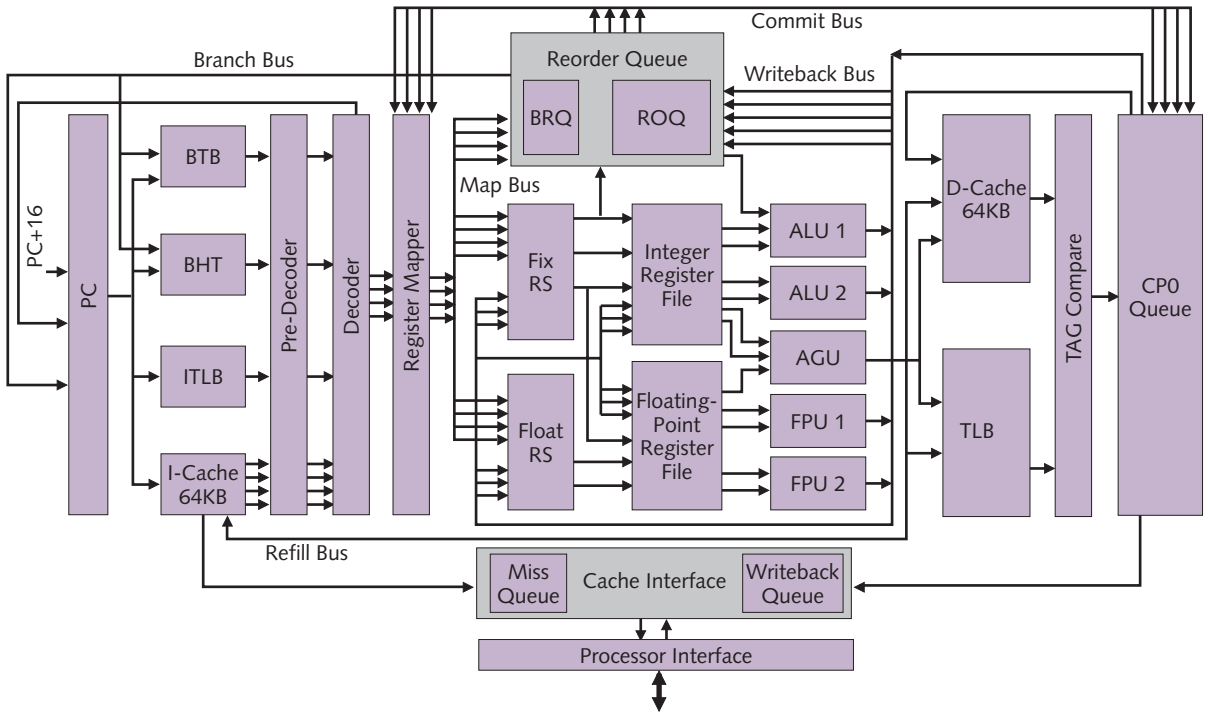

Figure 1. Godson-2 block diagram. China's most powerful microprocessor is patterned after the MIPS IV ISA and is similar to the MIPS Technologies R10000 processor introduced in 1995. Both are four-way superscalar 64-bit designs with five function units, out-of-order execution, dynamic branch prediction, integrated MMUs, and strong floating-point capabilities. The Godson-2 has deeper pipelines, larger L1 caches, and greater resources for branch prediction.

Instruction Type	Function Unit	Latency
Integer Instructions		
Add	ALU 1 & ALU 2	1 cycle
Subtract	ALU 1 & ALU 2	1 cycle
Multiply	ALU 2	4 cycles
Divide	ALU 2	4–37 cycles
Logical	ALU 1 & ALU 2	1 cycle
Shift	ALU 1 & ALU 2	1 cycle
Compare	ALU 1 & ALU 2	1 cycle
Trap	ALU 1	1 cycle
Branch	ALU 1 & ALU 2	1 cycle
Floating-Point Instructions		
Add	FPU 1	4 cycles
Subtract	FPU 1	4 cycles
Multiply	FPU 2	5 cycles
Divide	FPU 2	
Single-Precision		4–10 cycles
Double-Precision		4–17 cycles
Square Root	FPU 2	
Single-Precision		4–16 cycles
Double-Precision		4–31 cycles
Absolute	FPU 1	2 cycles
Negate	FPU 1	2 cycles
Convert	FPU 1	4 cycles
Compare	FPU 1	2 cycles
Branch	FPU 1	2 cycles
Memory-Access Instructions		
Load	AGU	variable
Store	AGU	variable

Table 1. The Godson-2's instruction latencies are similar to those of other high-performance RISC processors. The most common types of integer instructions can execute on either of the two ALUs. Notice that even double-precision floating-point divide instructions execute at least as fast as integer divides, and floating-point multiplies are only a little slower than integer multiplies.

traps, branches, and logical operations in a single clock cycle. ALU 2 can execute adds, subtracts, shifts, compares, and logical operations in a single clock cycle, but integer multiplies and divides have longer latencies. Multiplies require four cycles, and the integer divider—which uses the Sweeney-Robertson-Tocher (SRT) algorithm and isn't fully pipelined—requires 4 cycles to 37 cycles, depending on the complexity of the operation.

FPU 1 can execute floating-point adds, subtracts, absolute-value operations, negations, conversions, comparisons, and branches in 2 to 4 cycles. FPU 2 can execute floating-point multiplies, divides, and square-root instructions in 4 to 31 cycles, depending on the operation and whether the operands are 32-bit single precision or 64-bit double precision. The pipelined floating-point multiplier uses a 2-bit Booth-encoded Wallace-tree algorithm, whereas the divider and square-root units use the SRT algorithm and aren't fully pipelined. Table 1 shows the Godson-2's latencies for various types of integer and floating-point instructions.

Both FPUs can execute some special paired-single and SIMD instructions, which are typical of the MIPS architecture and are especially useful for data-intensive media processing. Paired-single instructions execute two 32-bit floating-point operations (adds, subtracts, or multiplies) in the 64-bit datapath of an FPU. The SIMD instructions can execute 8-, 16-, 32-, or 64-bit integer instructions (adds, subtracts, multiplies, divides, shifts, compares, branches, and logical operations) in the 64-bit floating-point datapath. Programmers must explicitly code the integer SIMD instructions—the processor can't route ordinary integer operations through the FPUs—but these instructions provide additional processing power and flexibility. The Godson-2 also supports a multiply-add (MADD) instruction similar to the MADD instruction in the MIPS architecture and multiply-accumulate (MAC) instructions in other architectures.

To keep up with the function units, the integer register file has six read ports and three write ports, and the floating-point register file has five read ports and three write ports. This generous porting allows each function unit to read two 64-bit input operands and write one 64-bit result per clock cycle while leaving one read port and one write port available for floating-point load and store operations.

Overall, the Godson-2's function units and other execution resources are quite similar to those in the MIPS R10000. Both processors can fetch, decode, dispatch, and retire four instructions per clock cycle, and both have five function units, creating a bulge of extra capacity in the execution stages of their pipelines. This extra capacity should increase the instructions-per-cycle average and help achieve the maximum throughput of four instructions per cycle more often.

Lavish Resources for Branch Prediction

In 1995, the MIPS R10000 reached 200MHz when fabricated in a 0.5-micron CMOS process. China's 0.18-micron fabrication technology is a few generations more advanced than that, but it is still behind the rest of the industry, so ICT lengthened the Godson-2's pipelines to reach higher clock frequencies. As Figure 2 shows, the basic integer pipeline is nine stages deep, compared with seven stages in the Godson-1 and five to seven stages in the R10000. As a result, the Godson-2 hits

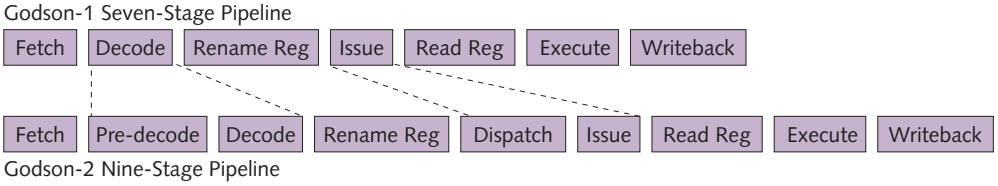

Figure 2. ICT lengthened the Godson-2 pipeline by two stages, compared with the Godson-1. The deeper pipeline enables higher clock frequencies in the same fabrication process, but greater penalties for mispredicted branches required ICT to improve the accuracy of branch prediction. The Godson-2's dynamic branch prediction is sophisticated and exceeds the capabilities of the MIPS R10000.

400–500MHz, and the upcoming 0.13-micron version is aiming at 800MHz to 1.0GHz.

Deeper pipelines impose greater penalties for mispredicted branches, so ICT has endowed the Godson-2 with dynamic branch prediction instead of the static prediction in the Godson-1, which simply predicts that all branch-likely and jump instructions will be taken. The Godson-2 uses the same static prediction for those instructions at the predecode stage (stage 2) but dynamically predicts conditional branches and jump-register instructions.

Branch-prediction resources consist of a 4,096-entry branch history table (BHT) with a nine-bit global history register and a 16-entry branch target buffer (BTB). The predictor algorithm uses the familiar 2-bit saturating counter for keeping track of four branch states: strongly not taken (0), weakly not taken (1), weakly taken (2), and strongly taken (3). The processor increments the counter each time a branch is taken or decrements the counter if the branch is not taken. The BHT can store 4,096 of those counters. To predict where the branch will land, the BTB stores up to 16 program-counter addresses and target addresses for jump-register instructions, plus another 2-bit counter for each entry. As a program runs, buffer entries whose counters equal 0 or 1 are replaced before entries whose counters equal 2 or 3.

A four-entry stack stores the return addresses for branches. For each branch instruction, the Godson-2 saves a copy of the top-of-stack pointer so the processor can restore the stack to its previous state when a branch is mispredicted. ICT hasn't quoted the accuracy of the Godson-2's branch predictor, but other processors with similar prediction algorithms and resources are usually 90–95% accurate—a huge improvement over static prediction, which is about 60% accurate.

However, one potential bottleneck in the Godson-2's branch-prediction mechanism is that it can decode only one branch instruction per clock cycle, even though it can fetch and decode four other types of instructions per cycle. Typical general-purpose program code averages one branch every four to six instructions, so the likelihood of two branch instructions entering the decode stage of the pipeline (stage 3) at the same time is relatively high. In that case, the Godson-2 pipeline stalls until it decodes the first branch instruction.

Dynamic Scheduling Improves Efficiency

Although the earlier Godson-1 can execute instructions out of program order, its resources for dynamic scheduling are somewhat limited. It supplements the architectural register file with only eight rename registers, all of them shadows of 32-bit general-purpose registers. It has no rename registers for 64-bit floating-point registers, so only integer instructions can execute out of order. Even so, to find dynamic scheduling in a uniscalar processor like the Godson-1 is unusual, though not unprecedented—most processors went superscalar before they tackled the complexities of out-of-order execution.

Dynamic scheduling is vastly improved in the Godson-2. To begin with, both the integer and floating-point register files are fully duplicated with rename registers, so there is a total of 64 integer registers and 64 floating-point registers. (And because the Godson-2 implements the 64-bit MIPS IV architecture, all those registers are 64 bits wide.) Indeed, the Godson-2 makes no distinction between architectural registers and rename registers—all are part of the same physical register file. Mapping tables indicate which physical registers are active logical registers, depending on whether the processor has committed the results of a particular instruction. Multiple physical registers can map to a single logical register at the same time, with each physical register holding different pending operands or results.

The Godson-2 uses the popular method of reservation stations to dispatch instructions out of order to the five function units. It has separate 16-entry stations for integer and floating-point instructions, allowing the processor to juggle as many as 32 instructions while determining the most efficient order in which to dispatch them. Each station can accept four instructions per clock cycle, and together they can dispatch five instructions per cycle. In a departure from the R10000, the Godson-2 routes load/store instructions through the integer reservation station instead of providing a separate station for that purpose.

At the back end of the pipeline, the Godson-2 has a 32-entry reorder buffer that holds the results of executed instructions until the processor can retire them in their original program order. This buffer can accept up to four results per clock cycle. Result forwarding and snooping allow subsequent instructions to immediately use results from recently executed instructions. All the resources for register renaming and dynamic scheduling include mechanisms for recovering from mispredicted branches and exceptions, so the Godson-2 maintains a precise exception model during out-of-order execution.

The Godson-2 can dispatch load/store instructions to the AGU out of order, and a multiported memory-access queue can juggle up to 16 of them at a time. Load instructions entering the queue always snoop for pending stores, seeking to bypass the store by reusing the data. Likewise, when a store instruction enters the queue, it checks for any subsequent loads to which it can forward data. The queue also snoops cache refills and replacements.

In another big improvement over the Godson-1, the Godson-2 has much larger L1 caches: 64KB each for instructions and data compared with 8KB caches in the Godson-1. Both primary caches are four-way set-associative and nonblocking. An external L2 cache is optional and can range in size from 256KB to 8MB. In contrast, the Godson-1 has blocking L1 caches and no provision for L2 cache at all. However, to reduce the chip's pin count, the Godson-2 lacks a dedicated back-side bus for the external L2 cache, as found on the MIPS R10000. Instead, the Godson-2 must access the optional L2 cache over the main system bus.

China Likes the x86, Too

Even while the Chinese develop their own Godson microprocessors patterned after the MIPS architecture, they are also seeking ways to make x86-compatible processors for China's domestic market and possibly for export.

Last May, Transmeta announced its intention to sell its Crusoe processors and license its Efficeon processors to Culturecom Technology Limited, a company based in Hong Kong. Culturecom will pay $15 million to buy the Crusoe product line outright and license technology for making 0.13-micron Efficeon processors in China. In addition to the upfront payment, Culturecom will pay chip royalties to Transmeta. If the deal receives the necessary technology export licenses from the U.S. government and clears other hurdles, it would infuse Transmeta with much-needed cash while providing Culturecom with a legal way to manufacture and sell x86-compatible processors. (See *MPR 5/2/05-01*, "The Transformation of Transmeta.")

Other Chinese companies are exploring different routes to the x86, although few details are available. In 2002, a Chinese company called Shanghai Fudan Microelectronics announced the Shenwei I, a 32-bit x86-compatible embedded processor. So far, China's efforts to imitate the x86 haven't provoked a legal response from Intel, but any attempt to export the chips to world markets would almost certainly attract Intel's attention.

No-Execute Bit Foils Malicious Hackers

Memory addressing in the Godson-2 is fairly conventional for a high-performance processor, with one notable exception: it implements page-level execution protection. This valuable feature is like the NX (No eXecute) bit recently added to some x86-compatible PC and server processors and isn't available in any MIPS processors. (See *MPR 8/9/04-01*, "NX Helps Windows Security.")

Each page entry in the Godson-2's 64-slot fully associative TLB has a special security bit. If a program tries to fetch an instruction from a page whose security bit is set, the processor triggers an address-error exception. An operating system can handle the exception by refusing to fetch the instruction or by alerting the user. The most common purpose of this security bit is to prevent buffer-overflow exploits by hackers, who often trick a program into fetching instructions from a malicious routine planted somewhere in memory. By setting the security bit for all pages outside a program's legitimate instruction memory, the operating system can ward off those exploits.

Otherwise, the Godson-2's memory addressing is straightforward. The 64-entry TLB stores the physical page numbers and security bits in SRAM and the virtual page addresses in content-addressable memory (CAM). The processor searches the fully associative CAM during the address-calculation stage. Several MIPS-type coprocessor-0 (CP0) control registers related to memory addressing are physically located near the TLB to minimize wire delays. Although the Godson-1's TLB is smaller than the TLBs in the R4000 and R10000, those MIPS processors were designed for higher-end workstation and server applications, so they had greater memory requirements.

In the same vein, the Godson-2 has only a 36-bit memory-address bus and allocates only 40 bits for virtual memory addressing, even though it's a 64-bit processor. Again, this is an economy decision—it reduces the chip's pin count without sacrificing anything significant for embedded applications. The 64-bit MIPS R10000 got by with 36-bit physical addressing and 44-bit virtual addressing, and even the latest 64-bit x86 processors from AMD and Intel make similar compromises. With 36/40-bit addressing, the Godson-2 can support 64GB of physical memory and 1TB (terabyte) of virtual memory—more than enough for its intended applications.

In almost every respect, the Godson-2's capabilities match or exceed those of the R10000, the most advanced microarchitecture ever designed by MIPS. (Later high-performance processors from MIPS, like the R12000 and R14000, were relatively minor enhancements of the R10000; see *MPR 10/6/97-01*, "MIPS R12000 to Hit 300MHz," and *MPR 8/7/00-01*, "SGI Updates Systems, CPU Plans.") Of course, ICT has the benefit of 10 years of hindsight, whereas MIPS was breaking new ground when designing the R10000 in the early 1990s. Nevertheless, the Godson-2's numerous improvements over the Godson-1 show how quickly the Chinese are applying advanced design techniques. Table 2 compares features of the Godson-1 with those of the Godson-2 and three important MIPS processors: the R3000, R4000, and R10000.

Although ICT used standard cells and automated place-and-route tools for most of the Godson-2 design, some critical blocks employ custom circuit design, another improvement over the Godson-1. Hand-crafted cells and macros include some 4-bit flip-flops, several types of low-latency gates (NANDs, NORs, and AOIs), multiplexers, buffers, inverters, 4/6/8-bit comparators, an adder, the multiported integer register file, and wire-bonding pads for the flip-chip package. Weiwu says the design is fully static; there is no dynamic or domino logic.

Thanks to the extra engineering effort invested in custom design and the deeper nine-stage pipeline, the Godson-2 can reach significantly higher clock frequencies than the Godson-1 in the same 0.18-micron process: 400–500MHz, versus 266MHz for the earlier chip. The Godson-2 die measures 6.7mm × 6.2mm (about 41.5mm^2), and power consumption is typically 3–4W. BLX IC Design recently introduced the production version of this chip for the Chinese domestic market. SMIC fabricates the chips on 8-inch wafers at a fab in Shanghai. SMIC also has an 8-inch wafer fab in Tianjin and is building a 12-inch wafer fab in Beijing.

While mass production of the 0.18-micron Godson-2 gets under way, ICT is porting the design to an SMIC 0.13-micron process, aiming for clock speeds in the 800MHz–1.0GHz range and power consumption below 8W. ICT hopes to have that chip ready for production in 4Q05 or 1Q06. Additional improvements contemplated for future versions of the Godson-2 include more custom-circuit design, support for conditional-move and floating-point MADD instructions, better branch prediction, hardware-assisted simultaneous multithreading, on-chip L2 cache, coherent caching for symmetric multiprocessing, an on-chip DDR memory controller, and perhaps a coprocessor for accelerating Java programs.

Beyond the Horizon: Godson-3

When ICT finishes a microprocessor, it makes only a few hundred samples before handing off the project to BLX IC Design, the Chinese company charged with producing and supporting the chips for the Chinese market. Then ICT turns its attention to the next design project. Even while ICT is porting the Godson-2 to a 0.13-micron process, engineers at the institute have started some exploratory work on the next-generation Godson-3.

Weiwu says the Godson-3 will strive for floating-point performance greater than 100 GFLOPS, perhaps by using simultaneous multithreading and multiple processor cores on a single chip. He wants to design a chip with at least four processor cores. However, a multicore chip of that scope would probably require much more custom-circuit design, especially if it targets a trailing-edge fabrication process. Without more custom design, four or more cores with the capabilities of the Godson-2 would occupy a relatively large slab of silicon, making the chip too expensive for the Chinese market.

Software is another problem. Like everyone else in the world, Weiwu worries about keeping all the processors on a multicore chip busy enough to justify the additional cost and power consumption of the design. He says ICT is intensively exploring ways to more efficiently distribute an application load across multiple cores, even when the software isn't multithreaded.

Feature	BLX IC Design Godson-1	BLX IC Design Godson-2	MIPS R3000	MIPS R4000	MIPS R10000
Architecture	Similar to MIPS III	Similar to MIPS IV	MIPS I	MIPS III	MIPS IV
Arch. Width	32 bits	64 bits	32 bits	64 bits	64 bits
Core Freq	266MHz (0.18µm)	400–500MHz (0.18µm) 800MHz–1.0GHz (0.13µm)*	20MHz	50MHz	200MHz
Pipeline Width	Uniscalar	4-way	Uniscalar	Uniscalar	4-way
Pipeline Depth	7 stages	9 stages	5 stages	8 stages	5–7 stages
L1 Cache (I/D)	8K/8K	64K/64K	32K/32K	8K/8K	32K/32K
L2 Cache (Internal)	—	—	—	—	—
L2 Cache (External)	—	256KB–8MB	—	Up to 4MB	Up to 16MB
L2 Back-side Bus	—	—	—	128 bits 800MB/s	128 bits 3.2GB/s
Branch Prediction	Static	Dynamic	—	—	Dynamic
Branch History Table	—	4,096 entries	—	—	512 entries
Out-of-Order Exe	Yes	Yes	—	—	Yes
Integer Registers	32 x 32 bits	32 x 64 bits	32 x 32 bits	32 x 64 bits	32 x 64 bits
Int Rename Registers	8 x 32 bits	32 x 64 bits	—	—	32 x 64 bits
Integrated FPU	Yes	Yes	—	Yes	Yes
FP Registers	32 x 64 bits	32 x 64 bits	—	32 x 64 bits	32 x 64 bits
FP Rename Registers	—	32 x 64 bits	—	—	32 x 64 bits
Integrated MMU	Yes	Yes	Yes	Yes	Yes
TLB Size	48 entries	64 entries	64 entries	96 entries	128 entries
Memory Addressing	32-bit physical 32-bit virtual	36-bit physical 40-bit virtual	32-bit physical 32-bit virtual	36-bit physical 40-bit virtual	36-bit physical 44-bit virtual
Transistors	2.6 million	13.5 million	110,000	1.1 million	5.9 million
IC Process (Intro)	0.18µm 6LM	0.18µm 6LM	1.2µm	1.0µm	0.5µm
Power	<0.5W (0.18µm)	3W–4W (0.18µm) 6W–8W (0.13µm)*	4W	n/a	30W
Introduction	2002	Now (0.18µm) 4Q05–1Q06 (0.13µm)*	1988	1991	1995

Table 2. The Godson-2 is a big improvement over the Godson-1 in several ways, and it compares favorably with historic MIPS processors. However, ICT's greater use of standard-cell logic and automated place-and-route tools has inflated the number of transistors in its designs. The Godson-2 has more than twice as many transistors as the MIPS R10000, even though both processors have similar microarchitectures. Nevertheless, the Godson processors consume less power, thanks to their more advanced fabrication processes. Note that the MIPS R3000 was the first commercially successful processor from MIPS Technologies; the R4000 was the first 64-bit MIPS processor; and the R10000 was the first single-chip superscalar processor from MIPS. (n/a: data not available. *ICT estimate.)

A Conversation With Godson's Father

Microprocessor Report recently interviewed Weiwu Hu, chief architect of the Godson-1 and Godson-2 microprocessors. Weiwu is a professor at the Institute of Computing Technology (ICT), Chinese Academy of Sciences. He received his B.S. in computer science from the University of Science and Technology of China in 1991 and his Ph.D. in computer science from ICT in 1996. His research interests include high-performance computer architecture, parallel processing, and VLSI design. Here are some excerpts from our interview.

MPR: What is the purpose of your project?

Weiwu: The purpose of the project is to design what is called high-performance microprocessors. It's low performance compared with Intel's or IBM's, but it's high performance compared to ourselves.

MPR: What is the intended purpose of Godson-2? What will it be used for?

Weiwu: Several kind of uses. First is low-cost desktop PC, very low-cost PC. In China there is a very big population, almost two billion people. Current PCs are not expensive, but they are still expensive for China's situation, because most Chinese people are still very poor. So we need to geometrically reduce the cost. We do not need very high performance as delivered by Intel and IBM and so on. You know Moore's law? Every 18 months, performance will be doubled. But Moore's law also tells us that with enough performance, cost is reduced every 18 months.

Also, our current Godson will be used in some embedded situations. The instruction set of Godson-2, we call it MIPS-like but not MIPS compatible. MIPS processors are often used in many embedded situations, such as networks, routers, game machines, industrial control, and so on. So high-end embedded applications and low-end desktop applications are the main goal of Godson-2. We are also aiming to make very cheap clusters with Godson-2, maybe a top-level cluster, not a network-level cluster.

This is a research project for me. The project is defined by my leader, by the government, by the National 863 Program. I'm just undertaking the project.

MPR: Are these processors only for China or will they be exported?

Weiwu: It's a research project, so I don't know exactly about the production and markets. But I think it's only for, my understanding, only for the Chinese market. We have a very long way to go. My task is, I finish maybe tens or hundreds of prototype machines, I can finish my project [laughs]. As a government project, of course, we also have a marketing goal, but I think, from what I can see, and what I can say, we still have at least two or three years to go before we can put it in the market.

ICT, my institution, is like a university. It's the Institute of Computing Technology, Chinese Academy of Sciences. It's not a company, it's like a university. BLX [BLX IC Design Corporation Ltd.], which is founded by ICT, their main task is to push Godson to market, but I think they also have a long way to go. It's very easy to design an aggressive CPU like Godson-2, but it's much harder to sell it.

MPR: Is there going to be Godson-3 someday?

Weiwu: We are designing an improved version of Godson-2, and, yes, we have a plan about Godson-3. I think Godson-3 should be a multicore processor. It will include at least four CPUs in the chip, a very aggressive architecture for interconnecting the processors inside the chip, for sharing the memory. The key problem is how to make the multiple cores in the same chip cooperate to solve a single problem.

MPR: Can you run Windows CE and VxWorks without recompiling?

Weiwu: How to say? Maybe some part would need recompiling, but you know, normally it's supported. But we need to make some modification, because we are not totally compatible. We are only MIPS-like. I think 95% of code doesn't need to be modified. We have to modify [the other 5%] because of some patented instructions by MIPS.

MPR: Oh, you don't use those unaligned load/stores, you mean?

Weiwu: Yes, they have some unaligned loads/stores. I think they are patented in the United States and Canada and Japan and Korea and so on. They are not patented in China, but we are not allowed to use it. You know, these kinds of instructions are very difficult to implement. There will be many muxes in the datapath. Even though MIPS has not patented these instructions in China, we still do not like to use it. We can provide a tool to remove these kind of unaligned instructions in executable code. So there will be no problem.

MPR: I see. Then it replaces them with regular loads and stores?

Weiwu: Yes. Just replace one instruction with two or three. The difficulty is how to relink it to make the branch point to the correct position. The performance will not lose much. This I think is the only difference.

I think we are defining the most aggressive MIPS architecture. The MIPS architecture was supported by SGI for high-performance processors, but now SGI has

"A Conversation" Continued

stopped. But we are defining a very aggressive architecture for MIPS, though not fully compatible. We are designing a multicore architecture for MIPS, and in my dream, I even think our multicore processor will speed up a single-threaded program. We have a very good program of research, which means when a single thread comes into multicore, it can speed it up. We like to make MIPS very popular in China.

We have a very long way to go, but we will continue to go, because we are a government project. We don't have great pressure from the market.

Weiwu wouldn't speculate about an introduction date for the Godson-3. If the processor is to be as advanced as he contemplates, experience with similarly ambitious projects suggests it will take three or four years to design and produce.

China's Goal: Technology Independence

Godson microprocessors are merely one facet of China's National 863 Program, which aims to reduce China's dependence on foreign technology in many fields. China doesn't necessarily have to create superior technology to achieve its goals. Technology sufficient for the intended applications is good enough, especially if Chinese manufacturing reduces costs and the Chinese designs don't owe licensing fees or royalties to foreign patent holders. In recent years, China has been chafing at pressure from foreign governments, corporations, and organizations to obediently follow standards and protocols created elsewhere. China believes it has a large enough market to establish some of its own standards—and perhaps to export some standards as well.

Outsiders frequently fail to appreciate the sheer numbers China brings to the game. Mainland China has more than 1.3 billion people. Even if the vast majority of the country remains poor and gains no significant buying power in world markets, China will soon boast an affluent middle class of 200 million people, as large as the middle classes in the United States and Europe. China is also a nation that graduates more than 300,000 engineers each year, enough brainpower to pursue a vast array of projects.

With the Godson family, China appears to be standardizing on a MIPS-derived architecture that can leverage some previous design work and existing software without licensing any patented IP. Already, ICT has carried the Godson architecture nearly as far as MIPS Technologies has carried the MIPS architecture. The most important omission is a subset of 16-bit instructions like the MIPS16e extensions. Virtually all 32-bit embedded-processor architectures have 16-bit instructions these days, because the shorter instructions significantly improve code density in memory-constrained embedded systems. *MPR* won't be surprised if future Godson processors add 16-bit instructions, too.

So far, ICT seems to be emphasizing fast architectural evolution over maximum processor performance. That strategy would explain why Godson processors rely so heavily on standard cells and automated design tools instead of full-custom circuit designs and hand-packed layouts. Certainly, a nation that graduates more than 300,000 engineers a year can't be suffering from a shortage of gate-pushers. Our guess is that when ICT thinks the Godson microarchitecture has more or less reached a design plateau, the engineers will focus more effort on optimizing circuit design and chip layout for higher performance. On the other hand, ICT might be starting a trend, placing a higher priority on design turnover than on squeezing out the last few drops of unneeded performance.

Godson can succeed even if BLX IC Design doesn't export a single chip outside of China. Even if China's domestic market consumes all the production, the Chinese will probably consider Godson a success, because it reduces their imports of foreign microprocessors (and, hence, their expenditure of hard currency) and makes China more self-sufficient. If Godson chips ever reach the outside world, they will probably travel inside finished goods exported from China instead of competing as discrete products on the merchant chip market, at least at first. Although the world market for microprocessors isn't a zero-sum game by any means, every Godson chip sold in China's domestic market potentially represents the loss of a sale by foreign chip vendors. Without Godson, China would probably import equivalent processors to fill the same sockets.

Price & Availability

BLX IC Design Corporation Ltd. introduced the Godson-1 microprocessor for the Chinese domestic market in 2002. Last quarter, the Beijing-based company introduced the 0.18-micron version of the Godson-2, also for the Chinese market. The Institute for Computing Technology at the Chinese Academy of Sciences, which designs Godson processors, is now porting the Godson-2 design to a 0.13-micron process and expects production to begin in 4Q05 or 1Q06. Godson prices are unpublished.

Very little information about Godson chips is available in English. ICT's English-language white paper on the Godson-2, recently published in the *Journal of Computer Science & Technology* (Volume 20, Number 2), isn't available on the Internet. For additional information, periodically check these web pages maintained by the Chinese Academy of Sciences:

- *http://english.cas.ac.cn/Eng2003/page/SRA/C_6.htm*
- *http://english.cas.cn/Eng2003/news/detailnewsb.asp?infoNo=25459*

For all these reasons, Godson is genuine competition for other chip vendors, even if performance seems less than competitive with the latest microprocessors from the United States, Japan, and Europe. Moreover, Godson's performance is limited mainly by fabrication technology, not by its architecture or microarchitecture. The sophistication of the Godson-2 shows that the Chinese are poised to produce microprocessors as powerful as any in the world. When China's manufacturing capabilities catch up with its design skills—or if China outsources the manufacturing to state-of-the-art foundries—the Chinese will be ready to take their place at the forefront of the world semiconductor industry.