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MICROPROCESSOR REPORT

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PREVIEW: SPRING PROCESSOR FORUM

Highlights Are IBM's Cell, DSPs, IP Cores, and New Track Sessions

By Tom R. Halfhill {4/28/05-01}

It's not a conference exclusively for embedded processors any more, but embedded processors and cores will nevertheless make the biggest news at this year's **Spring Processor Forum** (formerly Embedded Processor Forum). Innovation is running wild in the embedded industry, and SPF 2005 will be a showcase for radical multicore designs, aggressive new DSPs, new embedded-processor architectures, and much more.

The forum, sponsored by In-Stat (publisher of *Microprocessor Report*), will be held May 16–19 at the Doubletree Hotel in San Jose, California. Note the new venue. After several years at the Fairmont Hotel, the forum is moving to the newly renovated Doubletree, which is adjacent to San Jose International Airport and has plenty of free parking. (No more $18-a-day parking tabs on your expense report.) The four-day forum consists of a two-day conference (Tuesday and Wednesday, May 17–18) bracketed by two days of seminars (Monday, May 16, and Thursday, May 19). As usual, there will be an exhibition and reception on Tuesday evening, May 17.

New this year are special-interest tracks on the second day of the conference and the return of the popular "Birds of a Feather" confab later that afternoon. These tightly focused tracks and sessions will offer more opportunities to learn about timely technologies, such as video-processing engines, audio extensions for licensable processor cores, and performance benchmarking. The "Birds of a Feather" session is an informal panel discussion that encourages more audience participation—particularly important when the subject is benchmarking, a frequent source of controversy.

This year's all-day seminars are equally relevant. Monday's seminar is "Multicore Processors For Computing and Networking," led by Kevin Krewell, a principal analyst at In-Stat and editor in chief of *MPR*, and Jim McGregor, an In-Stat senior analyst and senior editor for *MPR*. This seminar will explore the design trade-offs of multicore processors from leading CPU vendors such as AMD, Applied Micro Circuits Corp. (AMCC), Broadcom, IBM, Intel, PMC-Sierra, and Sun Microsystems. It will address the issues of core selection, core interconnects, memory and I/O system design, die-size and power trade-offs, and the different workloads targeted by these leading CPU vendors.

Thursday's seminar is "High-Performance SoCs for Low-Power Applications," led by Max Baron, a principal analyst at In-Stat and senior editor of *MPR*. This seminar will explain how SoC vendors use architecture, microarchitecture, software, and power management to obtain the high performance required for mobile markets while achieving the best combination of power consumption, integration, and flexibility. Following a brief tutorial on low-power techniques, the seminar will analyze and compare more than 25 cores, chips, and SoCs, including the latest introductions aimed at cellphones, digital cameras, PDAs, and other low-power systems.

Separate admissions are available for the conference, the seminars, and the exhibition, as well as discount packages for multiple events. For more information, visit *www.in-stat.com/spf/05/*.

Lots of New Licensable IP

To launch the two-day conference, **Mentor Graphics** CEO Walden C. Rhines will deliver a keynote address about the

true ramifications of Moore's law and the challenges facing a semiconductor industry striving to obey it. Following the keynote, the first conference session is "High-Performance Licensable-IP Processor Cores," chaired by the author of this article. This busy session has six presentations, an indicator of the lively competition in the licensable intellectual-property (IP) market.

Leading off is **ARC** with "Silicon-Thrifty Floating-Point Extensions for ARC Processors" by Peter Wells, director of solution architects at ARC. This is the first time ARC has introduced floating-point acceleration for its low-power configurable processor, the ARC 600, and for its highest-performance configurable processor, the ARC 700. (See *MPR 12/15/03-01*, "ARC Alters Trajectory," and *MPR 6/21/04-01*, "ARC 700 Secrets Revealed.")

Cambridge Consultants comes next with "XAP3: A New 32-Bit Processor Core With High Code Density." The synthesizable XAP3 introduces a new 32-bit architecture evolved from the company's earlier XAP1 and XAP2 16-bit processors. XAP3 is designed for integration in ASICs, ASSPs, SoCs, and FPGAs, and it uses a modeless mix of 16- and 32-bit instructions to pack more program code into memory. Alistair Morfey, technology director at Cambridge Consultants, will describe the new instruction-set architecture and explain how it's optimized for target applications.

The Brits aren't done yet. Bristol-based **Elixent** will present "The Massively Parallel D-Fabrix v2.0 Processor Core." Elixent, a five-year-old spinoff from Hewlett-Packard Labs, first unveiled its extreme D-Fabrix architecture at Embedded Processor Forum 2003. (See *MPR 7/21/03-01*, "Elixent Expands SoCs.") D-Fabrix is based on a concept Elixent calls reconfigurable array processing (RAP). The first D-Fabrix processor was a configurable hard macro with up to thousands of four-bit ALUs and other elements. After performing extensive profiling on wireless and multimedia applications with key customers in mobile and consumer electronics, Elixent has refined the architecture. Elixent CTO Alan Marshall will explain how D-Fabrix v2.0 improves the performance of the company's latest processor core while significantly reducing die size and power consumption.

MIPS Technologies will shift the focus back to Silicon Valley by presenting "A High-Performance MIPS32 RISC Processor With DSP Enhancements." Engineering manager Chinh Tran will describe a new 32-bit synthesizable core based on the popular MIPS32 24K processor and incorporating the latest DSP application-specific extensions (ASE) from MIPS. (See *MPR 11/1/04-02*, "MIPS Takes Aim at Low-Cost DSP.") MIPS says the new core, like the 24K core, will be the highest-performance 32-bit soft processor for general-purpose embedded applications. The presentation describes how engineers leveraged existing logic to add the DSP extensions without impairing the performance of general-purpose instructions.

Silicon Hive, a Philips-funded startup from the Netherlands, follows with "The Avispa Family of ULIW Parallel-Processing Cores for Multimedia and Communications." Silicon Hive introduced its ultralong instruction-word (ULIW) architecture at Microprocessor Forum 2003 (see *MPR 12/1/03-02*, "Silicon Hive Breaks Out"), and the first-generation Avispa+ processor won our *MPR* Analysts' Choice Award for Best Soft-IP Processor Core of 2003. (See *MPR 2/9/04-18*, "Avispa+ Buzzes With Innovation.") Now, Silicon Hive is announcing two newly enhanced Avispa cores for embedded applications. The speaker is Dr. Jeroen Leijten, chief processor architect and cofounder of Silicon Hive.

Xilinx wraps up the licensable-IP session with a presentation entitled, "MicroBlaze: An Enhanced 32-Bit Processor Core for FPGA Integration." Ralph Wittig, director of engineering for the Embedded Processing Division at Xilinx, will disclose the first technical details about the company's new MicroBlaze 4.0 synthesizable processor core, which is specially optimized for implementation in programmable logic. MicroBlaze has some new user-configurable features sure to be of interest to embedded-system developers, and it will compete directly with Altera's Nios II. (See *MPR 6/28/04-02*, "Altera's New CPU for FPGAs.") The licensable-IP session will conclude with analysis by *MPR* before all the speakers return to the stage to answer questions from the audience.

New High-Performance Embedded Processors

After lunch comes the next session, "High-Performance Embedded Processors," chaired by Kevin Krewell, In-Stat

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principal analyst and editor in chief of *MPR*. Four companies will give presentations in this session, followed by the customary analysis and question-and-answer period.

AMCC will lead off by announcing the newest members of its PowerPC 440 family—an embedded-processor family the company acquired from IBM last year. (See the sidebar "AMCC Strikes a Big Deal for PowerPC" in *MPR 4/26/04-02*, "IBM Loosens Up CPU Licensing.") At Fall Processor Forum 2004, AMCC introduced the PowerPC 440SPe I/O processor (see *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF"), and it's a good bet that AMCC's announcements at SPF 2005 will also be oriented toward networking. AMCC's presenter is Xavier Bocquet, senior manager of engineering for AMCC embedded products.

Marvell Semiconductor follows with a presentation entitled "Feroceon: A Scalable, Low-Power, High-Performance, and Low-Cost Superscalar Processor Supporting the ARM ISA." Normally, ARM cores are associated with low power and high code density, not the kind of high performance required for a leading-edge network processor. However, Marvell is using some techniques never before seen in an ARM-compatible core. This processor will offer new competition for MIPS- and PowerPC-based network processors. Marvell's presenter is Dr. Sehat Sutardja, cofounder and CEO.

Matsushita Electric Industrial comes next with "An Instruction Parallel-Processor (IPP) Architecture on the Panasonic Integrated Platform for Digital Consumer Electronics." Masaitsu Nakajima, general manager of Matsushita's Processor Development Group, will describe a new media-processor architecture intended to support a host processor in consumer-electronics products. Matsushita's main goal is to standardize the processing platform across a wide range of those products to reduce development costs. The new architecture uses several techniques for efficient multimedia processing.

Raza Microelectronics (RMI) wraps up the session with a presentation entitled "A Next-Generation MIPS64 Multiprocessor" by David Hass, lead senior architect. Raza has been secretly working on this project for two years, and its SPF presentation will be the first significant disclosure of this new 64-bit MIPS-compatible processor family. The family will include multicore processors for networking and other applications.

The Return of Cool Technology

At Fall Processor Forum 2004, attendees were fascinated by IBM's presentation of the BlueGene/L supercomputer processor, a highlight of the "Cool Technology" session. SPF will have an expanded session called "Cool Processing Technologies," chaired by In-Stat principal analyst and *MPR* senior editor Jim McGregor. Unlike some of our other sessions, this one will append a five-minute question-and-answer session to each presentation instead of having a general-discussion panel at the end of the session.

Imagination Technologies will lead off with a presentation on its Universal Communications Coprocessor (UCC), a licensable-IP core designed for baseband decoding. This coprocessor has configurable signal-processing blocks that perform functions common to most radio standards plus a specialized programmable processor supporting demodulation and modulation functions. The presenter is Peter McGuinness, director of business development.

Intrinsity follows with "The Design of a Multi-Gigahertz Pipeline Control Unit Using Fast14 Technology," presented by Terry Potter, senior member of the technical staff. Late last year, Intrinsity changed its business model. No longer a fabless semiconductor company, Intrinsity has turned to licensing its unique flavor of dynamic logic. (See *MPR 1/10/05-02*, "Intrinsity Takes Its IP on the Road.") In this presentation, Intrinsity will give a practical example of using its licensable technology and design tools.

Rapport comes next with "Kilocore: Low-Power Parallel Computing on a Chip" by Dr. Andrew Singer, CEO and CTO. The new Kilocore architecture can integrate hundreds of tiny processor cores on a single chip that consumes significantly less than a watt. Rapport is billing its device—intended for low-power data-intensive applications—as "the first parallel computer on a chip."

Sun Microsystems returns to the conference with "Niagara: Sun's Radical Realization of Chip Multithreading," presented by William Bryg, distinguished engineer. Bryg will disclose new technical insights about Niagara's unique threading model, which allows the eight-core Niagara processor to execute up to 32 threads simultaneously. Sun's quad-threading technology overcomes the difficulties encountered by other multithreading models when attempting to execute so many threads. (See *MPR 9/13/04-02*, "Sun's Niagara Pours on the Cores.")

Tarari (rhymes with Atari) will wrap up the session by introducing a multicore, multifunction content processor for networking. This chip integrates security features and an XML offload engine (dubbed an XOE by In-Stat senior analyst Eric Mantion) to assist a host network processor with Layer 7 traffic management. The presenter is Jeff Carmichael, Tarari's CTO and vice president of engineering.

After concluding the "Cool Processing Technologies" session with McGregor's analysis of the presentations, the conference will adjourn for the day. All attendees are invited to the vendor exhibition and reception, which continues until 8:30 p.m.

Digital-Signal Processing Takes the Stage

On Wednesday morning, the conference resumes with our "Advances In DSP Engines" session, chaired by Max Baron, In-Stat principal analyst and senior editor of *MPR*. Seven presentations are scheduled for this session, including two by the leading DSP vendor, Texas Instruments. These presentations will announce or disclose new details about DSP chips, multiprocessors, DSP cores, and special-purpose accelerators.

ARM begins the session with "A Portable Media Architecture Implemented on OptimoDE" by Steve Steele, business development manager. Using its licensable OptimoDE architecture, ARM has designed a data-engine core optimized for running digital-audio codecs. (See *MPR 6/7/04-01*, "ARM's Configurable OptimoDE.") ARM will present data showing how the engine dramatically improves audio performance with a host processor.

Ceva follows with a presentation entitled "Advanced Memory Architecture of the Ceva-X1621 VLIW/SIMD DSP" by Avi Davis, senior DSP architect. Davis will describe the enhanced memory system of Ceva's newest licensable DSP, the Ceva-X1621, which follows the company's Ceva-X1620, introduced last year. We nominated the Ceva-X1620 for an *MPR* Analysts' Choice Award as Best Licensable DSP Core of 2004; see *MPR 1/10/05-01*, "DSPs Accelerate in 2004."

Next, **Freescale Semiconductor** will unveil its MXC91231 Edge Processor in a presentation by Jose Corleto, systems and architecture manager. This new processor is based on Freescale's MXC architecture announced in October 2003. (See *MPR 11/17/03-02*, "Jupiter's Twin Cores.") It combines an ARM core and a StarCore DSP in a single chip, eliminating the need for a separate application processor.

InterQoS Systems follows with "Processor Network Executes Multimedia and Graphics" by Ron Hui. Using a matrix of processing elements, this new architecture exploits parallelism to lower the processor's clock frequency and save power. It's designed for video applications and games with 3D graphics.

LSI Logic is next with "A Quad-MAC DSP Core Targeting Wireless Handset Applications" by Brendon Slade, director of DSP solutions engineering. Slade will introduce a new licensable DSP core in LSI Logic's ZSP line, which includes the ZSP500 and ZSP600 series. (See *MPR 3/17/03-04*, "ZSP500 and Jazz Play Different Beats.") The new core is designed for communications workloads.

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After a break, **Texas Instruments** weighs in with two back-to-back presentations. First is "TMS320C55x+ Architecture Lowers Power, Increases Performance" by Jean-Pierre Giacalone, distinguished member of TI's technical staff. This enhancement of TI's popular C55x architecture has an improved memory hierarchy and is intended to deliver greater performance and lower power. TI's second presentation is "High-Performance TMS320C6000 Architecture Extensions Target Video and Communications Infrastructures" by Nat Seshan, distinguished member of TI's technical staff. TI promises to reveal the latest C6000 architectural innovations at the conference.

Instead of a general panel discussion followed by audience questions, the DSP session will append a five-minute question-and-answer period onto the end of each presentation.

IBM Microelectronics will precede the lunch break with a special 45-minute presentation about the new Cell microprocessor architecture. This is certain to be a high point of the conference, because no other processor announced this year has generated as much excitement in both the trade press and the mainstream press. Cell, of course, is the chip destined for Sony's next-generation PlayStation 3 home videogame console. However, IBM has much greater ambitions for Cell, which is based on IBM's Power architecture augmented by numerous on-chip coprocessors. (See *MPR 2/14/05-01*, "Cell Moves Into the Limelight," and *MPR 1/3/05-01*, "New Patent Reveals Cell Secrets.") This special presentation will be delivered by Jim Kahle, an IBM Fellow who helped lead the Sony-Toshiba-IBM (STI) design team in Austin, Texas.

Keeping Track of Audio and Video

After Wednesday's lunch, something new happens: the conference separates into multiple tracks for the first time. This will allow SPF to accommodate the demand for more presentations while providing more-specialized information for attendees. There will be two simultaneous tracks of presentations in adjacent conference rooms, and all badged attendees are free to move back and forth. One track session is "Processing Engines for Video Applications," chaired by Jeff Bier, cofounder and general manager of Berkeley Design Technology Inc. (BDTI). The parallel track session is "Audio Extensions for Licensable Processor Cores," chaired by the author of this article.

Bier's video track will focus on off-the-shelf chips and licensable cores that use a variety of architectures to meet the demands of digital video, and it will cover RISC processors, DSPs, and configurable processors. The primary target markets for these processors are surveillance cameras, digital TV, video cameras, video recorders, and other consumer video products.

Altera begins the video track with a presentation entitled "Stratix-II FPGAs As Cost-Effective Video Engines" by Brian Jentz, DSP marketing manager. Jentz will describe how to apply

high-end FPGAs to demanding video tasks normally performed by dedicated video processors and media processors. Altera's assertion is that FPGAs can perform those tasks more cost-effectively than conventional programmable chips can.

Cradle Technologies will present "A High-Performance Multiprocessor DSP for Multimedia Infrastructure" by Erik Machnicki, processor architect. Machnicki will disclose new technical details about the CT3600 family, the next generation of Cradle's multiprocessor DSPs for video applications. Cradle believes the industry is finally recognizing the value of Cradle's multiprocessing philosophy and cites IBM's Cell as one example. We nominated Cradle's existing ECE3400/MPE3400 for an *MPR* Analysts' Choice Award as Best Extreme Processor of 2003. (See *MPR 2/9/04-15*, "Extreme CPUs Defy Conventions.")

On Demand Microelectronics wraps up the video track with "A Scalable, Low-Power Processor for DTV Applications" by Gerald Krottendorfer, CTO. This new licensable processor core for digital TV uses SIMD (single instruction, multiple data) and MIMD (multiple instructions, multiple data) to exploit data parallelism. It also has a sophisticated memory controller to accelerate data movement. On Demand is a new company based in Vienna, Austria.

Licensable IP for Digital Audio

Wednesday afternoon's alternate track, "Audio Extensions for Licensable Processor Cores," offers technical presentations about digital-audio extensions and coprocessors for licensable-IP embedded-processor cores. These extensions may include additional instructions or even complete coprocessor engines. Their primary targets are MP3 players, multifunction cellphones, set-top boxes, and other consumer-electronics products.

ARC International begins the track with "ARCsound: Audio Extensions for Low-Power Applications." Peter Wells, director of solution architects at ARC, will describe the ARCsound subsystem, which includes a preconfigured ARC 32-bit processor core, DSP extensions, additional extension instructions, software codecs, a sample implementation, and software-development tools. ARC's presentation covers the extensions in some detail, including examples and performance metrics.

ARM is up next with its presentation "Audio Applications on ARM Processors" by Travis Lanier, NEON product manager. Lanier will review the evolution of DSP at ARM and compare the various extensions, including the NEON technology announced late last year and the new OptimoDE-based data engine announced earlier at this forum. Lanier's presentation offers performance measurements and additional technical details to explain which extensions are appropriate for various applications.

For More Information

Spring Processor Forum 2005 will be held May 16–19 at the Doubletree Hotel in San Jose, California. The conference is on May 17–18 (Tuesday and Wednesday), and the all-day seminars are on May 16 and May 19 (Monday and Thursday). The exhibition and reception will take place Tuesday evening. To learn more about Spring Processor Forum or to register online, please visit our website at *www.in-stat.com/spf/05/conf.htm*.

MIPS Technologies will deliver the next presentation, "The MIPS Consumer Audio Platform" by Radhika Thekkath, director of architecture. MIPS offers a large library of audio codecs optimized for its 32- and 64-bit processor cores. In a series of slides with benchmark tables, Thekkath will show how performance varies with different-size caches and other configuration options.

Tensilica finishes the audio track with a technology preview of its next-generation HiFi-2 audio engine for the Xtensa LX configurable processor core. Robert Kennedy, senior software engineering manager, will unveil new codecs and features that improve performance while reducing power consumption. HiFi-2 is an enhancement of Tensilica's existing audio extensions for the Xtensa V processor core.

"Birds of a Feather": Benchmarking

For the first time in years, the so-called "Birds of a Feather" session is returning to the forum. This discussion panel is more interactive than the formal conference and track presentations are. Give and take with the audience is not only encouraged but expected. And with this year's panel focused on the challenges of benchmarking—a controversial topic, even in formal circumstances—there's sure to be plenty of give and take.

The panel will be chaired by Kevin Krewell, *MPR* editor in chief. Panel members will include Mike Goddard from **AMD**, Jeff Bier from **BDTI**, Markus Levy from **EEMBC**, Tero Sarkkinen from **FutureMark**, and Walter Bays from **SPEC** (Standard Performance Evaluation Corp.). These expert panelists are qualified to talk about all levels of benchmarking, from microprocessors to systems, and they span the range from embedded processors to server processors. If the "Birds of a Feather" session turns out to be anything like the benchmarking panel at Fall Processor Forum, sparks are sure to fly. (See *MPR 11/8/04-01*, "FPF '04 Benchmarking Panel.")

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THE EDITORIAL VIEW

Let's Retire Moore's Law at 40

By Kevin Krewell {4/25/05-02}

Intel trotted out Gordon Moore one more time in an attempt to prove that Intel sets the agenda for the industry. But Moore's Law isn't really about Gordon Moore any more; it's about setting the agenda and pace for the semiconductor industry. Intel isn't the first company to build dual-core processors, but when Intel announces that its roadmap is going completely to dual- and multicore processors, the press takes notice.

Moore's law is supposed to be this unstoppable locomotive in semiconductors, yet in embedded processors many companies are getting off the train at 130nm, 180nm, and even 250nm. I was recently briefed by ARM about its DesignStart Program, which gives free early design access to the ARM7TDMI core in 180nm, and was surprised to find out that about half of ARM's new design starts are still in 180nm. Some designs, especially in microcontrollers, will likely stay at older process generations for lower wafer and mask cost, more-robust ESD characteristics, and resistance to higher voltages, as well as because the designs don't need to go any faster or get any smaller.

Tom Halfhill, in his Viewpoint article in 2004 (see *MPR 12/13/04-02*, "The Mythology of Moore's Law"), talked about the various (mis)interpretations of Moore's law and how it changed over time. It hasn't been a completely stable "law" and has been subject to revisions and interpretation. I recommend subscribers read Halfhill's article to understand the intent behind Gordon Moore's projections.

When Gordon Moore first made the prediction, he was at Fairchild, and the products were MSI logic devices. He last updated his predictions in 1975, when the microprocessor industry hadn't yet taken off. Intel was still primarily in the DRAM and general LSI logic business. Since that time, Intel applied Moore's Law to microprocessors and widened the interpretation to include not just mainstream processors but also the ultralarge-die-size Itanium processors.

What Moore's Law Has Wrought

Moore long ago lost control of his law, and Intel, apparently, believes it owns the intellectual-property rights to it and can do with it as Intel pleases. Which is why we need to retire Moore's law. The semiconductor industry needs to follow the process roadmap that it finds economically advantageous to the industry and not dance to a preprogrammed tune. Each new process generation brings great expenses, greater risks, and, in some cases, diminishing performance returns. On its website, Intel says, "Our R&D investment and silicon expertise support unique Intel breakthroughs that will enable us to drive Moore's law well into the future and deliver more exciting capabilities into our technologies." The question the industry needs to answer is this: Do you want Intel (and the IDMs that follow Intel's path) *driving* the industry?

AMD, Intel, and server-processor vendors do not focus on making smaller and cheaper chips but rather on putting more features into roughly similar-size die. Some embedded designers are using advanced semiconductor processes to put multiple processor cores and other functions onto one die, which can enable new products that were not possible just a

few years ago. That is the progress we associate with Moore's law. But this progress relies on money, and each new process generation requires even more money. Intel has plenty of money to spend, and it uses that money to fund its semiconductor research and fabs. But those fabs and the company's latest-generation process haven't always produced winners. Intel's 90nm process produced a Pentium 4 that had much higher leakage currents than were produced using the preceding 130nm process and didn't reach the 4GHz goal the company set for it. Despite converting most of its products to 90nm, Intel couldn't clearly beat AMD (except in mobile), which continues to ship a considerable number of 130nm products. My point is this: Being first to a new process isn't a guarantee of success, and using an older, but appropriate, process does not signal failure.

Gordon Moore retired; shouldn't his "law" get to retire, too?

Spring Processor Forum Reminder

It's spring, and the first buds of new processors are starting to appear (single-core and multicore versions). They will be in full bloom at the **Spring Processor Forum,** May 16–19, at the Doubletree Hotel in San Jose. Make your plans now to be there and enjoy the new crop. And we encourage you to consider submitting presentations on your new processor or processor-related technology for our **Fall Processor Forum** (October 24–27) and **Processor Forum Taiwan** (November 9–10).