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FREESCALE QUICKENS POWERQUICC

New PowerQUICC II Pro Chips Have Two Auxiliary Processors

By Tom R. Halfhill {3/21/05-01}

It's been 10 years since Motorola created the PowerQUICC family of communications processors by substituting PowerPC cores for the 68360 CPUs in the original QUICC family. (QUICC, rarely spelled out these days, stands for QUad Integrated Communications Controller.) Now, Motorola spinoff Freescale is again improving the family with additional auxiliary processors, on-chip peripherals, I/O interfaces, and networking accelerators.

Also, Freescale has developed some asynchronous on-chip bus technology that allows different logic blocks on the new chips to run more efficiently in their own clock-frequency domains. Freescale is secretive about this technology while applying for patents, but it sounds similar in concept to the asynchronous buses found in some high-performance networking processors from PMC-Sierra.

In another interesting development, Freescale plans to next year ship software tools that will make the auxiliary processors in the new PowerQUICC chips fully programmable for the first time. At present, customers can interact with PowerQUICC auxiliary processors only by using Freescale's device drivers.

The new chips belong to the PowerQUICC II Pro series and are called the MPC8360E and MPC8358E. (Freescale will also offer them without integrated security engines as the MPC8360 and MPC8358; otherwise, they are identical to the MPC8360E and MPC8358E.) Both new chips have PowerPC e300 cores, which are software compatible with other PowerQUICC chips based on the PowerPC e300 and 603e cores. Likewise, the new chips' auxiliary processors are compatible with those in earlier PowerQUICC chips, so existing customers should have little trouble migrating their software. Freescale says it will begin sampling the chips in 3Q05 and make production quantities available in 1Q06.

Freescale Overhauls the Engine Room

Most existing chips in the populous PowerQUICC family (PowerQUICC I, PowerQUICC II, and PowerQUICC III) have a PowerPC core supplemented by a logic block known as the communications processor module (CPM). The CPM offloads networking tasks from the PowerPC, supports on-chip peripherals, and provides numerous I/O interfaces to the system. Software running on the CPM's auxiliary processor usually handles network-protocol processing and other data-plane tasks, freeing the PowerPC core to run an operating system and other control-plane tasks.

The first PowerQUICC II Pro chips, introduced last year, lack CPMs, although they do have Ethernet controllers, security engines, and other features for networking and communications. (See *MPR 5/10/04-02*, "Freescale Secures PowerQUICC.") However, those earlier PowerQUICC Pro II chips are exceptions to the rule—it's primarily the CPM that differentiates PowerQUICC chips from discrete PowerPC processors. In its new PowerQUICC II Pro chips, Freescale is adding a much-improved communications engine that goes beyond the capabilities of the existing engine.

In the existing CPM, there's one auxiliary processor based on a proprietary RISC architecture. The auxiliary processor can run at a different clock frequency than the PowerPC core does, but only at fixed ratios of 2.0, 2.5, or 3.0 times the speed of the system bus. Customers can control the CPM using Freescale's supplied device drivers, but they can't directly configure or program the auxiliary processor.

In contrast, the new PowerQUICC II Pro chips have a new module called the QUICC Engine. It can integrate one, two, or four auxiliary processors, instead of just one. Thanks to Freescale's new on-chip bus technology, these auxiliary processors can run at their own clock frequency, independent of either the PowerPC core or the system bus. And when Freescale ships its new software-development tools next year, customers will be able to program the auxiliary processors instead of relying exclusively on canned device drivers.

Both new PowerQUICC II Pro chips have QUICC Engines with two auxiliary processors. Future members of the family will scale upward or downward by integrating four auxiliary processors or a single auxiliary processor. Freescale says the MPC8360E will be available in several speed grades, with the PowerPC e300 core running at clock frequencies as high as 667MHz; the auxiliary processors in those chips will run at frequencies from 200MHz to 500MHz. The MPC8358E will be available in multiple speed grades, too, with its PowerPC core running at 266MHz to 400MHz; the auxiliary processors will run at 200MHz to 400MHz. The block diagram in Figure 1 is a top-level view of the new PowerQUICC II Pro design.

Note that the clock frequencies of the new chips don't break any records for the PowerQUICC family. The PowerPC cores in some PowerQUICC III devices run as fast as 833MHz, and the auxiliary processors in their CPMs run at speeds up to 333MHz. Nevertheless, the new chips should outperform most of their brethren, because the new QUICC Engines have twice as many auxiliary processors as existing CPMs as well as many other improvements.

One improvement is the mysterious asynchronous on-chip bus. In theory, an asynchronous bus should increase efficiency by wasting fewer clock cycles on wait states and other timing penalties when negotiating among logic blocks running at different frequencies. A big challenge of designing modern communications processors is accommodating the mismatches among the great number of different logic blocks and I/O interfaces operating at dramatically different clock speeds. These chips have everything from superfast CPU cores and Gigabit Ethernet controllers to pokey UARTs. Getting all of them to work together on the same chip is like driving a herd of horses in which some animals are thoroughbred racers and others are 20-year-old plow horses.

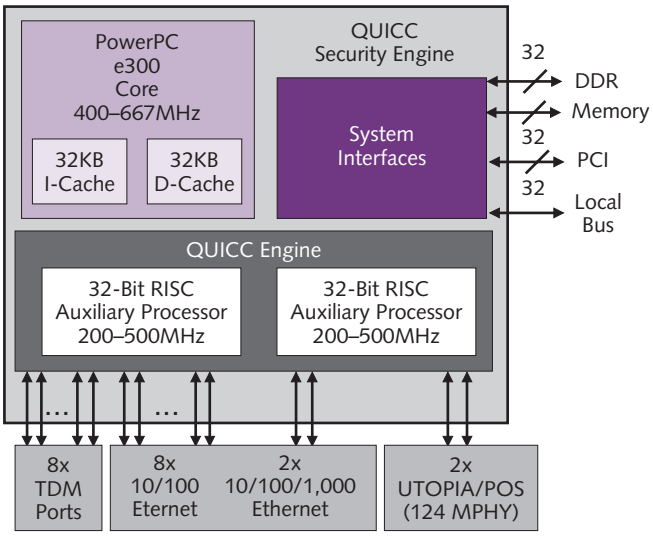

Figure 1. New PowerQUICC II Pro chips have a PowerPC e300 processor core, a QUICC Engine with two auxiliary RISC processors, much-improved I/O capabilities, and an optional security engine. This block diagram shows the MPC8360E, but the MPC8358E is similar.

PMC-Sierra has tackled this problem in some of its high-performance processors by using a novel asynchronous crossbar bus. The new RM11200, introduced at Fall Processor Forum 2004, has such a bus. It's based on asynchronous-logic technology licensed from Fulcrum Microsystems. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.") Freescale says it's keeping details about the PowerQUICC II Pro on-chip bus under wraps while applying for patents, which implies that the asynchronous technology is home-grown, not licensed.

No matter how it works, there are obvious benefits to decoupling the QUICC Engine auxiliary processors from the PowerPC core and other logic blocks. One is fewer wasted clock cycles. Another is that future modifications or extensions of the designs may be easier for Freescale to implement, because the asynchronous interfaces don't require the tight integration of a synchronous interface.

QUICC Engine Has Unified I/O Controllers

I/O interfaces are significantly improved in the new QUICC Engine. The CPMs in existing PowerQUICC chips have three fast communications controllers (FCC) for ATM, Fast Ethernet, and transparent I/O modes; four serial communications controllers (SCC) for 10Mb/s Ethernet, UARTs, and other slow serial interfaces; and two multichannel communications controllers (MCC) for high-level data-link control (HDLC). In contrast, the QUICC Engine pulls all that controller logic together into either six (MPC8358E) or eight (MPC8360E) unified communications controllers (UCC), plus a single MCC.

The new unified controllers can manage several protocols: ATM, Gigabit Ethernet, Fast Ethernet, regular Ethernet, USB, SPI, and transparent I/O modes. The UCCs provide Media-Independent Interfaces (MII) or Reduced MII (RMII) for eight 10–100Mb/s Ethernet ports, plus two Gigabit MII (GMII) ports for Gigabit Ethernet. They also have an integrated time-division multiplexer (TDM).

The QUICC Engine supports a pair of Utopia-2 ports, as do the CPMs in existing PowerQUICC chips. However, the QUICC Engine's Utopia-2 interfaces can support ATM and other packet data at OC-12 rates (622.08Mb/s), whereas the CPM is limited to OC-3 (155.52Mb/s). In addition, Freescale added more hardware acceleration for networking tasks. The QUICC Engine accelerates some Layer 3 functions, as well as

Layer 2 functions, and it offloads packet forwarding, parsing, and switching tasks from the PowerPC core. CPMs in previous PowerQUICC chips accelerated some Layer 2 functions, but not Layer 3 or the internetworking tasks. All these improvements make the new PowerQUICC II Pro chips more suitable for higher-end networking and packet-communications systems. Table 1 summarizes the differences between the QUICC Engine and CPM.

Until now, customers had to be satisfied with the CPM device drivers supplied by Freescale or third-party providers, because the auxiliary processors—based on a proprietary RISC architecture—weren't user programmable. Application software could interact with the auxiliary processors only by calling API routines in the standard drivers. This isn't unusual for networking chips with proprietary auxiliary processors; access to the RISC engines in Intel's IXP-series chips is similarly limited. However, some customers would like to interact more directly with the auxiliary processors.

For that reason, Freescale now provides a software tool that lets customers configure the device drivers by setting various properties. The new *CodeWarrior QUICC Engine Utility* works much like the visual programming tools that have property sheets. To change the properties of a device driver (and, therefore, the operation of an associated communications controller), users simply point and click. The next step is full programmability, and Freescale plans to ship those tools next year. When customers can write their own microcode for the auxiliary processors, they'll be able to create custom device drivers or implement protocols not supported by Freescale's drivers. Programmability will provide another way for customers to optimize and differentiate their designs.

As mentioned before, the new PowerQUICC II Pro chips are available with or without integrated security engines. Chips with security have the "E" suffix (as in MPC8360E), a common nomenclature across the PowerQUICC family.

Feature	QUICC Engine MPC8360E	QUICC Engine MPC8358E	CPM Existing PowerQUICC Chips
Product Families	PowerQUICC II Pro MPC8360, MPC8360E	PowerQUICC II Pro MPC8358, MPC8358E	PowerQUICC I, PowerQUICC II, PowerQUICC II Pro, PowerQUICC III
Auxiliary Processors	2 (1, 2, or 4 in future)	2 (1, 2, or 4 in future)	1
Aux Processor Clock Freq	200–500MHz	200–400MHz	133–333MHz
Asynchronous Clocking	Yes	Yes	—
Configurable Microcode	Yes	Yes	—
Programmable Microcode	Planned for 2006	Planned for 2006	—
Utopia-2 Interface	2 interfaces OC-12 ATM/POS 128 MultiPHY each	2 interfaces OC-12 ATM/POS Single 31 or 124 MultiPHY	2 interfaces OC-3 ATM 31 MultiPHY each
Media-Independent I/F (MII) Reduced MII (RMII) 10–100Mb/s Ethernet	8	6	3
Gigabit MII (GMII) 10–1000Mb/s Ethernet	2	2	—
Time-Division Multiplexers	8	4	8
Multichannel Controllers (High-level Data Link Control)	1 controller 256 HDLC channels	1 controller 128 HDLC channels	2 controllers 128 HDLC channels each
Unified Comm Controllers	8 UCCs for ATM, Fast Ethernet, GbE, transparent mode, slow serial protocols	6 UCCs for ATM, Fast Ethernet, GbE, transparent mode, slow serial protocols	—
Fast Comm Controllers	—	—	3 FCCs for ATM, Fast Ethernet, transparent mode
Serial Comm Controllers	—	—	4 SCCs for 10Mb/s Ethernet, UARTs, other slow serials
Layer 2 Acceleration	Yes	Yes	Yes
Layer 3 Acceleration	Yes	Yes	—
Internetwork Acceleration	Yes (Offloads forwarding, switching, parsing)	Yes (Offloads forwarding, switching, parsing)	—
Networking Performance	1.2Gb/s interworking 2Gb/s termination	960Mb/s interworking 1.5Gb/s termination	Up to 700Mb/s L2 termination

Table 1. Freescale has overhauled the communications processor module (CPM) in existing PowerQUICC chips to create the improved QUICC Engine in the new PowerQUICC II Pro MPC8360E and MPC8358E. In general, the controller logic is more unified and I/O is faster. Key differences between the QUICC Engines in the MPC8360E and MPC8358E are highlighted in purple.

("E" stands for "encryption".) The integrated security engine is identical to the enhanced SEC 2.0 engine introduced last year in the PowerQUICC II Pro and PowerQUICC III series. This engine is software-compatible with device drivers for Freescale's MPC184 and MPC185 standalone security coprocessors. (See *MPR 5/10/04-02*, "Freescale Secures PowerQUICC.")

Large PowerQUICC Family Keeps Breeding

As always, Freescale is aiming its latest PowerQUICC processors at high-volume communications and networking applications in both the client and service-provider sectors of the market. Over the past 10 years, the company has sold more than 185 million of these chips to more than 350 customers, accumulating more than 5,000 design wins.

The new PowerQUICC II Pro chips are suitable for small- to medium-size routers, DSL access multiplexers (DSLAM), broadband concentrators in multitenant units, wireless base stations, WiMAX wireless broadband access equipment, switches in packet-based telephone exchanges, and other systems requiring packet acceleration and support for multiple protocols. The variety of I/O interfaces and protocols supported by these chips is awesome, and their security engines are among the best.

PowerQUICC processors compete against similar chips from AMD, Broadcom, Intel, PMC-Sierra, and several other companies. All these vendors are in an arms race of sorts, rushing to keep up with evolving I/O standards and communications protocols. It's not an easy race, because industry standards and customer expectations keep changing

Feature	Freescale MPC8360E	Freescale MPC8358E	Freescale MPC8349E	Freescale MPC8541E	AMD Au1550	Intel IXP465
General Features						
Chip Family	PowerQUICC II Pro	PowerQUICC II Pro	PowerQUICC II Pro	PowerQUICC III	Alchemy	IXP4xx
CPU Core	PowerPC e300	PowerPC e300	PowerPC e300	PowerPC e500	Enhanced MIPS32	XScale
Core Freq	400–667MHz	266–400MHz	400–667MHz	533–833MHz	333–500MHz	266-667MHz
Networking Engine Aux Processors Aux Freq	QUICC Engine 2 200–500MHz	QUICC Engine 2 200–400MHz	—	—	—	NPE 3 133MHz
DDR Freq	266/333MHz	266/333MHz	266–333MHz	266–333MHz	200–400MHz	266MHz
L1 Cache (I/D)	32K/32K	32K/32K	32K/32K	32K/32K	16K/16K	32 /32K
L2 Cache	—	—	—	256K	—	—
FPU	64-bit	64-bit	64-bit	64-bit	—	—
Mul-Accum Unit	—	—	—	—	32 x 16-bit	—
MMU	Yes	Yes	Yes	Yes	Yes	Yes
Voltage (Core, I/O)	1.2V, 3.3V	1.2V, 3.3V	1.2V, 3.3V	1.2V, 3.3V	1.2V, 3.3V	1.4V, 3.3V
Total Power (typical)	3–5W	3–5W	2.5–4.5W	3.9–5.4W	<500mW (400MHz)	2.8W–3.4W*
Package	TBGA-740 37.5 x 37.5mm	TBGA-740 37.5 x 37.5mm	TBGA-672 35 x 35mm	FCPBGA-783 29 x 29mm	PBGA-483 21 x 21mm	PBGA-544 35 x 35mm
Production	1Q06	1Q06	2Q05	4Q04	2Q04	Mar-05
Price (10K)	$44+	$34+	$20–50	$72–102	$21–34	$26–62
On-Chip Peripherals & Interfaces						
DRAM Controller Bus Width	DDR 32/64 bits	DDR 32 bits	DDR 32/64 bits	DDR 64 bits	DDR 16/32 bits	DDR 32 bits
ROM-SRAM-Flash	Yes	Yes	Yes	Yes	Yes	Yes
DMA Controller	Yes	Yes	Yes	Yes	Yes	PCI only
Serial Protocols	SPI, MDIO	SPI, MDIO	I^2C, SPI	I^2C, SPI	AC'97, I^2S, SPI, SMBus	I^2C, SPI, SSP
PCI Controller	33/66MHz	33/66MHz	2 x 33/66MHz	2 x 33/66MHz	33/66MHz	33/66MHz
USB Controller	Host/device 2.0 †	Host/device 2.0 †	Host/device 2.0 Host 2.0	—	Host/device 1.1	Host 2.0 † Device 1.1
Utopia-2	2	2	—	—	—	1
Ethernet MACs	8 x 10/100 2 x Gigabit	6 x 10/100 2 x Gigabit	2 x Gigabit	2 x 10/100 2 x Gigabit	2 x 10/100	6 x 10/100
UARTs	Up to 10	Up to 10	2	2	3	2
Security Engine‡	Yes	Yes	Yes	Yes	Yes	Yes

Table 2. This comparison table matches Freescale's new PowerQUICC II Pro MPC8360E and MPC8358E against two PowerQUICC chips announced last year and some likely competitors from AMD and Intel. All are fast, highly integrated 32-bit processors for communications and networking. Note that CPU clock frequency appears to have a greater influence on pricing than I/O capability does, even though most customers will probably base their choice on feeds, not speeds. *Intel's power estimates are for maximum consumption, not typical consumption. †These USB 2.0 controllers support Low-Speed and Full-Speed data rates but not the Hi-Speed rate. ‡Security engines are integrated only in PowerQUICC chips with product names bearing the "E" suffix; the same devices are available without security.

from year to year. Freescale is a particularly strong competitor, because the PowerQUICC family is broad enough to offer good choices for many customers, and because Freescale refreshes the product line so frequently. Despite this rapid evolution, Freescale has managed to preserve a great degree of compatibility across the family for 10 years.

Table 2 compares the new PowerQUICC II Pro MPC8360E and MPC8358E with two other recent processors from Freescale—the PowerQUICC II Pro MPC8349E and PowerQUICC III MPC8541E—and two worthy competitors from AMD and Intel, the Alchemy Au1550 and the IXP465. Of course, many more comparisons are possible, and any table of this kind could be almost arbitrarily large. For instance, the MPC8358E competes strongly with the IXP465, whereas the MPC8360E competes more directly with Intel's IXP2325 (not listed in the table). All these chips are equipped with fast 32-bit CPU cores, DDR memory interfaces, MMUs, multiple Ethernet controllers, PCI controllers, and security engines. Some distinguishing features are Gigabit Ethernet controllers (not found in these AMD and Intel chips), USB (missing from the PowerQUICC III MPC8541E), and Utopia-2 (absent from two Freescale chips in this table and from AMD's Alchemy Au1550).

One interesting observation is that customers will pay more money for chips with faster CPUs. If that seems too obvious, consider that in this product category, I/O capability is more important than clock speed—these are communications processors, not PC processors. If a particular system design absolutely needs Gigabit Ethernet, the designer probably won't settle for a chip with Fast Ethernet, even if the Fast Ethernet chip has a faster CPU.

For example, customers could pay as much as $62 for an Intel IXP465 that runs at 667MHz but is limited to Fast Ethernet; or they could pay as little as $34 for a Freescale MPC8358E that runs at only 266MHz but supports two Gigabit Ethernet ports and as many Fast Ethernet ports as the IXP465 does. Lower yields for higher-frequency parts classically drive these price differences, of course. Nevertheless, it's interesting that value pricing hasn't narrowed the gap. *Microprocessor Report* believes the real value of these processors is their degree of I/O integration, which can reduce or eliminate the need for auxiliary chips in a system design.

Price & Availability

Freescale plans to begin sampling the PowerQUICC II Pro MPC8360E, MPC8360, MPC8358E, and MPC8358 in 3Q05. Production quantities are scheduled to be available in 1Q06. Development tools for programming the QUICC Engine auxiliary processors will ship in 2006. When purchased in 10,000-unit quantities, the MPC8360E and MPC8360 will start at about $44 for 266MHz parts; the MPC8358E and MPC8358 will start at about $34 for 266MHz parts. Freescale hasn't announced pricing for the faster parts up to 667MHz. For more information, see *www.freescale.com*.

On the other hand, if a communications chip has I/O capabilities a particular system design doesn't need, the overstuffed chip will probably consume more power and occupy more board space than a different chip having just the right amount of integration. In that case, a less integrated chip will look more attractive. Reconsider the previous example in this light: Intel estimates its IXP465 will consume a *maximum* of 3.4W at its highest clock speed of 667MHz, which is less power than Freescale estimates an MPC8360E will *typically* consume at the same frequency. If power matters, and the system design doesn't need Gigabit Ethernet, the IXP465 has an edge—although Freescale's PowerQUICC family is so heavily populated, finding a closer match will almost certainly be possible.

The competition in this market is so finely sliced that minor differences of integration, speed, and power can easily be outweighed by other factors—such as customer inertia. If a customer's previous system design used a PowerQUICC, odds are the next design will also use one. Design experience and software compatibility are powerful gravitational forces. That's why PowerQUICC's 10-year anniversary is significant. Corporate names may change, and executives may come and go, but the PowerQUICC family offers the rare comfort of continuity in a rapidly changing industry.