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ARC's Preconfigured Cores

Six "New" Processors Are Derivatives of ARC 600 and ARC 700

By Tom R. Halfhill {3/14/05-02}

ARC International has introduced six embedded-processor cores based on its configurable ARC 600 and ARC 700 families. The "new" 32-bit synthesizable processors are actually preconfigured cores, optimized for embedded applications in the low-power and high-performance realms. Although chip designers can further customize the cores for specific applications, the ready-made configurations are intended to accelerate design projects and allow easier comparisons with competing processors.

The six preconfigured cores are the ARC 605, 610D, 625D, 710D, 725D, and 750D. All but one (the 605) have DSP extensions, because ARC considers signal processing essential for hard real-time control systems and other target applications. The 6xx-series cores are based on the low-power ARC 600, which ARC announced in late 2003. (See *MPR 12/15/03-01*, "ARC Alters Trajectory.") The 7xx-series cores are based on the more powerful ARC 700, which ARC announced in early 2004. (See *MPR 3/8/04-01*, "ARC 700 Aims Higher.")

ARC considers the ARC 600 its low-power core and the ARC 700 its high-performance product, but these processors defy easy pigeonholing. Either core is configurable for low power or high performance. One of their predecessors, the ARCtangent-A4, handily beat a 1.0GHz PowerPC processor in the EEMBC consumer benchmark suite in 2002, thanks to custom extensions. The ARC 600 and 700 are significantly faster than the ARCtangent-A4 and ARCtangent-A5, making them formidable competitors against the 32-bit processor cores from ARM, MIPS Technologies, and Tensilica.

All the new ARC 6xx- and 7xx-series cores are available now as licensable intellectual property (IP), and some are already in the hands of customers. ARC doesn't disclose upfront licensing fees or royalties—which are negotiable, of course—but shoppers should note that the company is still climbing toward profitability and is strongly motivated to snatch business away from competitors.

ARC 6xx Family Targets Low Power

ARC advertises the ARC 605 as the world's smallest, lowest-power 32-bit processor core, but Tensilica disputes that claim. When fabricated in a 0.13-micron CMOS process and optimized for speed, the ARC 605 occupies 0.36mm^2 of silicon and consumes 0.06mW per megahertz—15mW at its maximum worst-case clock frequency of 250MHz. When optimized for die area in the same process, it occupies 0.31mm^2 of silicon and consumes only about 8mW at 133MHz. Those are impressive measurements.

However, Tensilica says a minimum configuration of its Xtensa LX processor can undercut the ARC 605. When fabricated in a 0.13-micron process, the base-configuration Xtensa LX (approximately 19,000–25,000 gates, depending on the synthesis script) occupies only about 0.2mm^2 of silicon and consumes 0.038mW per megahertz—or a tad less than 15mW at its maximum worst-case clock frequency of 390MHz. That's slightly better than the ARC 605, especially in clock speed. Of course, the ARC 605 isn't quite a minimum configuration of the ARC 600 core. An ARC 600 base configuration (about 27,000 gates) will consume about 0.04mW per megahertz, essentially matching the power consumption of Xtensa LX though still falling short of Tensilica's maximum clock speed (390MHz vs. 290MHz).

Reality check: this comparison is like asking how many angels would fit on the head of a pin, an unanswerable question that vexed medieval philosophers. Calculating how many ARC or Tensilica processors would fit on the head of a pin is mathematically possible, but it's not much more relevant. The fact is, both companies have freakishly small 32-bit processor cores, and few customers will implement the base configurations.

Although the ARC 605 is thrifty, it's not impoverished. It has a five-stage pipeline and static branch prediction, and it is fully compatible with the versatile ARCompact instruction-set architecture (ISA). To reduce code size by as much as 40%, ARCompact adds a subset of 16-bit instructions to the regular set of 32-bit instructions, much like ARM's Thumb, the MIPS16e extensions, and Tensilica's subset of 16-bit instructions.

Because ARC is aiming the 605 primarily at motor-control and other hard real-time applications, it is a cacheless core. Programmers need not worry about the nondeterministic behaviors of conventional instruction and data caches. Instead, the 605 offers the option of integrating closely coupled memory (CCM) with the processor. These synthesized SRAM arrays are divided into instruction memory (which can range in size from 1KB to 512KB) and data memory (2KB–16KB). The processor core can access CCM (read or write) in a single clock cycle.

ARC 605 Is an ARM Wrestler

It's apparent that the ARC 605 is aimed at the world's best-selling 32-bit embedded-processor core, the ARM7TDMI. Available for many years in both hard and soft versions, the ARM7TDMI and ARM7TDMI-S are the embedded industry's 32-bit workhorses. They offer chip designers a combination of economy and processing power that's hard to beat, and they are supported by a wealth of hardware- and software-development tools. In addition, numerous 32-bit microcontrollers based on the ARM7TDMI are available as standard parts, often eliminating the need for a costly chip-design project.

Nevertheless, the ARC 605 is an attractive alternative. Like the ARM7TDMI-S, the ARC 605 is a cacheless, synthesizable 32-bit processor core with a subset of 16-bit instructions for greater code density. Thanks to a deeper pipeline (five stages vs. three), however, the 605 can reach 250MHz (worst-case) in a 0.13-micron CMOS process, nearly twice the maximum clock speed of the ARM7TDMI-S (133MHz). Their die areas in such a process will be roughly the same, but the ARC 605 will consume only about half as much power (0.06mW/MHz vs. 0.11mW/MHz), thanks to more-extensive clock gating and other power-management improvements. And the ARC processor gives up nothing in ease of system-on-chip (SoC) integration, because it has a configurable system interface compatible with two industry-standard buses: ARM's own AMBA AHB and the Basic Virtual Component Interface (BVCI).

Adventurous SoC designers can wring much more performance from the ARC 605 than its clock speed implies. Although it ships as a preconfigured core, it's still highly customizable in numerous ways that ARM processors are not. Using ARC's improved processor-configuration tool *(ARChitect2),* designers can add application-specific instructions, registers, conditional execution codes, I/O interfaces, and other features to the ARC 605. It's even configurable as a big- or little-endian processor.

The main drawback of the ARC 605 is that it's Brand X. By now, engineers at many companies can design an ARM7TDMI-based chip with their eyes closed. And their programmers can go home early, because the finished silicon will be compatible with existing software. The ARC 605 and its siblings will be more compelling to customers less tightly embraced by ARM—or to customers needing the higher performance that is possible only with custom extensions.

ARC's Extensions Boost Signal Processing

The other two ARC 6xx-series preconfigured cores—the 610D and 625D—have the same basic features as the 605, plus ARC's DSP extensions. The 625D also offers the option of conventional instruction and data caches (up to 32KB each) in addition to CCMs. These two cores can deliver signal-processing performance similar to that of a dedicated DSP core, yet they're also suitable for low-power general-purpose processing. Their other big advantage is a unified tool chain for software development, because the DSP instructions share the instruction stream with regular instructions. No special DSP compiler or assembler is required.

ARC's DSP extensions are a little confusing, because they come in two sets. In the past, ARC offered all these extensions as a single package, but they are now separate, providing more flexibility for chip designers who prefer to configure their own cores. All the preconfigured ARC 6xx and 7xx cores with DSP extensions—indicated by the "D" postfix, as in 610D—include the first set of extensions by default; the second set is optional.

The first set of DSP extensions includes 16/32-bit multiply (MUL) and multiply-accumulate (MAC) instructions; dedicated DSP registers and pipelines allowing those MULs and MACs to execute in parallel with each other and with regular ALU instructions; saturating-arithmetic instructions; and support for zero-overhead looping, which eliminates the branch-delay penalty in tight program loops. Normally, customers can add these DSP extensions with a few mouse clicks in *ARChitect2* when manually configuring an ARC core, but ARC bundles them by default with all the preconfigured 6xxD and 7xxD cores.

For customers needing even more signal-processing capability, the ARC XY Advanced DSP extensions are optional for all 6xxD and 7xxD cores. In addition to the DSP features mentioned above, the XY Advanced DSP extensions provide dedicated X and Y memories for the data operands of DSP instructions; a dedicated DMA engine for

those memories; special memory-addressing modes; and a library of optimized DSP routines. The library accelerates fast-Fourier transforms (FFT), Viterbi error correction, cyclic redundancy checks (CRC), 24- × 24-bit MACs, and other functions. Figure 1 shows how the two sets of DSP extensions and library routines can accelerate a 256-point FFT on an ARC processor.

XY Memories Have Flexible Addressing

Note that ARC's XY memories are independent of the CCMs that store other instructions and data, and are also independent of the optional instruction and data caches for the ARC 625D, 725D, and 750D. XY memories are dedicated to DSP data and closely coupled to the processor core. The processor can fetch two source operands in a single clock cycle while storing results from a previous DSP operation. Thanks to a dedicated DMA engine, these data moves don't impede the main instruction pipeline.

ARC 6xx-family cores support one or two banks of XY memory, single- or dual-ported, configurable with 1KB to 32KB per bank. (ARC 7xx-family cores support only one bank, dual-ported, with 8KB to 64KB.) Special addressing modes allow programmers to access the XY memories, using addresses with variable offsets, modulo addressing, or bit-reverse addressing. Some instructions increment the memory addresses automatically after execution. Dedicated address generators offload all address calculations from the processor core.

Overall, ARC's DSP extensions surpass those available for 32-bit synthesizable processor cores from ARM and MIPS. ARM's DSP extensions are mainly limited to 16-bit fixed-point math, and they don't support zero-overhead loops, XY memory, or the flexible memory-addressing modes that ARC offers. ARM does offer a more powerful DSP option—the OptimoDE data engine—but it's a separate processor core that significantly inflates the gate count and has a different instruction set and tool chain. (See *MPR 6/7/04-01*, "ARM's Configurable OptimoDE.") MIPS introduced its own DSP application-specific extensions (ASE) only a few months ago at Fall Processor Forum 2004, but they too lack support for zero-overhead loops, XY memory, and fancy addressing modes. (See *MPR 11/1/04-02*, "MIPS Takes Aim at Low-Cost DSP.")

To do better than ARC's DSP extensions without turning to a dedicated DSP core, the only alternative is Tensilica's Vectra LX engine. Introduced last year with the Xtensa LX processor, Vectra LX uses 64-bit instruction words with three issue slots for ALU, MAC, and load/store operations. In all, it supports about 200 instructions for 16-bit fixed-point DSP. When Berkeley Design Technology Inc. (BDTI) benchmarked an Xtensa LX processor with a Vectra LX engine last year, the combination outperformed every other licensable DSP or CPU core BDTI ever tested. (See the sidebar, "How Tensilica Busted the Benchmarks" in *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.")

However, the combination of Xtensa LX and Vectra LX will almost certainly consume more power and silicon than a DSP-enabled ARC 6xx core, which is downright miserly in both regards. Furthermore, ARC's DSP extensions have better support for 32-bit math than Vectra LX does. If customers don't need the power of Vectra LX, Tensilica offers lighter-duty DSP extensions that can perform 16-bit MACs and 16/32-bit multiplies without requiring as many gates as Vectra LX does. These DSP extensions are optional in Tensilica's processor-configuration tool.

ARC 7xx Cores Deliver Greater Performance

If the lowest possible power consumption isn't paramount, ARC's preconfigured 7xx-family cores deliver significantly better performance than the 6xx cores do without busting the power budget. The ARC 710D, 725D, and 750D are based on ARC's latest processor core, and all have the standard DSP extensions; the XY Advanced DSP extensions are optional. The distinguishing features among these cores are caches and memory management.

The ARC 710D is the economy model. Nevertheless, like all 7xx-based cores, it has dynamic branch prediction and a seven-stage pipeline (vs. five stages in the ARC 6xx family), so it can reach higher clock frequencies (up to 405MHz in a 0.13-micron CMOS process, worst-case) while avoiding those pesky pipeline bubbles. Although the 710D is more power-hungry than a 6xx core, it's still a low-power processor by most standards, requiring only 0.11mW per megahertz, excluding memories (44.5mW at its maximum clock rate of 405MHz). The ARC 710D is intended for hard real-time systems, so it eschews caches in favor of CCMs, which can range in size from 8KB to 256KB for instructions and from 8KB to 512KB for data.

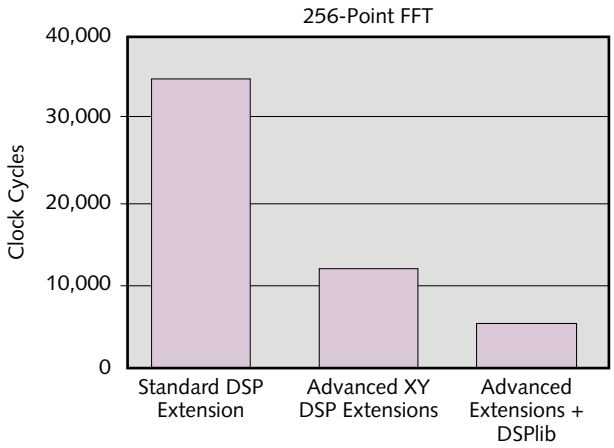

Figure 1. ARC's DSP extensions can dramatically improve signal-processing performance. This graph shows the number of clock cycles required to execute a 256-point FFT on an ARC 6xx or 7xx processor core, using the standard DSP extensions, the advanced DSP extensions with XY memories, and the advanced DSP extensions with ARC's DSPlib signal-processing library.

Feature	ARC 605	ARC 610D	ARC 625D	ARC 710D	ARC 725D	ARC 750D	ARM ARM946E-S	MIPS MIPS32-4KE	Tensilica Xtensa LX
General Features									
Architecture	ARC 600	ARC 600	ARC 600	ARC 700	ARC 700	ARC 700	ARMv5TE	MIPS32	Xtensa
Arch. Width	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
Instr Lengths	16/32 bits	16/32 bits	16/32 bits	16/32 bits	16/32 bits	16/32 bits	16/32 bits	16/32 bits	16/24 bits*
Pipeline	5 stages	5 stages	5 stages	7 stages	7 stages	7 stages	5 stages	5 stages	5–7 stages
Branch Predict	Static	Static	Static	Dynamic	Dynamic	Dynamic	—	—	—
Configurability	High	High	High	High	High	High	Low	Medium	High
L1 Cache (I/D)	— —	— —	0K–32K 0K–32K	— —	8K–64K 8K–64K	8K–64K 8K–64K	0–1MB 0–1MB	0–64K 0–64K	0K–32K 0K–32K
Closely Coupled Memory (I/D)	1K–512K 2K–16K	1K–512K 2K–16K	1K–512K 2K–16K	8K–256K 8K–512K	8K–256K 8K–512K	8K–256K 8K–512K	0–1MB 0–1MB	0–1MB Scratchpad	0K–256K 0K–256K
MMU	—	—	—	—	—	Yes	MPU only	Yes	—
DMA Controller	—	X/Y only	X/Y only	X/Y only	X/Y only	X/Y only	—	—	Yes
FPU	—	—	—	—	—	—	—	—	Optional
Max Freq †	250MHz	260MHz	240MHz	405MHz	400MHz	400MHz	210MHz	233MHz	390MHz
Die Area**	0.31mm^2	0.64mm^2	0.71mm^2	0.72mm^2	0.96mm^2	1.12mm^2	1.96mm^2	1–1.7mm^2	0.2mm^2
Power (/ MHz)†	0.06mW	0.07mW	0.08mW	0.11mW	0.12mW	0.13mW	0.30mW	0.25mW	0.04mW
Availability	Now	Now	Now	Now	Now	Now	Now	Now	Now
DSP Features									
DSP Extensions	—	Yes	Yes	Yes	Yes	Yes	Yes	Optional	Optional
16/32-Bit MAC	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Optional
Saturating Math	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Optional
Zero-Overhead Loops	—	Yes	Yes	Yes	Yes	Yes	—	—	Optional
X/Y Memory	— — — —	Optional 1–2 ports 1–2 banks 1K–64K	Optional 1–2 ports 1–2 banks 1K–64K	Optional 2 ports 1 bank 8K–64K	Optional 2 ports 1 bank 8K–64K	Optional 2 ports 1 bank 8K–64K	— — — —	— — — —	Optional
DSP Library	—	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional

Table 1. All these 32-bit embedded-processor cores are synthesizable and available as licensable IP. The preconfigured ARC cores are derivatives of the ARC 600 and ARC 700 processors. Most of ARC's preconfigured cores include DSP extensions, and one (the 750D) has an MMU. Even the higher-performance ARC 7xx cores require very little silicon and power; the ARC 6xx cores are extremely economical in both regards. For signal-processing tasks, Tensilica's Xtensa LX offers the toughest competition for ARC. *Shorter instructions are possible with Tensilica's FLIX extensions. **0.13-micron CMOS process, excluding memories. †0.13-micron process, worst-case.

Designers who want caches can step up to the ARC 725D, the next higher model. It supports instruction and data caches, from 8KB to 64KB each. It also supports CCMs that are the same size as the 710D's. The cache-control logic makes the ARC 725D slightly larger (0.96mm^2 vs. 0.72mm^2) and more power hungry (0.12mW/MHz vs. 0.11mW/MHz) than the 710D, but it's still a trim processor.

The final rung on this product ladder is the ARC 750D, which has all the features of the 725D plus a memory-management unit (MMU). This crucial feature allows the 750D to support a virtual-memory subsystem and run more-sophisticated operating systems, such as Linux. (Specifically, the 750D can run Embedded Linux and µClinux, as well as some popular real-time operating systems, such as MQX, ThreadX, and µITRON.) Although the MMU inflates the 750D to 1.12mm^2 and raises power consumption to 0.13mW per megahertz, that's still only 52mW at its maximum clock frequency of 400MHz (0.13-micron CMOS, worst-case, excluding memories). By any measure, the ARC 750D compares very favorably with other processors in its class.

Table 1 tells the story. It compares all the preconfigured ARC 6xx and 7xx cores with similar 32-bit synthesizable processors from ARC's chief competitors: ARM, MIPS, and Tensilica. Choosing representative processors from ARM and MIPS is difficult, because they have so many products, but we picked the ARM946E-S and MIPS32-4KE because they have DSP extensions, CCMs, and other features in common with the ARC cores. However, the ARM and MIPS cores tend to require more silicon and dissipate more power than similar ARC cores when fabricated in the same process, and they fall short of ARC's highest clock speeds. Tensilica's Xtensa LX is stiffer competition, especially when augmented with its optional Vectra LX engine. Xtensa LX is the only processor in this group for which there are published EEMBC and BDTI performance benchmarks.

New Cores Don't Alter ARC's Strategy

Don't jump to the conclusion that ARC is retreating from configurable processors by introducing preconfigured cores. This is a sideline to ARC's main strategy, not a wholly new strategy. In fact, ARC first explored this territory in 2001 by introducing some variations of the ARC3 processor that were preconfigured for synthesis in Xilinx FPGAs.

ARC is simply acknowledging reality. Configurable processors may be the best thing since sliced silicon, but not everyone is comfortable with the idea of becoming a CPU

ARC Wins Key U.S. Patent

ARC International was issued an important patent on configurable-processor technology by the U.S. Patent and Trademark Office (USPTO) on March 1. Entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design" (U.S. 6,862,563), the patent shows how to customize an integrated-circuit design by using automated tools that modify the synthesizable model. Although the patent applies broadly to ICs, it focuses on microprocessors, and more particularly on modifying the instruction set and other architectural features of a microprocessor.

ARC filed the '563 patent on October 14, 1999, so the application was under review by the patent office for more than five years. The patent lists three inventors: James Hakewill, Mohammed Khan, and Edward Plowman. Hakewill is the only one still employed at ARC. He is currently an ARC Fellow who relocated from ARC's office in Elstree, England, to Silicon Valley a few years ago. Khan is the principal engineer at Atollic Ltd., a security startup in the U.K. Plowman is currently at ARM, a major ARC competitor.

The '563 patent is very detailed—90 pages long with 44 pages of figures, mostly flowcharts, showing how a user-driven configuration process works. Among other things, the patent describes a software tool that collects a user's inputs and automatically generates scripts for modifying the hardware description language (HDL) of a synthesizable microprocessor core. Essentially, the patent describes *ARChitect*, the company's graphical processor-configuration tool. The current version of *ARChitect* resembles a visual software-development tool with numerous point-and-click options in menus and property sheets. Users can modify the processor's instruction set, register file, condition codes, caches, buses, and other features. The output includes a synthesizable Verilog model of the processor, synthesis scripts, test code for verification, and software simulators.

Microprocessor Report is still analyzing the '563 patent in the context of other patents, but it appears to be a well-written description of fundamental configurable-processor technology. Although it's not ARC's first patent, it protects broader aspects of the company's intellectual property than previous patents do. One question that comes to mind, then, is whether other vendors of configurable processors—mainly, MIPS Technologies and Tensilica—have anything to worry about.

ARC CEO Carl Schlachte deftly dodged our questions about using the '563 patent as an offensive weapon. Instead, he characterized it as important protection for ARC's intellectual property and said it will provide additional assurance to ARC's licensees. Schlachte says some licensees have already reacted positively to news about the patent, and that a few prospective customers have expressed stronger interest in becoming licensees.

Tensilica has patents in this field as well. On November 5, 2002, the USPTO issued patents 6,477,683 and 6,477,697 to Tensilica, which had filed the applications on February 5, 1999 and May 28, 1999, respectively. (See *MPR 12/9/02-01*, "Tensilica Patents Raise Eyebrows.") However, in response to an anonymous challenge, the USPTO reexamined the '683 patent and in April 2004 rejected all 104 claims. (See *MPR 6/2/03-03*, "Tensilica Patent Challenged.") After reexamination, the USPTO ruled that Tensilica's claims in the '683 patent were either invalid over the prior art or did not represent a patentable advance. Tensilica has appealed the ruling. Although ARC filed its '563 patent on October 14, 1999, several months after Tensilica's patent applications, the priority (effective) date of the '563 patent is a year earlier, because ARC filed a provisional application on October 14, 1998.

Neither ARC nor Tensilica has a history of aggressive litigation. We believe ARC's latest patent won't alter the balance of power between the companies. However, the growing patent portfolios of ARC and Tensilica could be worrisome for other companies that introduced configurable processors later (such as MIPS) or that may introduce such processors in the future.

architect, no matter how simple the configuration tools are. Some customers license ARC's processor cores for their out-of-the-box qualities and never get around to adding custom extensions. A few customers even *remove* features from the base configuration to make the cores still smaller and more power efficient. Either way, it doesn't matter much to ARC after the customer signs the license. However, ARC does worry about losing business when potential customers are confused by the myriad configuration options or don't understand that custom extensions aren't always necessary.

Hence the new line of preconfigured cores. It might seem as contradictory as selling a box of Legos preassembled as an airplane—why not just sell a toy airplane? But we believe it's a wise strategy. Preconfigured cores should reduce the confusion for some customers and give ARC the opportunity to compare its processors head-to-head with competing products, especially the popular cores from industry-leader ARM. ARC knows its processors will fare well in these comparisons. ARC also knows it can offer more-favorable licensing terms than ARM will. All things considered, some customers won't care that ARC is Brand X.

At the same time, ARC isn't throwing away the advantages of configurability. ARC is still selling a box of Legos, even if they are preassembled. Some new licensees will discover that the preconfigured cores are still configurable, and they may work up the courage to customize them further.

Price & Availability

The ARC 605, 610D, 625D, 710D, 725D, and 750D processor cores are available now as synthesizable Verilog models. They include ARC's hardware- and software-development tools and are portable to virtually any fabrication process. Licensing fees, royalties, and terms are private and negotiable. For more information, see *www.arc.com*.

It may not happen during the first design project, but as the engineers gain experience with the processors, they will grow more comfortable with the idea. Preconfigured cores allow ARC to stick its foot in the door.

It might seem that ARC's next logical step is to offer prehardened cores. However, that would definitely move away from the configurability and process portability that have always been cornerstones of ARC's strategy. If any of ARC's preconfigured cores become wildly popular, a prehardened version might make sense, but only as a sideline to ARC's primary strategy.

Another scenario would be to unleash a vast catalog of preconfigured cores. ARC could use its configuration tools and extensions library to generate a virtually infinite variety of processors, outnumbering even the Hydra-like offerings from ARM. It's not as if ARC's preconfigured cores would be occupying space in a warehouse—ARC could create them practically on demand. However, this strategy might confuse potential customers in a worse way than the processor-configuration options. ARC's catalog could grow so large it would resemble Amazon.com—or, come to think of it, the ARM catalog.

We believe ARC will find a happy medium. A comprehensible number of preconfigured cores is a useful adjunct to ARC's main strength: user-configurable processors. The derivative cores introduced thus far impose relatively few burdens on ARC's downsized engineering staff while giving the marketing department a new way to sell the company's best products. We believe that, over all, ARC has come up with a creative tactic to leverage existing resources and carry the company further toward its goal of profitability.