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MULTICORE CHIPS RULE IN 2004

High-Performance Embedded Processors Lead CPU Evolution

By Tom R. Halfhill {1/31/05-02}

PC processors boast the highest clock speeds. Server processors have the fattest caches. But unsung embedded processors are at the forefront of microprocessor evolution. As we noted last year, some of the architectural advances appearing first or most extensively in embedded processors are massively parallel processor arrays, on-chip interconnect fabrics, reconfigurable logic, DSP extensions, extendable instruction sets, and hardware-assisted simultaneous multitasking. In 2004, high-performance embedded processors also set the pace for multicore designs.

While the PC market is agog at dual-core 64-bit processors, the embedded market already takes such chips for granted and will deliver processors with four, eight, and sixteen 64-bit cores this year. The rising demands of telecommunications and network processing continue to drive aggressive innovation. Only the need for power efficiency restrains embedded chips from matching the high clock frequencies of PC processors and the bloated transistor budgets of the biggest server processors.

Our year-end review of high-performance embedded processors finds that innovation in this market continued to accelerate in 2004. Looking forward, we expect most chip vendors will be preoccupied delivering the ambitious processors announced last year. However, we also expect some exciting new announcements in 2005, including the public debut of at least two fabless semiconductor companies now working in stealth mode.

A Look Back—and Forward

Early in 2004, newcomer ClearSpeed Technology successfully demonstrated scientific software running on evaluation samples of its CS301 floating-point coprocessor, which the company unveiled at Microprocessor Forum 2003. The CS301 is a massively parallel chip with 64 processing elements, capable of executing 25.6 billion floating-point operations per second (GFLOPS) while consuming less than 2W. Such high performance at such low power might seem impossible, but ClearSpeed achieved its goals. (See *MPR 1/12/04-02*, "ClearSpeed Hits Design Targets.") Later in 2004, ClearSpeed announced a more powerful chip with 96 processing elements, the CSX600. Startups like ClearSpeed prove that innovation doesn't emanate from only the largest, richest companies.

Another startup, Stretch, announced an impressive family of processors with reconfigurable logic. Stretch's S5000 family is based on a Tensilica Xtensa processor core, which implies more emphasis on low power than on high performance. However, the integration of field-programmable logic potentially pushes these chips into the high-performance realm. Customers can create their own application-specific extensions to the instruction-set architecture (ISA), which can boost performance by an order of magnitude or more. A simulated 300MHz Stretch S5610 processor (with 100MHz reconfigurable logic) scored an amazing 877 TeleMarks in EEMBC's telecommunications benchmark suite—good enough to beat Intrinsity's 2.0GHz FastMath. Now sampling, the Stretch **S5610** deserves its nomination for an *MPR* Analysts' Choice Award in the High-Performance

Embedded Processor category, despite its dual identity as a low-power chip.

Although ISA extensions are Tensilica's bread and butter, the normal Xtensa design flow requires customers to spin their own silicon after extending the synthesizable core. Stretch provides an alternative by integrating reconfigurable logic with a preconfigured Xtensa core on a standard part, so customers can add ISA extensions to an off-the-shelf chip. Advantages: much faster time to market, much lower nonrecurring engineering (NRE) costs, and less development risk. Disadvantages: ISA extensions are more limited, and S5000 chips are more expensive than Xtensa-based SoCs in large volumes. (See *MPR 4/26/04-01*, "Stretching Performance.") For some expert insight into the pros and cons of reconfigurable logic, see this pair of opposing commentaries: *MPR 5/3/04-01*, "Microprocessor Sunset," and *MPR 5/10/04-01*, "Reconfigurable 'Illogic.'"

Security was a hot topic in 2004 and promises to be even bigger in 2005, so it's no surprise that many embedded-processor vendors are adding chip-level security features. VIA's Centaur Division, which makes x86-compatible chips for low-priced PCs and embedded systems, added two random-number generators and new instructions for accelerating encryption algorithms to the Esther C5J processor. Although these features fall short of the full-fledged security engines found in a growing number of network and communications processors, VIA is breaking new ground in the x86 market. (See *MPR 5/18/04-03*, "VIA Embeds Its Security Strategy.")

In mid-2004, AMD introduced the Au1550, the first Alchemy-series network processor with an integrated security engine. AMD licensed the SafeXcel engine from SafeNet, an intellectual-property provider. The engine supports Internet Protocol security (IPsec) and the Secure Sockets Layer (SSL) protocol for virtual private networks. As with other Alchemy chips, the MIPS32-based Au1550 integrates a variety of networking features, such as dual Ethernet controllers, a PCI controller, and USB host/device controllers. Overall, the Au1550 compares well with similar processors from Freescale and Intel. (See *MPR 4/5/04-01*, "Alchemy Adds Security Engine.")

PowerQuicc Strengthens Security

Not to be outdone, Freescale beefed up the security engines in its new PowerQuicc II Pro family. Three chips in the six-member Pro series have Freescale's SEC 2.0 security engine, a major improvement over the SEC 1.0 engine in some earlier PowerQuicc chips. SEC 2.0 includes a true random-number generator and five function units: a public-key unit, DES unit, AES unit, ARC4 unit, and message digest unit.

In addition to offering more security features, SEC 2.0 offloads more processing from the PowerPC core and consumes less bus bandwidth than SEC 1.0. Three other members of the Pro family are available without SEC 2.0, for customers preferring to use a proprietary security engine, software-based security, or no security at all. (See *MPR 5/10/04-02*, "Freescale Secures PowerQuicc.") Freescale has enjoyed considerable success with the PowerQuicc line since replacing the 68K-based Quicc processors with PowerPC-based chips in 1993, so additional improvements in 2005 are a sure bet.

Indeed, the PowerPC architecture offered stiffer competition across the board in 2004, a trend certain to continue in 2005. MIPS-compatible processor cores remain extremely popular in high-performance embedded processors, especially in chips for telecommunications and networking applications. However, Freescale's PowerQuicc chips are multiplying like Wallace-tree rabbits, and IBM Microelectronics is taking significant steps toward licensing PowerPC more widely. For now, PowerPC is handicapped by a lack of synthesizable cores compatible with popular IC processes at independent foundries, but things are changing.

In one interesting development, Applied Micro Circuits Corp. (AMCC) became the third PowerPC supplier by acquiring a vast array of PowerPC chips, intellectual property, and development resources from IBM. (See the sidebar, "AMCC Strikes a Big Deal for PowerPC," in *MPR 4/26/04-02*, "IBM Loosens Up CPU Licensing.") In another move, IBM formed an independent consortium to help guide PowerPC's progress. (See *MPR 12/27/04-02*, "Bringing Power to the People.") We expect PowerPC to be an even stronger competitor in 2005.

ARM Bridges the Power-Performance Gap

ARM is generally considered the leading provider of low-power 32-bit processor cores, not high-performance processors. At Embedded Processor Forum 2004, however, ARM announced MPCore, an integrated package of licensable intellectual property that includes up to four ARM11v6 32-bit processor cores.

Essentially, MPCore is a drop-in solution for multicore embedded-processor designs. It eliminates some of the busywork of designing cache-coherency logic and distributed interrupt channels, and it requires only one ARM license. MPCore still supports low-power designs, because a multicore SoC can run at lower clock speeds than a single-core chip can while doing the same work. But an aggressive design that cranks up the clock frequency could use MPCore as the foundation for a high-performance embedded processor. (See *MPR 5/24/04-01*, "ARM Opens Up to SMP.")

Two MIPS licensees—NEC Electronics and Intrinsity—have pretty much dropped out of the race for high-performance, general-purpose embedded processors. NEC is refocusing on MIPS-based ASICs and ASSPs. Intrinsity is changing its business model altogether, deciding it is no longer viable as a fabless semiconductor company. Instead, Intrinsity is trying to make the transition to an intellectual-property provider by licensing the proprietary tools and technology for its high-performance Fast14 logic. (See *MPR 1/10/05-02*, "Intrinsity Takes Its IP on the Road.")

Toshiba's Efficient MIPS64 Core

Despite the changes at Intrinsity and NEC, the MIPS architecture isn't waning. On the contrary, MIPS licensees were extremely active in 2004. In midsummer, Toshiba introduced its TX99 family of MIPS64-compatible processors, which use the new 64-bit TX99/H4 core developed jointly with MIPS Technologies.

The TX99 is Toshiba's first superscalar MIPS64 core, and its deeper seven-stage pipeline can reach clock frequencies as high as 800MHz in the company's 90nm fabrication process. In fact, the Toshiba **TX9956CXBG** was the first chip in its class to reach production in 90nm, and it deserves a nomination for an *MPR* Analysts' Choice Award. Although a two-way superscalar core running at 800MHz isn't exactly bleeding-edge technology for 2004, Toshiba is optimizing the TX99 for favorable power-performance and cost-performance ratios, not the highest possible throughput. Our analysis found that TX99 processors excel at price-per-megahertz and megahertz-per-watt duels against competing chips. (See *MPR 7/26/04-02*, "Toshiba's New MIPS64 Family.")

At Fall Processor Forum, MIPS licensees presented an avalanche of new high-performance embedded processors, and PowerPC vendors were busy, too. Broadcom, Cavium, and PMC-Sierra announced a total of nine MIPS64-based chips—all multicore designs—while AMCC and Freescale announced three 32-bit PowerPC chips. Faraday Technology elbowed into this crowd with a configurable structured ASIC based on a new 32-bit ARMv4-compatible core, the FA626. Rarely have so many processors that will compete head-to-head in the marketplace appeared in a single session at one of our forums. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

Cavium raised a storm with its Octeon family of "network services processors"—a category created by Cavium. No other chips integrate as many processor cores or networking functions, so they're truly in a class by themselves. Octeon chips integrate two, four, eight, or sixteen MIPS64-compatible processor cores with additional logic optimized for L3–L7 packet routing, deep content filtering, and security. Cavium designed a new full-custom MIPS64 core especially for the Octeon family. For data-plane tasks, Octeon is hard to beat. Before announcing Octeon, Cavium was a respected but relatively minor vendor of security processors and I/O chips; Octeon makes the company a significant player in network processors. (See *MPR 10/5/04-01*, "Cavium Branches Out.")

Broadcom: Better Late Than Never

Critics sniped at Broadcom for announcing its dual-core BCM12xx and quad-core BCM14xx processors at FPF, because the "new" SiByte-family chips are makeovers of products Broadcom announced in 2002 but never delivered. However, we think Broadcom deserved the stage time, because the processors are still very competitive, even if they're shipping two years late.

Broadcom began sampling the dual- and quad-core chips in December, just in time for our award deadline, so we nominated the quad-core Broadcom **SiByte BCM1480** for an *MPR* Analysts' Choice Award. Most other high-performance embedded processors announced in 2004 aren't sampling yet and therefore aren't eligible for a 2004 award. Barring last-minute problems, Broadcom's quad-core BCM1455 and BCM1480 should begin production before the new dual-core processors from Freescale and PMC-Sierra appear.

PMC-Sierra's dual-core RM11200 is no slouch, either. It doesn't have as many processor cores as the biggest multicore chips from Broadcom and Cavium, but it will reach a higher clock frequency (1.8GHz). That's because the RM11200 will be PMC-Sierra's first chip fabricated in a 90nm process, and it introduces the new E11K MIPS64-compatible processor core. One of the most interesting features of the RM11200 is its Nexus on-chip crossbar bus, based on asynchronous-logic technology licensed from Fulcrum Microsystems. The Nexus crossbar connects the dual E11K processor cores with on-chip peripherals running at greatly different clock speeds, and it doesn't require the multitier buses found in other highly integrated chips. Although the RM11200 didn't sample in time to be eligible for a 2004 *MPR* Analysts' Choice Award, it will be a strong contender in 2005.

In the same FPF session, AMCC and Freescale rolled out their latest PowerPC-based designs, including AMCC's first new PowerPC processor and Freescale's first dual-core PowerPC. AMCC's PowerPC 440SPe I/O chip is actually a modification of IBM's PowerPC 440SP—AMCC inherited both the design project and design team in its $227 million deal with IBM. Essentially, the 440SPe adds PCI Express to the 440SP network-storage processor, a small but important upgrade.

Freescale announced the dual-core MPC8641D networking processor, along with a single-core version, the MPC8641. Both chips integrate the 32-bit e600 processor core with the on-chip peripherals and I/O interfaces of a PowerQuicc III MPC8548. It's not a radical design, but it's sensible, because it allows customers to replace two or three separate chips with a faster, software-compatible processor.

Structured ASIC Offers Design Flexibility

Faraday raised eyebrows in the same FPF session with a structured ASIC based on the full-custom FA626 ARMv4-compatible core. ARM rarely makes an appearance in networking processors, mainly because ARM cores are prized for low power consumption, not high throughput. Nevertheless, Faraday's NetComposer-II (NC-II) is an L4–L7 networking processor with three optional metal layers of programmable logic gates. Customers can add application-specific logic and up to 1.5Mb of SRAM before manufacturing, which offers the opportunity to create a highly optimized solution.

Structured ASICs make sense when standard parts can't do the job or don't provide enough differentiation, or when developing a full-custom ASIC would be too expensive. However, we think building the NC-II around a MIPS core

Best High-Performance Embedded Processor: Broadcom BCM1480

Our *MPR* Analysts' Choice Award for the **Best High-Performance Embedded Processor of 2004** goes to **Broadcom**'s quad-core **SiByte BCM1480**. Yes, we know it's a controversial choice. The BCM1480 (and its fraternal twin, the BCM1455) is basically a revised version of the BCM1400 that Broadcom announced at Microprocessor Forum 2002 and promised to ship in 2H03. If Broadcom meets its delivery date for the "new" BCM1480, it will ship in 3Q05, about two years late.

We are rewarding persistence and performance. It's obvious that Broadcom's original engineering schedule was overoptimistic. Nevertheless, the BCM1480 is still a very competitive product for 2005 and 2006. PMC-Sierra, Broadcom's closest competitor in this market, hasn't even announced a quad-core processor yet. The new dual-core RM11200 from PMC-Sierra looks impressive, but it didn't sample in time for our award deadline. Freescale didn't announce a dual-core PowerPC processor until Fall Processor Forum 2004, and that chip won't begin production until 2006.

Cavium is emerging as a major contender with its Octeon family, which integrates as many as 16 MIPS64 cores on a single chip, along with more networking logic and peripherals than are found in the Broadcom parts. However, Octeon chips weren't sampling by the end of 2004, so they aren't eligible for a 2004 award. Furthermore, software limitations could restrain performance with these radical multicore designs. Theoretically, the quad-core BCM1480 can execute as many instructions per second as a 16-core Octeon, because the BCM1480 has wider superscalar cores (four-way vs. two-way) and runs faster (1.2GHz vs. 600MHz). We suspect programmers and compilers will find it easier to utilize multiple cores than multiple pipelines, but only benchmark testing and real-world applications will tell the story.

The other nominees in this category are all good products. Stretch's S5610 is an innovative hybrid of an SoC with reconfigurable logic; Toshiba's TX9956CXBG is a power-efficient performer; and IBM's BlueGene/L processor is a creative approach to high performance. All things considered, however, we prefer the BCM1480 for this award.

By any measure, the BCM1480 is a formidable processor. It's based on the SiByte SB-1 full-custom MIPS64 core—still the only four-way superscalar MIPS64 core. The chip includes a 1MB L2 cache, DDR1/DDR2 DRAM controller, 64-bit 133MHz PCI-X, four Gigabit Ethernet controllers with configurable FIFO modes, four Gigabit Media-Independent Interfaces, and three I/O ports independently software-switchable between HyperTransport and SPI-4.2. Speed grades will range from 800MHz to 1.2GHz when the processor ships later this year. The nearly identical BCM1455 lacks HyperTransport and SPI-4.2. Even though it's tardy, we think the BCM1480 is a worthy award winner.

instead of ARM could have delivered even greater performance and made the processor compatible with more networking software and tools.

No year-end review of high-performance embedded processors would be complete without mentioning the extreme makeover of IBM's five-year-old PowerPC 440, a 32-bit embedded chip introduced at Microprocessor Forum 1999. Attendees at FPF's Cool Technology session listened raptly as IBM described how engineers modified the PowerPC 440 to build a custom processor for the company's new BlueGene/L supercomputer—the fastest computer in the world. IBM slapped down two 440 cores on a single chip, bolted on a dual-pipelined 64-bit FPU, defined a handful of new instructions, and pumped up the clock speed to 700MHz.

If that still doesn't sound like a world-class supercomputer processor, keep in mind that a fully configured BlueGene/L system has 65,536 of those chips, for a total of 131,072 processors. Theoretical peak performance is 360 trillion floating-point operations per second. (See *MPR 10/11/04-01*, "IBM Makes Designer Genes.") To link all those chips together, the supercomputer has an internal network running at 1.4GHz—making the BlueGene/L chip the first microprocessor we've seen that drives an I/O interface faster than the CPU core clock frequency.

The IBM **BlueGene/L** processor is unique and innovative, so it deserves a nomination for an *MPR* Analysts' Choice Award in the High-Performance Embedded Processor category. (A supercomputer destined for number crunching at a national laboratory isn't exactly a server, and it's definitely not a desktop or mobile PC, so we'll claim it as an embedded system. A *super* embedded system.) Although the BlueGene/L chips aren't for sale on the merchant market, they prove embedded processors don't have to be invisible workhorses in anonymous black boxes. ◇