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Best Processor Cores of 2004

Processor-IP Cores and Tools Grow More Versatile, Sophisticated

By Tom R. Halfhill {1/24/05-01}

Greater performance, architectural enhancements, and improved design tools marked the progress of intellectual-property (IP) embedded-processor cores in 2004. Although the number of companies competing in this tight market remained static, one company booted its CEO, hired a new executive management team, and changed its strategy (again). Another company announced a mind-numbing barrage of new products and spent nearly a billion dollars on a binge of acquisitions. And the biggest competitor announced plans to greatly expand its licensing strategy. It was not a boring year.

On the technology front, the general trends were toward greater versatility, multicore designs, better tools, and higher clock frequencies—without ignoring the importance of low power consumption. For a brief period, one synthesizable processor core held the world speed record in the EEMBC consumer benchmark suite. It was overtaken by a microprocessor chip at least an order of magnitude larger, more expensive, and more power hungry. Yet the most impressive feat we witnessed during 2004 was the introduction of a new design tool that automatically creates custom processor extensions by analyzing software written in ordinary C or C++. And near the end of the year, another company impressed us by announcing the first commercial 32-bit microprocessor core implemented in asynchronous logic.

Here is an alphabetical review of the leading processor-IP companies—ARC International, ARM, IBM Microelectronics, MIPS Technologies, and Tensilica—and the most important news they made in 2004. We also name the nominees and winner of our *Microprocessor Report* Analysts' Choice Award for Best IP-Core Processor of 2004.

ARC Hires New Crew, Changes Course

Historically, the management team at ARC is about as stable as a Britney Spears marriage. Since ARC went public in the fall of 2000, there have been four CEOs, and the company has frequently flushed vice presidents from its caches. In 2004, ARC changed CEOs once more, revamped its marketing/PR team, and embarked on a new strategy—again. With cautious optimism, we think ARC's new look is the best in years.

The new CEO is Carl Schlachte, a 20-year veteran of ARM, BOPS, Motorola, SandCraft, and Raza Microelectronics. His technical background and business experience with licensable IP at those companies will be invaluable at ARC. Even before Schlachte came onboard in April, the company was altering course. In a crucial move, ARC decided to concentrate on its core products—32-bit embedded-processor cores—and begin divesting itself of distracting product lines, such as USB peripheral cores, system software, and software-development tools for other CPU architectures. In July, ARC announced the sale of its peripheral IP to Transdimension. The new ARC is promoting itself as a platform-IP provider for vertical embedded applications. (See the sidebar, "New CEO Brings Varied Background to ARC," in *MPR 3/8/04-01*, "ARC 700 Aims Higher.")

To support its long-overdue change of direction, ARC introduced the new ARC 700 customizable processor core in 2004, only months after announcing the ARC 600 in late 2003.

The ARC 700 was ARC's first ground-up redesign in several years and a significant step forward for the company. Thanks in part to a deeper seven-stage pipeline, the ARC 700 can run 38% faster than the ARC 600 in the same fabrication process. It's one-third the size of an ARM11 processor core and requires less power. It also adds DSP instructions, dynamic branch prediction, wider cache interfaces, a single-cycle adder, a nonblocking load/store pipeline, out-of-order completion, and new support for multicore designs.

In addition, the ARC 700 is the company's first processor capable of running Linux and other sophisticated embedded operating systems, because it's the first ARC processor with a memory-management unit (MMU), translation lookaside buffer (TLB), precise exception model, and multiple privilege levels. (See *MPR 6/21/04-01*, "ARC 700 Secrets Revealed.") Clearly, the **ARC 700** is a big step forward for the company, and it deserves our nomination for an *MPR* Analysts' Choice Award.

ARC also upgraded its hardware- and software-development tools in 2004. The improved tools make it easier to customize ARC's configurable processors and to write optimized software for them. Although ARC's latest tools aren't quite as slick as Tensilica's, they are powerful, and they give SoC designers a degree of control over the processor architecture that was once the exclusive domain of CPU architects.

Finally, to put a fresh face on its new products, ARC brought in a new vice president of marketing and a corporate communications manager, both of whom hail from MIPS. They are working on an aggressive schedule of new-product introductions for the first half of this year.

No other processor-IP company made as many drastic changes in 2004—but then, no other company needed to make as many drastic changes. ARC has never returned a profit as a public company, so 2005 may be its last chance to make a turnaround. We think ARC has the ingredients to succeed.

ARM Goes On a Tear

Few companies were as busy in 2004 as ARM. The market-leading British firm introduced a flood of new products, launched its own developers' conference, and spent nearly a billion dollars acquiring other companies, vastly extending its reach. In 2005, ARM will probably slow down a little, if only to digest its acquisitions and fulfill its commitments to ship previously announced products.

During the first half of 2004, ARM expanded its highest-performance ARM11 family by delivering two new series of cores: the ARM1156 and ARM1176. So far, each series consists of two synthesizable 32-bit processor cores, distinguished mainly by their Thumb-1 or Thumb-2 instruction sets, integrated floating-point units, Java extensions, power-management features, and TrustZone security. With pipelines eight or nine stages deep, these fast processor cores can reach 550MHz in a 0.13-micron fabrication process. The new processors solidify ARM's hold on the market for high-performance, low-power soft cores. (See *MPR 1/5/04-01*, "ARM Expands ARM11 Family.") The best-equipped cores in these two series—the **ARM1156T2F-S** and the **ARM1176JZF-S**—deserve our nominations for *MPR* Analysts' Choice Awards in the Best IP-Core Processor category.

In February and March came one of the strangest incidents of 2004: ARM's wrestling match with Xilinx over Triscend, a small fabless semiconductor company based in Silicon Valley. Initially, ARM announced it had acquired Triscend, signaling its important strategic move into the microcontroller market. (See *MPR 2/17/04-02*, "ARM Grabs Triscend.") A few weeks later, however, ARM lost its grip on Triscend, which had secretly negotiated a better deal with Xilinx. (See *MPR 3/15/04-02*, "Xilinx Reconfigures Triscend.")

The sudden reversal of the Triscend acquisition stalled ARM's plans to pull the microcontroller market further toward 32-bit processing—but only for a moment. Soon afterward, microcontroller giant STMicroelectronics launched two new families of microcontrollers based on 32-bit ARM7 cores. ARM views the microcontroller market as fertile ground for future growth and will continue pursuing this strategy in 2005.

Four-Way SMP in a Wrapper

At Embedded Processor Forum 2004, ARM made big news by revealing MPCore, a package of IP that unites up to four ARM11 cores in a symmetric multiprocessor (SMP) configuration. Multicore system-on-chip (SoC) designs are becoming commonplace in embedded systems, and MPCore provides a relatively simple drop-in module of preconfigured multicore IP.

Although a four-way SMP design might seem to contradict ARM's traditional strategy of emphasizing low power, MPCore could reduce power consumption by allowing an SoC to run at a lower clock frequency than a single-core design delivering similar performance. For SoC architects, the preconfigured IP module (which requires only one license, even with four CPU cores) can simplify multicore design projects. However, as with all multicore designs, a successful implementation depends as much on the software as it does on the hardware. (See *MPR 5/24/04-01*, "ARM Opens Up to SMP.")

In another session at EPF 2004, ARM unveiled OptimoDE, a configurable DSP engine for ARM processors. (See *MPR 6/7/04-01*, "ARM's Configurable OptimoDE.") OptimoDE is based on a parallel-processing VLIW architecture acquired from Adelante Technologies in 2003. For now, OptimoDE is ARM's answer to the customizable CPU architectures from ARC, MIPS, and Tensilica. Instead of offering a customizable processor core, ARM is promoting OptimoDE as a configurable data engine for existing ARM cores. Essentially, OptimoDE is an ARM-sanctioned solution for adding programmable coprocessors to the AMBA buses of ARM-based SoCs. (Actually, designers can attach OptimoDE engines to the AMBA buses of *any* SoCs, even those using other processor cores.)

One drawback of OptimoDE is that it requires new tools for hardware configuration and software development. In contrast, the customizable processors from ARC, MIPS, and Tensilica have unified tool chains that let programmers mix DSP instructions with regular CPU instructions in the same datapath. The hardware-configuration tools for OptimoDE also look more daunting than those from ARC, MIPS, and Tensilica. We hope ARM will demonstrate the practicality and performance of OptimoDE by publishing EEMBC benchmark results comparable to those for competing processor cores.

ARM Snatches Artisan, Adds Cortex

As the summer of 2004 drew to a close, ARM surprised the industry by announcing a huge $913 million acquisition of Artisan Components, a leading provider of semiconductor IP. The Artisan deal came only a week after ARM said it would buy Axys Design Automation, a vendor of system-level design tools and models. (See *MPR 9/7/04-01*, "ARM Extends Its Reach.")

These bold moves confirmed ARM's imperial ambitions beyond embedded-processor cores. As SoC designs become larger and more complex, ARM is determined to capture more business by providing the peripheral cores, on-chip interconnects, memory, physical-library IP, and other components and tools required to build the chips. The Artisan deal also brings some valuable engineering experience with power optimization to ARM, which is already a market leader in low-power embedded design. Although ARM is moving in the opposite direction of ARC, MIPS, and Tensilica—which are focusing almost exclusively on processor cores—ARM is a much larger company, with the resources to make a broader strategy work.

By Fall Processor Forum, ARM had already announced a year's worth of new products by anyone else's standards, but there was much more to come. First, ARM unveiled a reorganization of its product line and the new Cortex family of embedded-processor cores. Then, ARM revealed its NEON DSP extensions for next-generation Cortex cores. Finally, near the end of the year, ARM announced the world's first commercial 32-bit processor implemented in asynchronous logic. All three announcements will keep ARM busy in 2005 meeting promised delivery dates.

ARM's Cortex-A series will include high-performance processor cores supporting the complete ARM instruction-set architecture, including Thumb-1 and Thumb-2 16-bit instructions. The Cortex-R series will deliver somewhat less performance than Cortex-A processors while using less power. The Cortex-M series is a greater departure, because it will consist of even smaller 32-bit cores supporting only Thumb-1 and Thumb-2 instructions, not the standard set of 32-bit ARM instructions.

Cortex-M is the flag bearer for ARM's microcontroller strategy, which is to pull the market away from 16-bit processing in favor of ARM's 32-bit architecture. (Although Cortex-M processors will be limited to 16-bit Thumb instructions, they are still 32-bit processors.) The first core in this series is the Cortex-M3, which is also the first processor to implement the ARMv7 architecture. (See *MPR 11/29/04-01*, "ARM Debuts Logical V7.")

ARM's Own Alternative to OptimoDE

Although ARM hasn't finalized the architectural specification, the NEON extensions will add SIMD and DSP instructions to Cortex processors. NEON will include an additional register file, and the new instructions will perform integer arithmetic as well as fixed-point or floating-point signal processing.

Unlike OptimoDE, NEON isn't a loosely coupled coprocessor—the NEON engine is tightly coupled to the Cortex processor core. One benefit is a unified programming model. Programmers can mix ARM, Thumb-2, and NEON instructions in the same datapath using a single view of memory, with a single core to trace and debug. Although NEON could be an alternative to OptimoDE, it's possible to use both with the same processor.

Before the industry had time to fully digest the news about Cortex and NEON, ARM announced a new ARM9 processor core implemented in asynchronous logic. Although it isn't the first 32-bit asynchronous processor, or even the first asynchronous ARM processor, it will be the first commercially available 32-bit asynchronous processor when it ships to licensees in 2005. (Alas, it didn't ship in time to be eligible for our 2004 *MPR* Analysts' Choice Awards. Wait until next year.)

Remarkably, SoC architects can integrate the asynchronous core in their designs using industry-standard design tools, physical libraries, and fabrication processes. Handshake Solutions, a Royal Philips line of business in the Netherlands, designed the new core by working closely with ARM. By our estimates, the new core could deliver the same performance as a conventional ARM9 while consuming 30–50% less power—a significant accomplishment. (See *MPR 11/29/04-02*, "ARM's Asynchronous Handshake.")

We hope the busy bees at ARM enjoyed a much-deserved rest over the holidays, because no other processor-IP company introduced as many new products, extended as many existing products, or executed as many strategic acquisitions as ARM did in 2004. The coming year will be crucial for the company, because it has to fulfill its numerous commitments and absorb its acquisitions without stumbling in the marketplace. If ARM can follow through, it will finish 2005 a much more formidable competitor.

IBM Expands Licensing Strategy

Although IBM Microelectronics has licensed a great deal of semiconductor IP to its own ASIC customers over the years, the company is a relative newcomer to the business of licensing processor IP for fabrication at outside foundries. In 2004, IBM embarked on a major campaign to expand its licensing business and promote its Power architecture—IBM's umbrella term for the Power/PowerPC architecture.

In April, IBM announced its "Power Everywhere" initiative. For the first time, IBM will consider licensing any Power/PowerPC core or chip implementation. The company said it's already licensing some PowerPC 7xx- and 9xx-series cores to customers. IBM's website even offers a freely downloadable model of the PowerPC 440 hard core for evaluation. (See *MPR 4/26/04-02*, "IBM Loosens Up CPU Licensing.")

The most interesting aspect of Power Everywhere was IBM's formation of Power.org, an open industry consortium that will help guide the architecture. The consortium is independent of IBM and may even formulate standards for submission to industry-standards bodies, such as the IEEE. However, IBM firmly stated it will retain ultimate control of the Power architecture. The consortium will have a mechanism for suggesting architectural changes or extensions, but the initial indication is that architectural modifications won't be the main order of business. So far, 15 companies have signed up for Power.org. One notable absence is Freescale, IBM's longtime PowerPC partner and competitor. (See *MPR 12/27/04-02*, "Bringing Power to the People.")

In another surprise move, IBM closed an unprecedented deal with Applied Micro Circuits Corp. (AMCC) in 2004. For $227 million in cash, AMCC purchased a royalty-free license to all PowerPC 4xx-series cores and acquired about 150 standard parts based on the PowerPC 403, 405, and 440 cores. Although IBM still owns the cores, AMCC is now the sole supplier of the chips. In addition, AMCC acquired two of IBM's PowerPC design teams and negotiated a global patent cross-licensing agreement with IBM. (See the sidebar, "AMCC Strikes a Big Deal for PowerPC," in *MPR 4/26/04-02*, "IBM Loosens Up CPU Licensing.") AMCC lost little time exploiting this deal. At Fall Processor Forum, AMCC announced its first new PowerPC chip, the 440SPe I/O processor. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

Despite these moves, IBM still is less flexible than other processor-IP vendors are. To compete more effectively with ARC, ARM, MIPS, and Tensilica, IBM needs more synthesizable processor cores that are portable to fabrication processes at independent foundries. IBM also needs a wider variety of processor cores spanning the range from low power to high performance. Nevertheless, IBM is on the right course and is successfully promoting PowerPC to a larger audience.

MIPS Keeps Relatively Quiet

Unlike the noisemakers at ARM, the folks at MIPS Technologies quietly concentrated on supporting their existing products and returning the company to firm financial ground in 2004. The most significant MIPS announcement was its new DSP extensions unveiled at Fall Processor Forum.

It would be a mistake to interpret the company's relatively low profile as a sign the MIPS microprocessor architecture is waning. On the contrary, MIPS licensees were extremely active during the year. Companies like AMD (with its Alchemy family), Broadcom, Cavium, PMC-Sierra, and Toshiba announced significant new MIPS32- and MIPS64-based embedded processors in 2004, and MIPS scored numerous design wins in the fast-growing consumer-electronics market. While ARM has staked a solid claim in the wireless handheld territory, MIPS is more popular in higher-performance embedded systems, such as DVD recorders and digital TV set-top boxes.

The new DSP extensions shown at FPF will improve media performance on MIPS 32- and 64-bit processors without bloating the size of the cores. New SIMD instructions and registers support 32-bit multiply-accumulate (MAC) operations in addition to multiple 8- or 16-bit MACs. Simulations indicate that performance improvements will range from 1.4× to 3.0× when compared with existing MIPS cores. (See *MPR 11/1/04-02*, "MIPS Takes Aim at Low-Cost DSP.") However, MIPS still hasn't caught up with similar technology from ARC, ARM, and Tensilica. All three competitors offer DSP extensions to their processor cores or optional DSP engines that surpass the MIPS DSP extensions in both scope and performance. The ARC 700 processor even includes some formerly optional DSP instructions as a standard feature.

MIPS also lags behind ARC and Tensilica in configurability, though it remains a notch ahead of ARM in that regard. MIPS introduced its first configurable processor cores in 2003 and has done little to advance the technology since then. (See *MPR 3/3/03-01*, "MIPS Embraces Configurable Technology.") It's not that MIPS is lazy. Unlike ARC and Tensilica, MIPS views processor configurability as a worthwhile convenience, not a central theme of its strategy. In addition, MIPS—like ARM—is very protective of its CPU architecture. Both companies view unrestricted customization as a potential threat to architectural stability. And both companies have CPU architectures to defend that are more solidly entrenched than are those of ARC and Tensilica.

The most impressive MIPS-based chips announced in 2004 were high-performance embedded processors from Broadcom, Cavium, PMC-Sierra, and Toshiba. The first three companies in that group made a big splash at FPF with multicore MIPS64 processors. Broadcom announced its dual-core BCM12xx series and quad-core BCM14xx series. (Broadcom announced almost identical processors in 2002 but missed its delivery dates; the new chips are now sampling and will ship in 2005.) Cavium, a well regarded but relatively small vendor of network security chips, stunned the industry by announcing its new Octeon family of network processors with two, four, eight, or sixteen MIPS64 cores. In addition, the Octeon processors are the first to implement the MIPS64 Release 2 specification, and they do it with a new full-custom MIPS64 core. (See *MPR 10/5/04-01*, "Cavium Branches Out.") Not to be outdone, PMC-Sierra announced the dual-core RM11200 processor, which will run at a speedy 1.8GHz. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

According to the industry's rumor mill, MIPS was a troubled company in 2004, but recent financial results don't justify the pessimism. For years, MIPS enjoyed rich royalties from the PlayStation 2 and especially from the Nintendo 64, a

bonanza that couldn't last forever. (See *MPR 6/1/98-03*, "Mario Makes Millions for MIPS.") By refocusing on synthesizable processor cores instead of full-custom hard cores, MIPS has tightened its business strategy.

In 2005, the company's challenge will be to resist growing competition from ARM at the low end and PowerPC at the high end. In particular, MIPS needs to defend against encroachment by PowerPC into network processors and other high-performance embedded processors, which are vital markets for MIPS. Still, it would be foolish to bet against the MIPS architecture, which remains one of the most popular CPU architectures in the embedded-processor world.

Tensilica: Processor-IP or EDA Company?

ARC was the first company to license a configurable microprocessor core, but Tensilica is pushing the technology to new frontiers. Indeed, Tensilica is moving so aggressively in this direction that some observers wonder if the company is really a processor-IP vendor. Lately, Tensilica seems more like a vendor of electronic design automation (EDA) tools that also happens to license microprocessor cores. *MPR* considers the question moot, because we think design-time configuration should be a standard feature of all soft IP.

Tensilica stimulated the debate by introducing a revolutionary design tool in 2004: the XPRES (Xtensa PRocessor Extension Synthesis) compiler. XPRES automatically creates application-specific custom instructions for the Xtensa LX processor core by analyzing ordinary C/C++ software code. In fact, XPRES can generate hundreds of thousands of possible custom extensions in minutes, along with nifty graphs that allow Tensilica's customers to make intelligent tradeoffs between performance and cost. No other processor-configuration tool comes close to XPRES. (See *MPR 7/12/04-01*, "Tensilica's Automaton Arrives.")

XPRES is an optional tool for Tensilica's latest customizable processor core, Xtensa LX, also introduced in 2004. Xtensa LX alone would have been enough to cement 2004 as a productive year for the company. The new core is a major upgrade of the Xtensa V, which was introduced in 2002. Xtensa LX relieves the bottlenecks restricting on-chip I/O bandwidth; has an easily configurable instruction pipeline; offers the option of extensive clock gating to slash power consumption by 37% compared with Xtensa V; and debuts Tensilica's Flexible-Length Instruction Xtensions (FLIX). FLIX allows customers to create VLIW-like 32- or 64-bit instruction words containing multiple subinstructions—a unique way to extend a RISC instruction set.

In addition, Xtensa LX has a new configurable DSP engine called Vectra LX. This optional engine has 64-bit instruction words with three issue slots for ALU, MAC, and load/store operations. In all, Vectra LX supports about 200 instructions for 16-bit fixed-point signal processing. Among processor-IP vendors, only ARM offers similar DSP power, with its OptimoDE engines. However, Vectra LX is more closely coupled to the processor core than OptimoDE is. (See *MPR 5/31/04-01*, "Tensilica Tackles Bottlenecks.")

Tensilica backed up its performance claims for Xtensa LX and Vectra LX with independently certified benchmark results. For a while, Xtensa LX owned the highest score in the EEMBC consumer benchmark suite, outrunning the previous champion by a three to one margin. Shortly afterward, Freescale's MPC7447A surpassed Xtensa LX, but the MPC7447A had to run at 1.4GHz to beat the Tensilica processor, which was simulated at only 330MHz. When Berkeley Design Technology Inc. benchmarked an optimized Xtensa LX core with Vectra LX DSP engine at 370MHz, the Tensilica processor easily beat every other licensable DSP or CPU core ever tested by BDTI.

For all these reasons—high bandwidth, low power consumption, architectural flexibility, powerful DSP extensions, and benchmarked performance—we have chosen **Tensilica**'s **Xtensa LX** for our *MPR* Analysts' Choice Award as the **Best IP-Core Processor** of 2004. Owing to the nature of Tensilica's technology, the processor core is almost inseparable from its design tools and configuration options, so the award recognizes the whole package—including XPRES, an extra-cost option. All things considered, Xtensa LX was the most innovative IP-core processor shipped last year. ◇

Best IP-Core Processor: Tensilica's Xtensa LX

Our *MPR* Analysts' Choice Award for the **Best IP-Core Processor** of 2004 goes to **Tensilica**'s **Xtensa LX**. Our other nominees are also strong products: the ARC 700, ARM1156T2F-S, and ARM1176JZF-S. However, Xtensa LX emerges as the obvious choice.

We chose Xtensa LX for several reasons: its exceptional performance (verified by independent benchmark results), low power consumption, high bandwidth, unmatched architectural flexibility, powerful Vectra LX DSP engine, and unique XPRES design tools.

Tensilica used XPRES to boost Xtensa LX's performance in the EEMBC consumer benchmarks by 1.17× to 18.7×—and the modifications required only about an hour's work. That's a remarkable return on a minimal investment of labor. Even without XPRES, Xtensa LX would be the leading contender for this award, but the combination is unbeatable. Our congratulations to Tensilica on a job well done in 2004.