Reed Electronics Group

MICROPROCESSOR REPORT

www.MPRonline.com

THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

PREVIEW: FALL PROCESSOR FORUM

Deluge of Multicore Processors for PCs, Servers, Embedded Systems

By Tom R. Halfhill {9/20/04-01}

If two heads are better than one, microprocessors are about to become twice as smart. Dual-core x86 processors for PCs and servers are coming soon from AMD and Intel, along with their transition to the x86-64 architecture. It's the biggest step in x86 evolution since the migration from 16 bits to 32 bits during the 1980s.

Meanwhile, high-performance embedded processors and digital signal processors (DSP) are evolving at an even faster rate. Networking chips with as many as 16 processor cores are making their debut, along with massively parallel processors that squeeze hundreds of cores onto a single chip. New extensions for audio and video decoding are coming from multiple vendors. Another company is unveiling a parallel-processing DSP for imaging systems. A leading intellectual-property (IP) vendor will describe a configurable on-chip interconnect, and a leading server company will reveal the first technical details of a processor for massively parallel supercomputing.

All that and more is happening at **Fall Processor Forum** (FPF), formerly known as Microprocessor Forum. FPF will be held October 4–6 at the Fairmont Hotel in San Jose, California, with the conference portion of the event on October 5 and 6. The conference is preceded by two all-day seminars on October 4: "From SIMD Through Reconfigurable Fabrics: DSP Architectures in SoC Configurations," by *Microprocessor Report* principal analyst Max Baron, and "High-Performance Processors: Trends and Implementations," by *MPR* editor-in-chief Kevin Krewell. FPF is sponsored by In-Stat/MDR and *MPR*.

Two weeks after FPF, In-Stat/MDR is sponsoring another new conference, **Processor Forum Taiwan** (PFT). This event largely consists of papers presented at FPF in San Jose, plus some new material. (See the sidebar, "Introducing Processor Forum Taiwan.")

The following FPF preview is drawn from preliminary papers submitted for the San Jose and Taiwan conferences, although we must withhold the best information under the terms of our NDAs with vendors. In all, there will be 22 vendor presentations of new processors or technologies at FPF, plus an opening-day keynote speech, discussion panels, our humorous *MPR* Awards, a vendor exposition, an evening reception, and postpresentation reviews by In-Stat/MDR analysts. For registration information, visit *www.MDRonline.com/fpf04/*.

PC, Notebook, and Server Processors

This year's opening-day keynote speech is by Dr. Bernard Meyerson, chief technologist and vice president of the

ROSS MEHAN


ROSS MEHAN

IBM Microelectronics Systems and Technology Group. Meyerson's talk is titled "Driving System Performance—A New Paradigm." The premise that device densities will double every 18 months, coupled with matching improvements in power consumption and performance, is no longer valid. Current leakage and statistical fluctuations at near-atomic dimensions are disrupting the model. Meyerson will talk about the latest alternatives, such as lower-frequency multicore processors and hardware multithreading.

After the keynote, day one of the conference begins, as usual, with a session on PC, notebook, and server processors. This high-profile session will provide a look into the future of multicore and multithreaded processors as well as power- and cost-efficient designs for notebook and desktop PCs. Each design team is pushing the limits of power efficiency, aggressively managing die size, compressing the time to market for server processors, and building complex systems on a chip (SoC). One thing all have in common is state-of-the-art manufacturing in a 90nm fabrication process.

AMD kicks off the session with a landmark paper, "Multicore Processors Go Mainstream with AMD64 Technology." AMD publicly demonstrated its first multicore Opteron processors to industry analysts and the press during the week of August 30 and is driving hard to move its multicore designs into servers. Can AMD leverage its 64-bit x86 architecture and multicore processors to win more server designs away from Intel? The speaker addressing that question is AMD Fellow Kevin McGrath, chief architect of AMD64.

VIA always has a prominent presence at our forums, and this one is no exception. Glenn Henry, president of VIA's microprocessor subsidiary, Centaur Technology, will reveal new details about the company's next-generation x86 microarchitecture. We can't divulge any more about this paper, except to say the new design is a clean break from past Centaur processors.

Fujitsu will make a strong case that Sun's SPARC architecture is alive and well by publicly disclosing new technical details about the next-generation SPARC64 V+ and SPARC64 VI server processors. Although Fujitsu announced the SPARC64 V+ this summer and the dual-core SPARC64 VI at Microprocessor Forum 2003, some of the most interesting technical information has been withheld until now. (See *MPR 8/2/04-02*, "SPARC's New Roadmap," and *MPR 11/24/03-01*, "Fujitsu Makes SPARC See Double.") Fujitsu's speaker is Aiichiro Inoue, director of the Enterprise Server Development Division.

Sun Microsystems follows up with a paper on the new UltraSPARC IV+ processor. Although x86 vendors are only now migrating to dual-core chips, the UltraSPARC IV+ is a second-generation dual-core design. The new cores are significantly upgraded, and they will run at higher clock frequencies. Sun claims the chips will be the fastest UltraSPARC processors ever built. This paper will be delivered by Dale Greenley, UltraSPARC IV+ director of engineering.

Transmeta will describe a second-generation design of its x86-compatible Efficeon processor for notebook PCs and embedded systems. Efficeon—the sequel to Transmeta's groundbreaking Crusoe processor—was introduced at Microprocessor Forum 2003. (See *MPR 10/27/03-01*, "Transmeta Gets More Efficeon.") Built in a 90nm fabrication process by Fujitsu, the second-generation Efficeon will run at higher clock frequencies and introduce new features. Transmeta's speaker, cofounder and CTO David R. Ditzel, will also update Transmeta's technology roadmap.

After these presentations, *MPR* editor in chief and principal analyst Kevin Krewell will offer his analysis of the papers, along with an analysis of Intel's recent announcements, missteps, and future plans. Next, all the speakers in this session will reassemble on stage for a question-and-answer period, which includes audience participation. Everyone will have a chance to probe the vendors about their respective plans for multicore designs, hardware multithreading, and 64-bit architectures.

High-Performance Embedded Processors

After lunch, the second conference session on day one will feature six papers on high-performance embedded processors from AMCC, Broadcom, Cavium, Faraday, Freescale, and PMC-Sierra. All the processors are intended mainly for communications and networking, and all are highly innovative designs, including multicore designs. Because most companies in this session are head-to-head competitors, it will be interesting to hear how they came up with different solutions to similar problems. The general trend is toward multiple processor cores surrounded by more peripherals and fast on-chip interconnects.

AMCC is a newcomer to this party. In April, AMCC paid $227 million to IBM Microelectronics for royalty-free licenses to all PowerPC 4xx-series processor cores; it also acquired about 150 standard-part chips based on the PowerPC 403, 405, and 440 cores. (See the sidebar "AMCC Strikes a Big Deal for PowerPC" in *MPR 4/26/04-02*, "IBM Loosens Up CPU Licensing.") Wasting no time, AMCC is ready to announce its first PowerPC 440-series product, an I/O processor for storage-area network (SAN) equipment. The speaker is Alan Millard, AMCC's senior solutions architect.

Broadcom follows with an introduction to its next-generation line of multiprocessing SoCs. Before its acquisition

Introducing Processor Forum Taiwan

Silicon Valley is the traditional center of the semiconductor industry, but everyone knows that significant engineering activity has shifted to Asia, Europe, India, and the Middle East. To reach more engineers, engineering managers, and other technology workers who cannot conveniently journey to San Jose for Fall Processor Forum, In-Stat/MDR is launching a new conference, **Processor Forum Taiwan** (PFT).

The first PFT will be held October 19–20, two weeks after FPF in San Jose. Its venue is the Lakeshore Hotel in Hsin Chu, Taiwan's high-tech suburb near Taipei. Most papers at this two-day conference are from FPF, but there will also be some new papers. PFT will share the same focus on microprocessors and microprocessor-related technology as our other conferences, and the presentations will be of the same high technical quality. PFT is an English-language event and will be moderated by *MPR* principal analyst Max Baron.

Day 1: Processors and Design

On October 19, PFT begins with a keynote speech by David Chang, deputy general director of the SoC Technology Center at the **Industrial Technology Research Institute** (ITRI), the primary center for industrial research and development in Taiwan.

Following Chang's keynote, the conference begins with a session on high-performance general-purpose processors and technologies. **Centaur Technology**, the microprocessor subsidiary of **VIA**, will deliver the first paper, a description of its next-generation x86 processor microarchitecture. This will be the same paper delivered by Centaur president Glenn Henry at FPF in San Jose.

Next comes **Fujitsu** with a paper on its SPARC64 V+ and SPARC64 VI processors: "SPARC64 V/VI for Mission-Critical Servers." This, too, will be substantially the same paper Fujitsu delivered at FPF in San Jose. The next paper, however, is something new: "Breaking Down the Requirements of Backplane Interconnects," presented by Rakesh Bhatia, a senior applications engineer at **IDT**.

Sun Microsystems is next with a presentation about its UltraSPARC IV+ processor, followed by **Transmeta** with a presentation about its second-generation Efficeon processor and its technology roadmap. These two papers will be substantially the same as the Sun and Transmeta papers given at FPF. This session wraps up with an analysis by Max Baron and a question-and-answer period, which includes an opportunity for audience participation.

The second conference session at PFT is about advanced design and implementation technologies. Three papers from ARC International, ARM, and IBM Microelectronics will be substantially the same as their papers at FPF. **ARC** will describe its extension automation for configurable ARC processors; **ARM** will explain its PrimeCell AXI configurable on-chip interconnect; and **IBM** will reveal the first architectural details of its BlueGene/L processor for massively parallel supercomputing.

Three other papers in this session are new and will discuss power-saving technology. **Cadence** will deliver a presentation titled, "Advanced Solutions for Low-Power IC Design." **National** Semiconductor's Juha Pennanen will deliver a paper about its PowerWise technology, and **Synopsys** will present "Realize Power-Efficient Designs" by Rajiv Maheshwary, senior director of Power Management Products. Day one of the conference will end after an analysis and question-and-answer period.

Day 2: DSPs and Embedded Processors

A packed session on innovative DSP architectures opens the second day of the conference. **ARM** will deliver two papers: "Multimedia Technology for Application Processors" by Philip Lu, president of ARM Taiwan (substantially the same paper ARM is presenting at FPF), plus an entirely new product announcement, presented by Noel Hurley, director of product marketing at ARM.

Four papers from MIPS Technologies, PicoChip, Renesas, and Xilinx are substantially the same as their FPF presentations. **MIPS** will present "Signal-Processing on the MIPS Architecture"; **PicoChip** will deliver "Redundancy and Binning in PicoChip's Processor," by Will Robbins, design director; **Renesas** will present "An SH-4 CPU with an AV/Graphics Subsystem and High-Speed Interconnects," by Mitsuhiro Miyazaki, deputy project manager; and **Xilinx** will deliver "Virtex-4 FX Extends PowerPC Instructions."

Tensilica will round out the DSP session with a new presentation by Steve Leibson, technical evangelist. The end of this session features the customary analysis and question-and-answer period.

Wrapping up the conference is a session on high-performance embedded processors. All four papers are substantially the same as presentations at FPF: **AMCC** will deliver "Unveiling the PowerPC 440xx I/O Processor," by Sam Fuller, vice president of marketing, AMCC Embedded Group; **Broadcom** will present "The Next-Generation Line of Broadcom's SiByte Multiprocessing SoCs"; **Cavium** will present "A Next-Generation Processor for Networking," by Amer Haider, director of strategic marketing; and **Faraday Technology** will present "An Integrated Networking Application Processor," followed by the analysis and question-and-answer period.

For more information about PFT or to register online, go to:

www.mdronline.com/pft04/

by Broadcom, SiByte announced its first MIPS64-compatible SB-1 processor core at Embedded Processor Forum 2000 (see *MPR 6/26/00-04*, "SiByte Reveals 64-Bit Core for NPUs") and the first dual-core MIPS-based SoC, the BCM1250, at Microprocessor Forum 2000 (see *MPR 1/29/01-05*, "Network Processors Multiply"). The latest Broadcom chips will build on the first-generation architecture by adding multiple processor cores, more memory, and enhanced I/O features—all connected by a high-bandwidth, low-latency on-chip bus. Broadcom's speaker is Laurent Moll, SoC architect.

Cavium Networks will introduce a new MIPS-compatible multiprocessor for next-generation network services. It marks a significant new direction for Cavium, which until now has been known primarily for its security processors. (Cavium's Nitrox Plus CN1340P won the *MPR* Analysts' Choice Award for Best Security Processor in 2002; see *MPR 2/18/03-09*, "Security By Design.") The company's new Octeon network service processors are radical MIPS64-based designs with 2 to 16 processor cores. Octeon chips will integrate packet processing, content filtering, and security processing. Cavium's speaker is Richard E. Kessler, principal member of the technical staff.

Faraday Technology will introduce a new integrated networking-application processor. Intended for network storage systems and offload engines, the processor is based on Faraday's recently announced FA626 core, which is compatible with the ARM v4 architecture. Unlike conventional ARM cores, the FA626 includes a custom on-chip interconnect, an L2 cache, and coherency logic for interfacing with additional processing resources. (See *MPR 5/18/04-02*, "Risk Reduction Faraday Style.") Faraday's speaker is C.J. Liang, associate vice president of research and development.

Freescale Semiconductor (formerly the Motorola Semiconductor Products Sector) will take the stage to introduce its first dual-core PowerPC processor. This landmark SoC has multiple on-chip controllers and the latest I/O interfaces to support its dual processor cores. The chip is intended for networking, wireless communications, storage applications, industrial applications, and general high-performance computing. Freescale's speaker is Toby Foster, system architect.

ROSS MEHAN

PMC-Sierra will deliver the final paper in this session: "PMC-Sierra's Third-Generation Integrated Processor." Most details are under wraps, but the processor is a significantly upgraded MIPS64-compatible chip that embodies the latest trends in high-performance designs. It's intended for networking, telecommunications, and storage applications. The presenter is Bryan Chin, a principal engineer of the Microprocessor Products Division at PMC-Sierra.

After a review of the high-performance embedded-processor papers by *MPR* senior analyst Tom R. Halfhill, the speakers from AMCC, Broadcom, Cavium, Faraday, Freescale, and PMC-Sierra will reassemble on stage for the question-and-answer panel—with an opportunity for the audience to participate.

Following the panel, *MPR* editorial board member Nick Tredennick will ascend to the podium for his satirical *MPR* Awards, a long-running tradition at the forum. When the conference adjourns, attendees will move down the hall for the Expo Night reception.

Innovative Signal-Processing Architectures

The second day of the conference opens with an unusually large session on DSPs and other chips for signal processing and parallel processing. There will be eight presentations from ARM, MIPS Technologies, Renesas, Xilinx, Texas Instruments, ChipWrights, ClearSpeed, and PicoChip. Among their announcements are instruction-set architecture (ISA) enhancements, configurable arrays, high-performance/low-power DSPs, and massively parallel arrays—all aimed at the fast-moving DSP markets. So busy is the schedule that this session, interrupted by a break, will occupy the entire morning.

ARM will begin the session by unveiling its next-generation media architecture: new SIMD (single instruction, multiple data) extensions that will accelerate multimedia applications by using tightly integrated, but separate, execution hardware. These extensions will support multiple data types in an independent register file. ARM's speaker is Simon Ford, the technical lead for multimedia application processors.

MIPS will deliver the next paper by publicly disclosing the first technical details about new signal-processing capabilities on the MIPS architecture. Target markets include set-top boxes, DVD players/recorders, digital cameras, printers, handheld audio devices, soft modems, and voice-over-Internet-Protocol (VoIP) phones and switches. The presenter is Radhika Thekkath, director of architecture at MIPS.

Renesas follows with a paper titled "An SH-4 CPU with an AV/Graphics Subsystem and High-Speed Interconnects," presented by Mitsuhiro Miyazaki, deputy project manager. Renesas has reinforced an SH-4 processor with special engines for MPEG audio/video decoding and 3D graphics. A unified memory architecture and high-speed on-chip interconnects

help reduce costs while maintaining high performance. Target applications include entertainment and multimedia systems.

Xilinx is next on the schedule, with a paper titled "Virtex-4 FX Extends PowerPC Instructions," presented by Ahmad Ansari, senior staff systems architect. The new Virtex-4 FX is the latest family of FPGAs that includes one or two embedded processor blocks, up to four Ethernet controllers, and serial transceivers capable of supporting I/O operations from 600Mb/s to 11.1Gb/s. Each hard-processor block has a PowerPC 405 core. Xilinx will explain how the FPGA's configurable logic can adapt the PowerPC core for high-performance embedded applications.

Texas Instruments precedes the midmorning break with a paper titled "A Hardware and Software Approach to Portable Power Management," presented by Leon Adams, DSP strategist. TI will discuss various approaches to reducing power consumption in DSPs, using such techniques as clock gating, optimized clock tree structures, greater parallelism, low-leakage fabrication, idling clock domains, scaling voltage/frequency, peripheral management, and sleep modes.

ChipWrights will follow the morning break by unwrapping a high-performance imaging DSP with 16 parallel processors. This powerful chip is also a highly integrated SoC that includes a RISC processor core. It's designed for applications that need high-performance imaging with a low-power, low-cost DSP: digital cameras, camcorders, security cameras, portable media players, machine-vision systems, and digital copiers. The presenter is John Redford, CTO of ChipWrights.

ClearSpeed returns to our forum with a paper describing a new 50GFLOPS processor for scientific computing and DSP applications. This chip is a significantly improved version of the CS301 processor ClearSpeed launched at Microprocessor Forum 2003. (See *MPR 11/17/03-01*, "Floating Point Buoys ClearSpeed," and *MPR 1/12/04-02*, "ClearSpeed Hits Design Targets.") ClearSpeed says the new chip has twice the peak performance of its predecessor and significantly faster memory I/O. The presenter is Simon McIntosh-Smith, director of architecture.

PicoChip will close this busy session with a paper titled "Redundancy and Binning in PicoChip's Processor." The company will reveal new information about its PC102, a massively parallel chip with 344 processor cores. (See *MPR 10/14/03-03*, "PicoChip Makes a Big MAC.") Although speed binning is common in the processor industry, PicoChip does defect binning—built-in redundancy allows the chips to bypass internal defects and still deliver high performance. Will Robbins, design director, will reveal new details about the technique.

After lunch, *MPR* principal analyst Max Baron will offer his analysis of the eight papers in the DSP session and then moderate the question-and-answer period.

Cool Technology and a Benchmarking Panel

Next comes the Cool Technology session—a collection of papers that didn't quite fit into other categories but were simply too intriguing to pass by. The papers are eclectic, and they feature three vendors: ARC International, ARM, and IBM. Topics include advanced design automation for configurable processors, on-chip interconnects, and massively parallel supercomputing.

ARC begins with its paper, "Extension Automation for the ARC Processor Family," presented by Lee Hewitt, lead designer. ARC's Extension Interface Automation (EIA) is designed to automate and simplify the extension of the company's customizable processor cores, including the latest high-performance ARC 600 and ARC 700 processors. (See *MPR 3/8/04-01*, "ARC 700 Aims Higher," and *MPR 12/15/03-01*, "ARC Alters Trajectory.") Starting with a basic extension specification, EIA can automatically synthesize the extension logic in multiple industry-standard hardware-design languages.

ARM follows with its second paper of the conference, "PrimeCell AXI Configurable On-Chip Interconnect." Tim Mace, PrimeCell product manager, will describe how chip designers can rapidly configure a multilayer AXI-compatible on-chip interconnect for high-performance, low-power applications. Interoperability with other intellectual property and electronic design automation (EDA) tools will make it easier to design highly integrated SoCs.

IBM Microelectronics finishes the Cool Technology session with a paper about its new BlueGene/L processor for massively parallel supercomputing. This will be the first public disclosure of significant architectural details. IBM will reveal the PowerPC chip's internal design, cache hierarchy, use of embedded DRAM, and custom floating-point unit. IBM will also provide some measured performance metrics. The presenter is Alan Gara, chief architect.

Following the customary question-and-answer period, the conference will close with a late-breaking addition: a special discussion panel about embedded x86 benchmarking. We've added this panel to address the issues reported in our recent article, "Benchmarking the Benchmarks" (see *MPR 8/30/04-01*). In addition, the Embedded Microprocessor Benchmark Consortium (EEMBC) has established a working group to develop new benchmarks for

For More Information

- More information about **Fall Processor Forum 2004** is available on our website: *www.mdronline.com/fpf04/*
- To register for FPF online, please go to: *www.mdronline.com/fpf04/register.html*
- More information about **Processor Forum Taiwan** is available: *www.mdronline.com/pft04/*
- To register for PFT online, please go to: *www.mdronline.com/pft04/reg.html*

multiprocessing systems—an especially relevant topic, considering the numerous multicore processors announced at FPF.

MPR has extended panel invitations to AMD, Intel, Transmeta, VIA, EEMBC, and Synchromesh Computing. As this article went to press, almost all those companies had agreed to send representatives, including Glenn Henry from VIA's Centaur subsidiary, David Ditzel from Transmeta, Markus Levy from EEMBC, and Alan Weiss from Synchromesh Computing. This is sure to be a lively and controversial discussion.