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PREVIEW: EMBEDDED PROCESSOR FORUM 2004

New CPUs From ARM, Motorola, PMC-Sierra, TI, Tensilica, and More

By Tom R. Halfhill {4/19/04-01}

The boom years of the 1990s aren't quite back, but at least now the semiconductor industry has a steady pulse. **Embedded Processor Forum 2004** will be the coming-out party for several innovative development projects that survived the tech recession and hope to breathe new life into the embedded market. They span an unusually wide range of architectures and applications.

During the two-day conference portion of **EPF 2004**—May 18–19, at the Fairmont Hotel in San Jose, California—new embedded processors, architectures, and synthesizable cores will be unveiled by Altera, AMD, ARM, Cradle, Emblaze, MobilEye, Motorola, PMC-Sierra, StarCore, Texas Instruments, Tensilica, Ultra Data, and VIA/Centaur. Almost all these presentations will be the first technical disclosures of their products. The new processors run the gamut from traditional RISC and CISC architectures to bold new designs optimized for communications, mobile multimedia, machine vision, and signal processing.

Each conference day will begin with a keynote address, this year featuring ARM on May 18 and AMD on May 19. A three-part session on unusual embedded-software tools is scheduled for May 18, with presentations from ACE (Associated Compiler Experts), Silicon Hive (a Philips-funded startup), and Transitive. A special panel discussion about on-chip interconnect technology will follow the regular sessions on May 19. As is customary, the first day of the conference will end with a vendor exhibition in the evening.

Three all-day seminars on May 17 and May 20 will bracket the conference portion of the forum. The Monday seminars are "Microprocessors for Professionals," an introductory-level presentation by Tom R. Halfhill, senior analyst, In-Stat/MDR, and "Best Processors for Low-Power Applications," presented by Max Baron, principal analyst, In-Stat/MDR. The Thursday seminar is "Choosing the Best High-Performance Embedded Microprocessors," presented by Jim Turley, industry analyst, *Silicon Insider*.

For more information or to register for **EPF 2004**, visit *www.MDRonline.com/epf04*.

Day One: High Performance and Tools

ARM will open the conference with a keynote address by CTO Mike Muller, who will talk about present and future system-level design challenges. Afterward, the first session will begin with four presentations of high-performance

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embedded processors. In the first presentation, ARM's Peter Middleton, an engineering manager, will unveil a new symmetric-multiprocessing (SMP) core based on the ARMv6 architecture. This core will launch ARM—known primarily for its low-power processors—into a new realm of high performance. In addition, the synthesizable SMP core offers developers new flexibility to create scalable designs.

Next is **Motorola's** presentation of its new V4e-based ColdFire processors. These standard-part chips are designed for embedded control, communications, and security applications. The presenter will be C. Edward Nuckolls, a technical staff fellow. (Motorola introduced the V4e architecture at Microprocessor Forum 2000; see *MPR 10/23/00-02*, "ColdFire V4 Gets Even Hotter.")

PMC-Sierra will follow with a technical presentation of its new RM9150MR processor, which will debut an on-chip interconnect called the Fast Device Bus (FDB). John Kinsel, PMC-Sierra's principal engineer, will explain how his team designed the FDB for high performance and rapid reuse in the company's future CPUs.

Wrapping up the session on high-performance embedded processors will be a presentation by Glenn Henry, founder and president of **Centaur Technology**, now part of VIA. Henry—a lively speaker and longtime favorite at the forums—will describe a new embedded x86 processor with integrated security hardware. This processor is notable for both its x86 compatibility and its low power consumption.

The second session on day one is a slight departure for **EPF**: it will focus on three unusual software tools for embedded systems. The first speaker will describe **ACE's** CoSy Express compiler generator, which allows CPU architects and tool vendors to rapidly develop new compilers and explore the possibilities of new architectures. ACE believes it can accelerate innovation by relieving a difficult bottleneck in embedded-software development. The presentation will be delivered by Martijn de Lange, CEO of ACE, which was founded in 1975 in Amsterdam.

Next on the schedule is a new C/C++ compiler for a massively parallel CPU architecture: the ultralong instruction word (ULIW) architecture introduced at Microprocessor Forum 2003 by **Silicon Hive**, a Philips subsidiary. (See *MPR 12/1/03-02*, "Silicon Hive Breaks Out.") One of Silicon Hive's first implementations of this architecture, the Avispa+ processor core, won the *MPR* Analysts' Choice Award for Best Soft-IP Processor Core of 2003. (See *MPR 2/9/04-18*, "Avispa+ Buzzes With Innovation.") Silicon Hive claims it has solved one of the toughest problems in massively parallel computing: creating a compiler capable of exploiting the processor's potential for instruction-level parallelism. *MPR* has been a little skeptical of that claim, so Silicon Hive has offered to describe its HiveCC compiler in public. The presenter will be Dr. Ir. Lex Augusteijn, Silicon Hive's chief compiler architect, who will fly in from the Netherlands to defend his company's claims of a massively parallel breakthrough.

To finish the session on software tools, **Transitive** will present QuickTransit, a dynamic binary translator for embedded processors. QuickTransit is essentially an emulation layer that allows software compiled for one embedded-processor architecture to run on a different architecture. It sounds too good to be true—or perhaps too good to be practical—but Transitive has been developing the technology for years and will give a demonstration. The presenter will be Alasdair Rawsthorne, Transitive's founder and CEO.

More on Day One: Signal Processing

The third and final session on day one of the conference will offer four interesting presentations related to embedded signal processing, which includes more than just DSPs. First on the slate is **ARM**, which will disclose technical details about its new OptimoDE data-engine technology. OptimoDE is part of ARM's answer to the configurable-processor technology from companies like ARC and Tensilica. Instead of letting customers modify the CPU core, ARM is providing a new way to integrate application-specific data engines that work like on-chip coprocessors. ARM's presenter will be Koen Van Nieuwenhove, the OptimoDE product development manager.

Following ARM's presentation, **Broadcom** will reveal new details about its FirePath microprocessor architecture, first introduced at **EPF 2001**. FirePath is a symmetric long-instruction-word (LIW) architecture with SIMD capabilities and is particularly well suited for signal processing in DSL modems. (See *MPR 9/9/02-01* "The Proprietas Paradox.") New instructions with packed-data formats make FirePath even more efficient for signal processing in communications as well as in other applications. The presenter will be Sophie Wilson, Broadcom's chief architect for FirePath.

Next, **Motorola** will introduce a new family of StarCore-based DSPs. They represent the "low end" of Motorola's high-performance StarCore-based devices and are designed for communications, security, industrial control, office automation, and other signal-processing applications. (See *MPR 10/20/03-01*, "Motorola Enhances StarCore DSP.") The speaker is Joseph Gergen, Motorola's StarCore chief architect.

Wrapping up the session and the first day of the conference is **Tensilica**, which will unveil a second-generation DSP engine for its configurable Xtensa microprocessor. The

new DSP engine is based on Tensilica's FLIX technology, announced at **EPF 2002**. (See *MPR 11/25/02-06*, "FLIX: The New Xtensa ISA Mix.") Like the Xtensa microprocessor core, the DSP engine is configurable for specific applications. Tensilica promises to show benchmark results that will surprise everyone.

Day Two: More Diversity and Low Power

The second day of the conference begins with a keynote address by **AMD's** new chief strategy officer, Dr. William T. Edwards, who will show how embedded-processor technology is driving the future of consumer products.

Jeff Bier, general manager of Berkeley Design Technology Inc. (BDTI), will host the first session of the day: processors for video applications. The first presentation is from **MobilEye Vision Technologies**, which will disclose the architecture of its EyeQ programmable vision processor. This unusual processor is designed for computationally intensive real-time visual-recognition and scene-interpretation applications, especially in vehicles. The presenter will be Elchanan Rushinek, MobilEye's ASIC director.

Next, **Ultra Data** will describe a licensable video-processor core optimized for decoding H.264 and video codecs for high-definition displays. It's a fully programmable processor, so developers can adapt it for different applications. Jonah Probell, the founder and principal design engineer of Ultra Data, will deliver the presentation.

Cradle Technology will disclose the first technical details of its new CT3400 multiprocessor DSP, which was publicly announced last year. Although Cradle has shown high-level block diagrams of the video/imaging processor, this presentation will reveal details about the memory structure, SIMD instructions, and programmable I/O architecture. The presenter is Arthur Chang, Cradle's CEO and CTO.

The fourth presentation in this session is by **Texas Instruments**, which will disclose new details about the OMAP2420 video/imaging coprocessor, the first OMAP 2 chip. (See *MPR 3/22/04-01*, "Dial the Future.") Although TI has previously released some information about the OMAP2420, the **EPF 2004** presentation will describe the chip's imaging and video accelerator. The OMAP2420 is optimized for mobile multimedia applications. Avner Goren, a senior member of TI's technical staff, will deliver the presentation.

Six Low-Power Processors and a Special Panel

Low-power embedded processors are always an important part of **EPF**, and this year's low-power session has more presentations than any other session. **Altera** will begin by introducing the Nios II, an extensible 32-bit RISC core designed for integration in FPGAs, ASICs, and structured ASICs. Altera will describe various aspects of the instruction set, bus architecture, and instruction pipeline. The presenter will be Tim Allen, senior director of processor engineering at Altera. (Don't confuse the Nios II with Nios 2.0, presented at **EPF 2001**; see *MPR 12/3/01-01*, "Excalibur Sharpened by Nios 2.0.")

AMD follows with a presentation on an enhanced Geode system-on-chip (SoC) device. AMD acquired the Geode family from National Semiconductor late last year. (See *MPR 9/2/03-02*, "AMD, on Geode-Trek, Buys IA Division From National.") Geode is designed for thin clients, web pads, set-top boxes, and other embedded applications that are relatively low power and can benefit from x86 software compatibility. AMD's paper will describe the chip's low-power performance and other features. The presenter will be Steve Kommrusch, a senior manager and design engineer at AMD.

Next up is **ARC International**, which will reveal heretofore-secret details about its latest configurable-processor core, the ARC 700. (See *MPR 3/8/04-01*, "ARC 700 Aims Higher.") We can't even hint at what this presentation is about, but it will definitely alter ARC's competitive position in the low-power market. Nigel Topham, ARC's chief architect, will spill the secrets.

Following ARC's revelations, **Emblaze Semiconductor** will officially launch a new multimedia application processor for wireless handsets, disclosing technical details for the first time. This chip is designed for next-generation cellphones and other handheld devices that will have the latest audio/video capabilities. The presenter will be Erez Sperling, director of architecture and algorithms for Emblaze.

For More Information

Embedded Processor Forum 2004 takes place on May 17–20 at the Fairmont Hotel in San Jose, California. The two-day conference portion of the forum is May 18–19 (Tuesday and Wednesday), with a vendor exhibition on the evening of May 18. In addition, In-Stat/MDR will offer two all-day seminars on Monday, May 17, and another all-day seminar on Thursday, May 20. For more information about **EPF 2004** and to register online, visit *www.MDRonline.com/epf04*.

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Tensilica will introduce a new configurable-processor core to succeed the Xtensa V. (See *MPR 9/16/02-01*, "Tensilica Xtensa V Hits 350MHz.") The next-generation core is capable of even higher performance and is more configurable as well. Ashish Dixit, Tensilica's vice president of hardware engineering, will deliver this paper.

The final conference presentation will be from **StarCore LLC**, the independent spinoff from Infineon, Lucent/Agere, and Motorola. The company will introduce a new DSP architecture that's backward compatible with previous StarCore DSPs while offering lower power consumption, reduced code size, and higher performance. StarCore will license synthesizable DSP cores based on the new architecture. (See *MPR 10/20/03-01*, "Motorola Enhances StarCore DSP" and the sidebar, "StarCore LLC Offers Soft DSPs.") CTO Amnon Rom is StarCore's scheduled speaker.

Day two and the conference portion of **EPF 2004** will close with a special panel discussion about **on-chip interconnect technology**. Panelists will be engineers from companies that have designed licensable or proprietary interconnects. They will explain the advantages and disadvantages of their technologies and answer questions from the audience. As is customary, all other sessions at the two-day conference will also be followed by question-and-answer panel discussions.

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