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# ARC 700 Aims Higher

## *Redesigned Configurable CPU Shoots for Higher Performance*

*By Tom R. Halfhill {3/8/04-01}*

Only a few months after introducing the ARC 600 configurable processor, ARC International has announced another new core: the ARC 700. But it's not an egregious exercise in instant obsolescence. The new(er) ARC processor is fully compatible with its still-available predecessor and is intended for customers willing to tolerate a larger core in return for higher performance.

ARC claims the ARC 700 is the smallest 400MHz 32-bit RISC core available—one-third the size of an ARM11 when fabricated in a 0.13-micron IC process—with lower power consumption to boot. Of course, the actual mileage may vary, because the ARC 700 is a customizable processor in the ARC tradition, so the clock speed, silicon area, and power consumption greatly depend on the customer's final configuration. Even so, it's a safe assumption that an ASIC or SoC based on the ARC 700 will outrun a comparable chip built around the ARC 600, which peaks at about 290MHz in a 0.13-micron process. The downside is that the base configuration of the ARC 700 requires nearly four times the silicon area and power of an ARC 600, which explains why the slower core remains in the product line.

The ARC 700 can run at a 38% faster clock rate than the ARC 600 because it's the first ground-up redesign of the ARC microprocessor core in many years. Although the ARC 600 improves on the earlier ARCtangent-A5 core by introducing a deeper pipeline, static branch prediction, and more power-saving features, it's still based on the same synthesizable model as the A5, which was derived from the ARCtangent-A4 and ARC 3. (See *MPR 12/15/03-01*, "ARC Alters Trajectory.") In contrast, the ARC 700 is the fruit of a parallel development project that started from scratch. To squeeze out more performance, ARC's engineers applied everything they had learned since designing the first configurable embedded-processor core in 1993.

In addition to its higher potential clock frequency—mostly the result of an even deeper pipeline—the ARC 700 has several other improvements over the ARC 600: dynamic branch prediction; a faster, single-cycle adder; some DSP extensions that were previously optional; wider memory interfaces for the instruction and data caches; a nonblocking load/store pipeline that allows two hit-under-miss data accesses; out-of-order completion for nondependent instructions; and two new instructions that will be especially useful in multicore designs.

Despite all those enhancements, the ARC 700 supports the same ARCompact instruction-set architecture (ISA) as the ARC 600 and ARCtangent-A5 do, which allows programmers and compilers to mix 16- and 32-bit instructions for greater code density. In fact, the ARC 700 is binary compatible with both the ARC 600 and ARCtangent-A5, although recompilation will improve performance. In addition, the ARC 700 works with the same new hardware- and software-development tools ARC introduced last year. The ARC 700 is fully synthesizable and licensed as soft intellectual property (IP)—and it's available now.

### Pipeline Improvements Boost Clock Frequency

Foremost among the ARC 700's enhancements is the deeper, more efficient instruction pipeline. It's now seven

stages long, compared with five stages in the ARC 600 and four stages in the ARCtangent-A5. To add two stages, ARC divided the decode and writeback stages. There is now a separate instruction-alignment stage immediately before the decode stage, plus a new result-selection stage before writeback.

RISC purists will decry the instruction-alignment stage, because RISC processors normally don't need to align instructions before decoding them. A founding principle of RISC is that 32-bit fixed-length instructions align neatly on 32-bit memory boundaries, so the processor always gets one complete instruction when it fetches 32 bits from memory. Instruction alignment is supposed to be a messy detail of old CISC architectures and their unruly variable-length instructions. But times change. Historically, RISC architectures were designed for workstations and servers, which can sacrifice the greater code density of CISC for the swifter decoding of fixed-length instructions. When CPU architects began adapting RISC architectures for embedded processors, code density suddenly became important again. That's why so many embedded RISC architectures (ARC, ARM, MIPS, SuperH, Tensilica, and others) have shorter 16-bit instructions in addition to their longer instructions.

The ARC 700 is a 32-bit RISC architecture, but the ARCompact ISA has 16- and 32-bit instructions. The 16-bit instructions duplicate the most commonly used 32-bit operations. Unlike some other ISAs having multiple instruction lengths, ARCompact doesn't require mode switching—programs can use the different instructions in any sequence. ARCompact code is up to 40% smaller than 32-bit code, and ARC claims it's even denser than ARM's Thumb-2. (See "ARCompact: An Elegant 16/32-Bit ISA," the companion article to *MPR 2/18/03-06*, "Soft Cores Gain Ground.")

When a program mixes 16- and 32-bit ARCompact instructions, it's inevitable that some of them won't align with 32-bit memory boundaries, so the processor can't depend on getting one complete instruction per fetch. Instead, the processor must scan the incoming instruction stream and find the instruction boundaries before decoding the instructions, much as a CISC processor does. When the ARCompact ISA debuted in the ARCtangent-A5 in 2001, the A5 retained the four-stage pipeline of the ARCtangent-A4, and the additional gate delays required for alignment and decoding reduced the A5's maximum clock speed by about 25%.

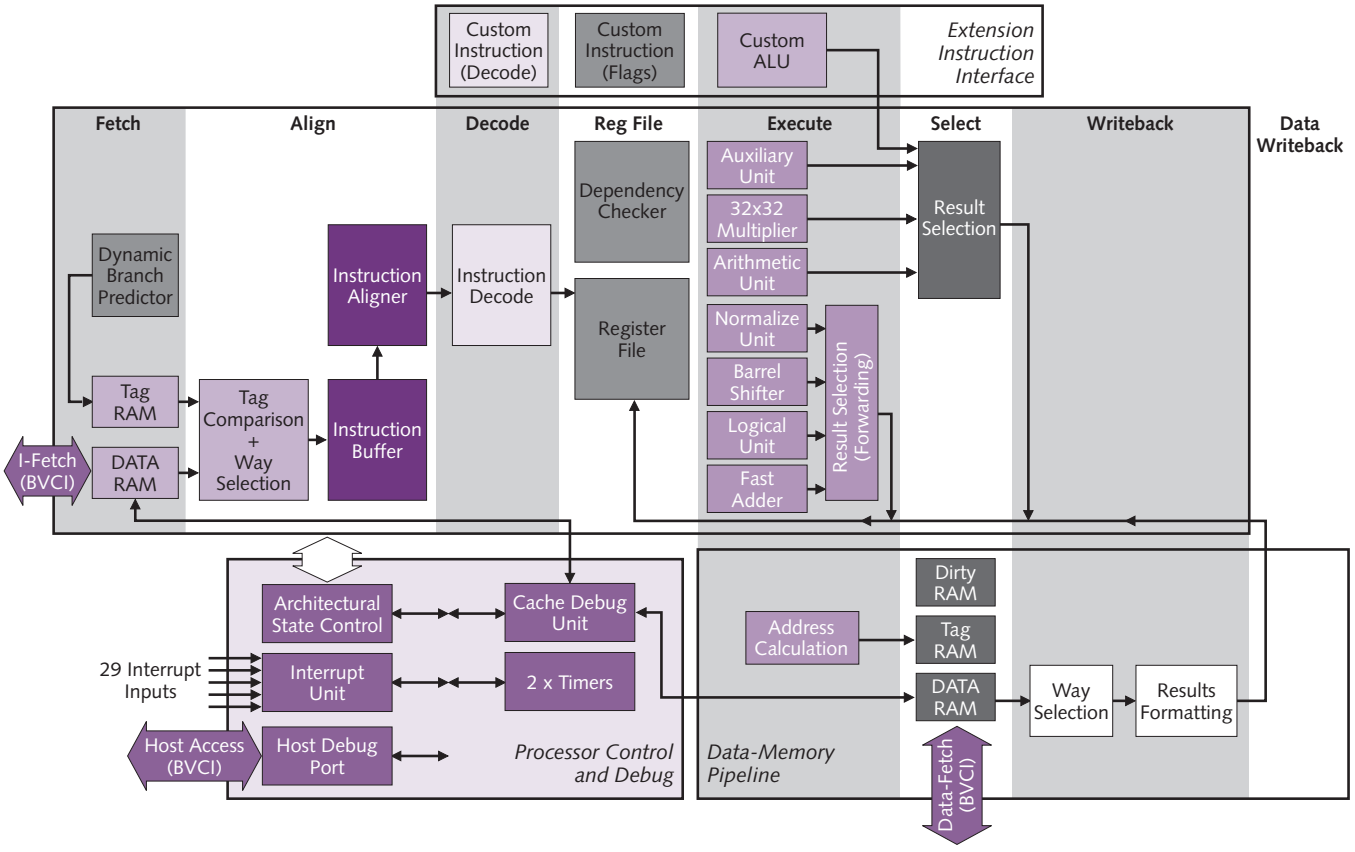


**Figure 1.** The ARC 700's seven-stage pipeline is two stages deeper than the ARC 600's pipeline. New are stages 2 (align) and 6 (select). The dynamic branch-prediction logic, another new feature of the ARC 700, is part of stage 1 (fetch). The instruction-alignment logic, previously in stage 1, now has its own stage. Stage 5 selects a result from an execution unit, which may be a standard unit or an extension unit.

Interestingly, both the ARC 700 and ARC 600 distribute those additional gate delays across two stages, but they do it differently. The ARC 600 aligns the instructions in stage 1 (fetch), then decodes the instructions in stage 2. In contrast, the ARC 700 moves the alignment logic into the new stage 2 (align), which pushes decoding to stage 3. The pipeline diagram in Figure 1 shows why. To compensate for the greater branch penalties of its deeper pipeline, the ARC 700 is the first ARC processor with dynamic branch prediction, and the prediction logic is part of stage 1. Therefore, to rebalance the pipeline without introducing too many gate delays in the decode stage, ARC inserted a new stage for the alignment logic.

The other new stage in the ARC 700—stage 6, result select—decides which execution unit will pass its result to the final writeback stage. Result selection is necessary because multiple execution units can operate in parallel and complete their results out of order in the ARC 700, even though it isn't a fully out-of-order superscalar processor. The ARC 700 always fetches, decodes, and dispatches one instruction at a time in program order, but instructions can execute, and even retire, out of order if they have no mutual dependencies.

To manage out-of-order completion, the result-select stage can accept results from multiple sources: execution units in the ARC 700's base configuration, such as the adder; optional extensions offered by ARC, such as the 32 × 32-bit integer multiplier; execution units added by licensees as custom extensions; and the load/store pipeline, which can operate in parallel with the other execution units. Because all those sources may have different latencies, depending on the instruction, any execution unit may complete a result before a preceding instruction's result is ready. If there is no interdependency, the result-select stage can choose the first available result and pass it along to the writeback stage, which can store the result out of order.

## Load/Store Pipeline Reduces Bottlenecks

ARC processors have incorporated a load/store or "data memory" pipeline for several years, and the ARC 700 expands the concept. Essentially, the processor detours load/store instructions into a separate pipeline that allows nondependent computational instructions to execute in parallel with memory accesses, thereby hiding the memory latency. The ARC 700 can now buffer two load misses at a time. In combination with out-of-order completion, this hit-under-miss capability helps compensate for the variable latencies of different execution units and memories.

Programmers writing in assembly language can manually rearrange their code to take advantage of the improved load/store pipeline, but it's easier to delegate the work to an optimizing compiler. ARC provides a good C/C++ compiler designed by MetaWare, a development-tool company acquired in 1999. Although the ARC 700 will run existing ARCompact code written for the ARC 600 and ARCtangent-A5, recompiling with the updated MetaDeveloper tools will optimize the code for the new characteristics of the ARC 700 pipeline.

The pipeline improvements alone are worthwhile, but ARC's engineers took the opportunity to make several other changes as well. As mentioned above, the 32-bit adder is faster than previous versions, allowing the ARC 700 to compute results in a single cycle. The 32-bit barrel shifter, previously an optional extension, is now standard equipment. Also standard are 13 DSP instructions, formerly optional, although the other DSP extensions (such as X and Y data memories) are still optional. Furthermore, ARC has streamlined the DSP extensions so they won't impair the ARC 700's maximum clock frequency. With or without DSP, the ARC 700 can reach 400MHz in a 0.13-micron process. Earlier ARC processors lose about 25% of their clock speed with DSP extensions.

Two entirely new instructions in the ARC 700 are EX (atomic exchange) and SYNC. Both make it easier to write code for multicore SoCs. EX is a single-cycle, noninterruptible, read-modify-write operation, which is useful for semaphores and for preserving coherency in shared-memory systems. SYNC flushes the processor's instruction and data caches, allowing multiple processor cores to synchronize their caches with shared memory. Table 1 lists all the new instructions in the ARC 700.

The memory interfaces on the optional instruction and data caches are twice as wide in the ARC 700: 64 bits, versus 32 bits in previous ARC processors. The address buses are still 32 bits wide, as are the I/O and address buses on the

| Instruction | Description |
|---|---|
| **Single Source-Operand DSP Instructions** | |
| ABSS | Absolute value (32-bit input) |
| ABSSW | Absolute value (16-bit input) |
| NEGS | Negate and saturate (32-bit input) |
| NEGSW | Negate and saturate (16-bit input) |
| RND16 | Round (32-bit input to 16 bits) |
| SAT16 | Saturate (32-bit input to 16 bits) |
| **Dual Source-Operand DSP Instructions** | |
| ADDS | Add and saturate |
| ADDSDW | Dual 16-bit add and saturate |
| ASLS | Arithmetic shift left and saturate |
| ASRS | Arithmetic shift right and saturate |
| DIVAW | Division assist |
| SUBS | Subtract and saturate |
| SUBSDW | Dual 16-bit subtract and saturate |
| **Miscellaneous Instructions** | |
| EX | Noninterruptible read-modify-write |
| SYNC | Flush instruction and data caches |

**Table 1.** The ARC 700 has 13 DSP instructions that were optional extensions for the ARC 600 and ARCtangent-A5 processors, plus two wholly new instructions. ARC says including the DSP instructions in the base configuration of the ARC 700 adds a negligible number of gates, because adding them as optional extensions would have required duplicating some arithmetic units to support the extensions without impairing the processor's maximum clock speed.

### New CEO Brings Varied Background to ARC

As *MPR* was preparing this article for publication, ARC announced a new CEO: Carl Schlachte, most recently the vice president and general manager of advanced processor solutions at Raza Microelectronics. Schlachte took the reins at ARC immediately, beginning his new job during the last week of February.

Schlachte, 40, has 20 years experience in the semiconductor industry. He landed at Raza Microelectronics after that company's acquisition of SandCraft in 2003. Schlachte was president and CEO of SandCraft, a MIPS licensee and fabless semiconductor vendor. Before joining SandCraft, Schlachte was the chairman and CEO of BOPS, which designed high-performance DSPs. Prior to joining BOPS, Schlachte spent several years at ARM as vice president of North American operations and embedded business-development manager. And before that, he worked for 11 years at Motorola, mostly in sales positions. He has a B.S. in computer science from Clemson University.

In his first interview with an outside party since becoming CEO of ARC, Schlachte told *MPR* that he approves of the company's current reorganization and tighter focus on core products. Although he was hired to implement a strategy set by the board of directors, Schlachte says he has the freedom to improvise, as conditions warrant. He believes that ARC's fundamental business model—licensing configurable soft IP—is viable and that ARC can survive and thrive as an independent company.

Under his leadership, Schlachte says, ARC will concentrate on vertical markets in which ARC-based chips already have a firm toehold. Those markets and applications include digital cameras, network-attached storage (NAS), wireless communications, and industrial control. Schlachte says he believes in the value of configurable processors and intends to continue ARC's development of small, power-efficient processor cores that allow licensees to customize the instruction set.

To reduce ARC's operating costs, Schlachte says he will form more alliances with other companies so ARC doesn't have to provide the whole ecosystem for its processors. ARC has already been moving in that direction, but the company remains burdened with too many in-house products to support. Schlachte promises to take a fresh look at ARC's product line and commitments: "We're going to run this place like a startup. We will feel the spirit of entrepreneurship running through our veins."

At first glance, Schlachte's plans for ARC don't sound radically different from the course steered by ARC's previous CEO, Mike Gulett. However, *MPR* interviewed Schlachte after he had been on the job only two days, so we expect to see his strategy evolve.

optional code and data memories. (Choosing between instruction/data caches or on-chip code/data memories is a configuration option; designers who need deterministic performance usually prefer memories over caches.) For now, the 64-bit memory interfaces aren't configurable, but ARC says a future release of the ARC 700 will allow designers to revert to 32-bit interfaces. A future version will also support configurable 64- and 128-bit I/O interfaces on the optional X and Y data memories for DSP. Until then, the ARC 700's XY memories have 32-bit interfaces, as with previous ARC processors.

In other respects, the ARC 700 resembles the ARC 600 and ARCtangent-A5. The configurable register files, number of extension-instruction slots, cache options, and other customizable parameters are the same. The ARC 700 works with the same hardware- and software-development tools from ARC, including the ARChitect 2 graphical processor-configuration tool. It's compatible with the same peripheral soft-IP, such as ARC's USB 2.0 and Ethernet controllers. The ARC 700 also supports the same BVCI and AMBA bus interfaces as the ARC 600, allowing designers to integrate soft IP from other vendors and to reach timing closure more quickly by isolating the processor core on its own "island" within a larger design.

#### Higher Speed Comes At a Price

Although the ARC 700 remains one of the smallest 32-bit RISC cores on the market, the enhanced pipeline and other new features inevitably inflate the core's size and power consumption. The base configuration of the ARC 700—excluding caches and memories—totals about 100,000 gates. When fabricated in a 0.13-micron process, it will occupy about 0.56mm$^2$ of silicon and consume about 0.15mW per megahertz (60mW at the maximum frequency of 400MHz). In a 0.18-micron process, the core occupies about 1mm$^2$ of silicon and consumes about 0.5mW per megahertz (133mW at the maximum frequency of 266MHz).

In other words, you'll need a magnifying glass to find the ARC 700 core on an SoC, and it consumes only a little more energy than a mosquito. To put things in perspective, however, note that the 27,000-gate ARC 600 is a genuine miser. In a 0.13-micron process, the ARC 600 occupies only 0.15mm$^2$ of silicon and consumes 0.04mW per megahertz (11.6mW at its maximum frequency of 290MHz). In a 0.18-micron process, the ARC 600 occupies 0.27mm$^2$ of silicon and consumes 0.18mW per megahertz (36mW at the maximum frequency of 200MHz). Bottom line: the ARC 700 requires roughly four times the silicon area and power of the ARC 600 in any given IC process, but both cores are economical and efficient.

Still, chip designers can be obsessive about conserving silicon and power, no matter how tiny the amounts. The differences between the ARC 600 and ARC 700 are significant enough to justify keeping the ARC 600 in the product line for applications that don't need the ARC 700's higher performance. However, offering both cores could exacerbate a perennial problem at ARC: supporting an ever-growing collection of code bases.

In the past, each new processor core has required ARC to build and maintain at least four code bases: the Verilog and VHDL synthesizable models of the processor plus the instruction-set simulator and cycle-accurate simulator, which are additional representations of the processor written in C instead of a hardware-design language. On top of that, each new processor requires modifications to the ARChitect hardware-configuration tool, the MetaDeveloper software-development tools (assembler, linker, C/C++ compiler, and debugger), and miscellaneous other tools (the MetaSim system emulator, ARCangel FPGA development system, and more). ARC's peripheral IP may require some tweaking for a new processor, too.

Developing, maintaining, and upgrading this comprehensive product line is a difficult challenge for a company battered by the tech recession and layoffs. ARC is down to about 180 employees, from a peak of nearly 300 a few years ago. To make things even more interesting, ARC maintains a vast catalog of other products, some of which are unrelated to its central product line. Because of previous acquisitions, ARC sells software-development tools for non-ARC processor architectures (68K/ColdFire, ARM, MIPS, PowerPC, and XScale), system software (the MQS real-time operating system, network-protocol stacks, and other embedded middleware), and even some legacy 8- and 16-bit processor cores (V8086, V186, Turbo86, and Turbo186). Do the engineers at ARC ever sleep?

### ARC Begins a Long-Overdue Reorg

After losing tens of millions of dollars and shedding scores of employees in the past three years, ARC has finally realized that its business model is unsustainable. The company has announced a major reorganization that will phase out almost all unrelated products and make an independent operation out of the system-software business gained by acquiring Precise Software Technology in 2000. However, ARC will keep the MetaWare development-tool division in house, because it's vital for supporting the ARC processor architecture.

Another change is that the ARC 700 core is available only in Verilog, not in both Verilog and VHDL. Previously, U.K.-based ARC maintained two HDL models of its processors, because VHDL is more popular in Europe, and Verilog is more popular elsewhere. ARC says Verilog is gradually overtaking VHDL and is preferred by most new customers. Dropping VHDL eliminates a duplicate code base and yields some efficiencies, too: the ARC 700 requires 3–5% fewer gates in Verilog.

Both the reorganization and the ARC 700 are steps in the right direction. The big question about the reorg is whether it's too late to save the company from drastic downsizing or an acquisition by another party. ARC still has a great many customers (86 licensees with 141 design wins) and a strong cash position from its initial public offering in September 2000 (about $69 million at the end of 2003)—but the burn rate has been corrosive, and the company recently replaced its CEO. (See the companion article, "New CEO Brings Varied Background to ARC.") To compete effectively against rivals like ARM, MIPS, and Tensilica, ARC needs to divest itself of unprofitable sideline ventures and concentrate on its core technology.

The ARC 700 is a product worth keeping. Its ground-up redesign sweeps out cobwebs that have impeded the clock speeds of ARC's last three processors. In truth, though, clock frequency is an even more overrated metric for a configurable processor than for a desktop CPU. As EEMBC benchmarks of previous ARC processors and the Tensilica Xtensa V amply demonstrate, configurable processors can deliver far more performance with a few custom instructions than with any conceivable increase in clock frequency. And custom extensions often consume less power than simply cranking up the clock rate. (See *MPR 9/16/02-01*, "Tensilica Xtensa V Hits 350MHz," and *MPR 11/12/01-01*, "Configurable vs. Fixed Instruction Sets.")

There's more to come about the ARC 700. With nearly four times as many gates as its predecessor, the ARC 700 surely has some unannounced features lurking in its core. ARC promises to disclose more information about the microarchitecture at Embedded Processor Forum (May 17–20). Even so, judging from what the company has announced to date, the ARC 700 is a welcome upgrade of a field-proven configurable architecture. ◇

### Price & Availability

The ARC 700 is available now for IP licensing as a fully synthesizable Verilog model. The optional DSP extensions will ship in May. Up-front license fees and royalties are negotiable and not publicly disclosed. All development tools and peripheral IP available for the ARC 600 are compatible with the ARC 700 and are available now. For more information: *www.arc.com*.