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Media Processors Poised to Pounce

Digital Engines Power Next-Generation Consumer Electronics

By Tom R. Halfhill {2/9/04-13}

After years in the doldrums, consumer electronics is exciting again. Historically, this industry thrives on paradigm shifts: radio to television, black-and-white TV to color, stand-alone TVs to home entertainment centers, VCRs to DVDs, vinyl records to CDs, CDs to MP3s, wired telephones to wireless cellphones. Even perennial sellers like videogame consoles must be reinvented every few years to maintain their expected thrill level.

Now the consumer electronics industry is verging on more transitions. DVD players will soon give way to DVD recorders and personal video recorders (PVR), banishing the last unique feature of VCRs. CRT-based TVs, the final bastion of big vacuum tubes, seem increasingly old-fashioned next to flat-screen LCD and plasma displays. Single-function wireless phones are being replaced by multipurpose communicators that will serve as PDAs, text messengers, Web browsers, walkie-talkies, digital cameras, handheld game machines, and perhaps even videophones and TVs.

While sales of audio CDs decline, MP3 audio is going legit as major companies stampede into the music-download business. TV set-top boxes that are little more than passive channel tuners are yielding to TiVo-type devices that learn the owner's viewing preferences and automatically record shows to match. And, of course, the troika of videogame vendors (Sony, Nintendo, Microsoft) is preparing to launch the next generation of home consoles, which will trigger a surge of new sales.

Nowhere was the industry's excitement more evident than at the recent winter Consumer Electronics Show (CES) in Las Vegas. Attendance reportedly hit an all-time high, surpassing 129,000. In contrast, the fall Comdex show in Las Vegas drew about 50,000 attendees, down from a high of 211,000 in 1997. Although the computer industry is bouncing back from its worst-ever recession, the consumer electronics industry appears to be rebounding faster.

Fertile Ground for Media Processors

A vital difference between today's consumer electronics and the products of yesteryear is that almost every modern device contains at least one microprocessor—and often several other chips as well. Digital technology has spawned a huge market for embedded processors of every species, from tiny 8-bit microcontrollers to powerful 32-bit system-on-chip (SoC) processors and DSPs. It is also creating demand for new breeds of specialized media processors that can efficiently handle digital audio, motion video, high-resolution still images, and communication bitstreams.

Media processors were once known as multimedia processors, before "multimedia" became an unfashionable buzzword from the 1980s. Now, multimedia is making a comeback. Audio, video, and computer graphics are becoming vital features in cellphones, PDAs, handheld game machines, and other portable devices. At the same time, upper-echelon products like high-definition TVs, DVD recorders, PVRs, and advanced set-top boxes are driving demand for unprecedented amounts of media-processing power. Bottom line: What's good for consumer electronics is good for media processors.

Requirements for media processors vary widely, depending on the application. In battery-operated devices, small size and low power consumption are paramount. Higher-end AC-powered products that need strong performance can tolerate larger, hotter chips. As a result, media processors represent many different architectures and implementations. The only valid generalization is that media processors are better at media-specific tasks than are general-purpose processors at a similar price or power level.

As multimedia continues to pervade consumer electronics—a trend that varies with the business cycle but moves forward independently of it—the demand for media processors will climb. The only threats are ASICs, SoCs, and microprocessors that absorb media-processing functions with application-specific logic. That logic may come in the forms of fixed-function, hard-wired logic; runtime-reconfigurable logic; or a design-time-configurable architecture. Of course, media processors can use those technologies, too.

We nominated five **Media Processors** for our 2003 *Microprocessor Report* Analysts' Choice Awards. All the processors in this category are exceptional in some way. It's a tough category to judge, because the processors—designed for different applications—tend to be very different from each other. The five nominees are Equator Technologies' BSP-15; Intel's MXP5800; Motorola's MRC6011; Philips Semiconductor's TriMedia TM5250; and Silicon Hive's Avispa+.

Equator Redraws the MAP

Equator announced the **BSP-15** at Microprocessor Forum 2001 and began producing the chip in 2002, which makes it relatively aged for a media processor. The company announced a successor, the BSP-16, at Embedded Processor Forum 2003, but the new chip has been delayed and is ineligible for an award nomination this year. (See *MPR 7/28/03-04*, "Equator Revs Media Processor.")

Meanwhile, the BSP-15 remains the company's top-of-the-line media processor and is still competitive in the marketplace. Both the BSP-15 and BSP-16 are upgrades of the impressive MAP-CA, which won our Analysts' Choice Award for the Best Media Processor of 2000. (See *MPR 3/13/00-04*, "MAP-CA Ready for Prime Time.")

BSP stands for "broadband signal processor." The BSP-15 is a programmable SoC optimized for both signal processing and high-quality video. It can act as a host processor as well as a media processor, thereby reducing a system's total chip count. At 400MHz, the BSP-15 can execute 400 billion operations per second (BOPS). That's a peak number, naturally, based on the ideal full utilization of its proprietary VLIW/SIMD architecture. Even in real-world applications, however, the BSP-15 is a proven product that delivers strong performance, thanks to some dedicated logic on chip.

One special feature of the BSP-15 is a 2D video filter that accelerates zooming, format conversions, and other image-processing functions. Another feature is an on-chip 16-bit coprocessor that offloads the variable-length encoding and decoding of serial bitstreams. A display refresh controller (DRC) supports several different types of displays, including VGA, interlaced NTSC, and high-resolution progressive-scan monitors. Because the DRC can handle multiplexed image streams, the BSP-15 also supports picture-in-picture video and text overlays. There's even some dedicated logic for offloading DES and 3DES encryption/decryption from the CPU.

Moving data on and off chip is a particular challenge for media processors, which must keep up with streaming audio and video in real time. To that end, the BSP-15 has a specially designed 64-channel DMA controller with an 8KB buffer. I/O interfaces support ITU-R BT.656, MPEG2, I^2C, I^2S, IEC958, SDRAM, PCI, and 8-bit general-purpose I/O.

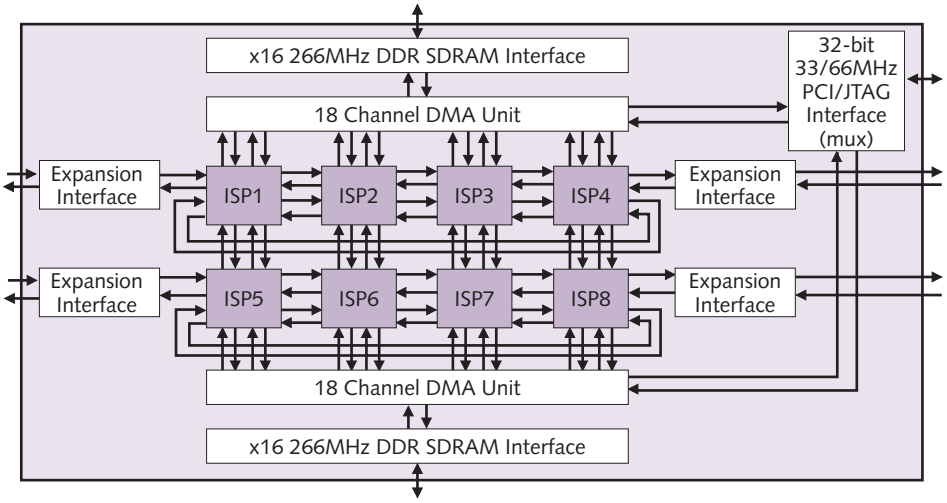

Figure 1. The MXP5800 is the more powerful member of Intel's new MXP family of media processors. The less expensive MXP5400 has only half the resources shown in this block diagram.

The BSP-15 has been around longer than other media processors nominated in this category, so it can boast of design wins, including Sony plasma TVs, Polycom videoconferencing systems, digital TVs, and MPEG-4 video servers/recorders.

As good as the BSP-15 is, however, we are looking forward to its postponed successor, the BSP-16, which is binary compatible with the BSP-15. New interfaces for 32/64-bit DDR-SDRAM and IDE will update the BSP-16 for the most recent embedded systems, and it will run

faster while consuming about half as much power (up to 500MHz, 1–2W typical). The big difference is a shrink from TSMC's 0.15-micron process to the 0.13-micron "G" process, which will drop the core voltage to 1.0V while maintaining 3.3V I/O (5V for PCI). We believe the BSP-16 will be a more formidable competitor against the other new media processors shipping in 2004.

Intel Caters to Xerox

The world's largest chip company is a newcomer to media processors, deciding to enter the fray in 2003 with a new parallel-processing architecture called MXP. The first two chips in the MXP family are the MXP5400 and **MXP5800**, and we deemed the more-powerful processor worthy of an award nomination. Intel's auspicious debut is sure to draw new attention to all types of media processors and liberate them from any lingering prejudice that they represent the lunatic fringe of microprocessor design. (See *MPR 10/27/03-02*, "Intel Enters Media-Processor Biz.")

Actually, Intel codeveloped the MXP architecture with Xerox, which is also the first customer for the chips. Although such close involvement with a customer in the development of an Intel microprocessor architecture is unusual, it is not unprecedented. Intel's partnership with Hewlett-Packard to develop the IA-64 architecture is the most notable previous example. As a result of the Intel-Xerox nexus, the first two MXP processors appear to be optimized for Xerox's applications, which may or may not coincide with the applications of other potential customers. Nevertheless, the MXP architecture is powerful and flexible, and we expect greater things from it in the future.

The target market for the MXP5800 is high-performance 16-bit-integer image processing. Xerox will use the chips to perform image enhancement, compression, and other imaging tasks in photocopiers, printers, scanners, and multifunction peripherals. As Figure 1 shows, the MXP5800 deploys eight image-signal processors in a rectangular array, plus a pair of 18-channel DMA controllers, two DDR-SDRAM controllers, and a 32-bit 33/66MHz PCI interface. Each signal processor contains five programmable processing elements and additional function units, all clocked at 266MHz. The DDR-SDRAM interfaces also transfer data at 266MHz.

Unlike the Equator BSP-15 and Philips TriMedia TM5250, the MXP5800 is primarily useful as a coprocessor, not as a standalone host/media processor. For example, the PCI interface can function only as a target for PCI transfers, not as an initiator. The system must have a separate host processor to control the MXP5800 and manage data transfers. Other clues also suggest an application-specific design that is probably perfect for Xerox but less suitable for different media-processing applications.

Despite the MXP5800's limitations, the MXP architecture shows great promise and appears unconstrained by the design tradeoffs in these first two implementations. Future MXP chips will probably offer stiffer challenges to competitors' more-mature media-processor designs.

Motorola Emphasizes Communications

Motorola's **MRC6011** is an unusual nominee for a media processor award, because it's more strongly oriented toward communications than are the other nominees in this category. Indeed, it could anchor a separate category for communications processors—if we had one this year. We've included the MRC6011 with the media processors because it deserves a nomination and because next-generation wireless phone networks will require crossover processors capable of handling media-rich datastreams.

The MRC6011 is a powerful processor that has a programmable RISC controller, six DSP cores, and integrated peripherals. Each DSP core contains no fewer than 16 function units. Although the MRC6011 is suitable for many compute-intensive applications, Motorola designed it primarily for baseband processing in 3G-cellular and wireless-LAN base stations. It's a programmable, standard-part alternative to an ASIC or conventional DSP. (See *MPR 7/14/03-01*, "Motorola Attacks ASICs.")

Figure 2 shows the basic microarchitecture of the MRC6011. This highly symmetrical design distributes the six DSP cores in two independent modules, each having its own input bus, DMA bus, and RISC controller bus. The RISC controller ties the DSP modules into the memory controllers and external DSP buses.

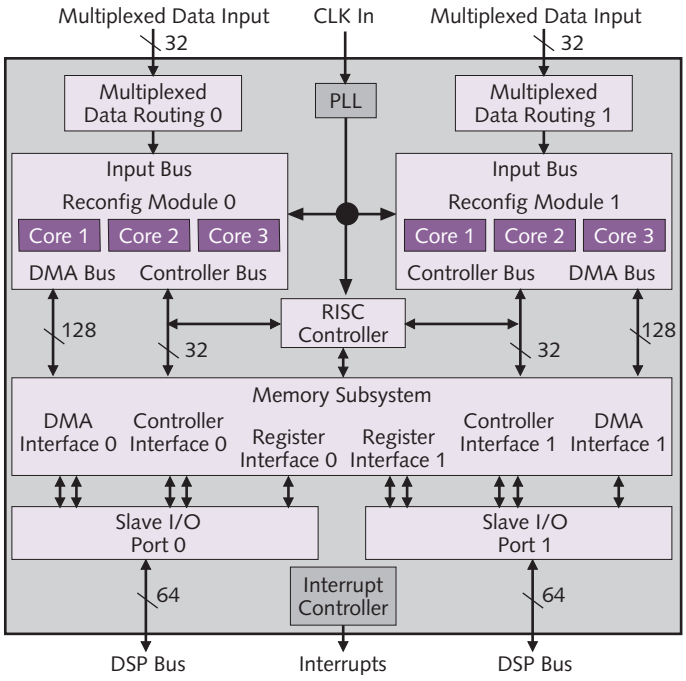

Figure 2. Motorola's MRC6011 is a super-DSP with its own RISC controller and memory controllers. The symmetry of the design suggests that future implementations could have only one DSP module for less-demanding applications or additional DSP modules for higher-end systems.

Media-Related Processors in 2003

In addition to the five media processors nominated for a *Microprocessor Report* Analysts' Choice Award, many other chips and cores related to media processing were announced or introduced in 2003. These include DSPs and hard-to-classify "extreme processors" for compute- or data-intensive applications, as well as general-purpose microprocessors and licensable CPU cores that may be suitable as control processors alongside a media processor or in a standalone role for media processing.

Analog Devices introduced its new TigerSHARC TS201S DSP, which has 3MB of embedded DRAM (see *MPR 7/14/03-02*, "TigerSHARC Swallows DRAM").

ARC International announced it will license a new configurable microprocessor core, the ARC 600, plus extensions and software codecs for digital audio (see *MPR 12/15/03-01*, "ARC Alters Trajectory").

Elixent introduced a massively parallel array processor, which is based on a proprietary D-Fabrix architecture and is licensable as a hard macro (see *MPR 7/21/03-01*, "Elixent Expands SoCs").

IBM decided to license PowerPC cores for manufacturing at any independent foundry, not just at IBM Microelectronics fabs. The first openly licensable PowerPC core is the PPC440 (see *MPR 3/31/03-02*, "IBM Opens Up PowerPC Licensing"). Later, IBM announced its first Customizable Control Processor, a PowerPC 405–based hard macro for SoC integration (see *MPR 6/23/03-02*, "IBM Offers SoC Head Start"), and a high-performance PowerPC processor, the 750GX, which runs at 1.1GHz and has 1MB of Level 2 cache (see *MPR 7/21/03-04*, "IBM Proliferates 750 Family").

Infineon announced new multithreading extensions for its DSP/microcontroller TriCore 2 processors (see *MPR 9/8/03-01*, "Two Threads for TriCore 2").

Intrinsity introduced the MIPS32-compatible FastMath and FastMIPS processors at 2GHz (see *MPR 1/6/03-01*, "Intrinsity Delivers On Its Promise") and later announced slightly slower and lower-power versions of the chips (see *MPR 5/27/03-03*, "Update on Intrinsity Fast Products").

MathStar announced a line of configurable array processors based on the company's Field Programmable Object Array architecture (see *MPR 12/15/03-03*, "Roll Your Own Array Processor").

MediaQ announced three members of its new Katana family. Each chip integrates an ARM core, a graphics engine, multimedia processing, and Java acceleration (see *MPR 8/18/03-02*, "MediaQ's Silicon Katana").

MIPS Technologies introduced the Pro Series cores, which add some design-time configurability to MIPS32 synthesizable processors (see *MPR 3/3/03-01*, "MIPS Embraces Configurable Technology") and announced more details about its MIPS32 24K processors (see *MPR 10/20/03-03*, "MIPS Reveals 24K Core Family").

Motorola introduced two high-performance PowerPC embedded processors at 1.3GHz: the MPC7447 and MPC7457 (see *MPR 3/10/03-03*, "Motorola Processor Cools Down"). Later, Motorola announced the MRC6011, a new chip that has a programmable RISC controller, internal peripherals, and six DSP cores (see *MPR 7/14/03-01*, "Motorola Attacks ASICs"), and the StarCore SC140e, an improved high-performance DSP (see *MPR 10/20/03-01*, "Motorola Enhances StarCore DSP").

NeoMagic announced the MiMagic 6, a new type of multimedia and graphics accelerator for smart cellphones, wireless PDAs, and multimedia PDAs (see *MPR 6/17/03-01*, "New Magic in MiMagic 6").

PicoChip announced the massively parallel PC101, which has 430 16-bit processors on a single chip (see *MPR 7/28/03-02*, "PicoChip Preaches Parallelism"), and the PC102, which has 344 processors, including 260 with multiply-accumulate (MAC) units (see *MPR 10/14/03-03*, "PicoChip Makes a Big MAC").

StarCore LLC announced the first two licensable StarCore DSP cores, the SC1200 and the SC1400 (see "StarCore LLC Offers Soft DSPs," a companion article to *MPR 10/20/03-01*, "Motorola Enhances StarCore DSP").

Tensilica announced a new software-analysis and hardware-generation tool that can automatically generate optimized instruction extensions for its configurable Xtensa V microprocessor core (see *MPR 6/23/03-01*, "Tensilica's Software Makes Hardware"). Later, Tensilica announced new extensions and software codecs for digital audio (see *MPR 9/29/03-01*, "Tensilica Makes Music").

Texas Instruments introduced two 'C55x-series DSPs with some microcontroller features (see *MPR 1/21/03-02*, "TI DSPs Play the Limbo Game"). A few months later, TI introduced its fastest MS320C64x-series DSP at 720MHz (see *MPR 4/28/03-02*, "C64x DSP Gets Performance Boost") and announced that a 1GHz version would sample in early 2004 (see *MPR 5/19/03-02*, "TI DSP Leapfrogs TI DSP").

Transmeta introduced embedded versions of its x86-compatible Crusoe processors (see *MPR 1/13/03-01*, "Transmeta Charges the Embedded Market").

Motorola describes the MRC6011 as a reconfigurable processor, but we prefer to call it reprogrammable. There is no reconfigurable logic as found in an FPGA. Instead, the "reconfigurable" elements are the DSP cores, which have their own local registers, memories, and function units. Their autonomy allows the DSPs to execute all or part of an algorithm locally, without fetching instructions from global memory. Once programmed, the MRC6011 can work almost as efficiently as a fixed-function ASIC, except that it's more flexible than an ASIC because the programming can change. Nevertheless, we reserve the term "reconfigurable" for devices having true reprogrammable gates. (See *MPR 7/14/03-01*, "Defining Reconfigurable Processing," the companion article to "Motorola Attacks ASICs".)

When they are fabricated in a 0.13-micron process, production examples of the MRC6011 are expected to run at a maximum clock rate of 250MHz at 1.2V. Power consumption is less than 3W (typical), so it's serious competition for less-integrated solutions built around conventional DSPs and separate ASICs. However, evaluating the MRC6011's performance will be difficult, owing to the scarcity of standardized benchmarks for such a specialized processor. Potential customers will probably have to conduct their own lab tests, using samples of the chip.

Philips Updates a Seminal VLIW Architecture

Since 1987, Philips has pioneered the evolution of very long instruction-word (VLIW) microprocessor architectures. The Philips TriMedia architecture was an outgrowth of that early work and debuted in 1994. Ten years later, TriMedia is still going strong, and the **TM5250** media-processor core is the newest member of the family. Announced at Microprocessor Forum 2003, the TM5250 is designed for PVRs, HDTVs, wireless networking, and other audio/video products. (See *MPR 11/3/03-01*, "Philips Powers Up for Video.")

Not that there haven't been bumps on the road. In 2000, Philips created a spinoff company—TriMedia Technologies—to offer the TriMedia architecture as licensable intellectual property (IP). As luck would have it, the new venture opened for business just in time for the worst tech recession in history. In 2002, Philips gave up and reabsorbed TriMedia into the parent company. (See *MPR 5/19/03-03*, "TriMedia Comes Home.") Consequently, the synthesizable TM5250 core is not available as licensable IP. Instead, Philips is designing around the TM5250 a chip that will be available later this year.

The TM5250 offers several improvements over the TriMedia CPU core in the Nexperia PNX1300, the existing top-of-the-line media processor from Philips. Superpipelining helps to boost the worst-case core clock frequency to 500MHz (assuming a standard TSMC 0.13-micron process), which is more than twice as fast as the PNX1300 is. Philips created nine new instructions for video processing, improved the L1 caches, added an on-chip L2 data cache, improved the prefetching mechanism, added dynamic branch prediction, and endowed the TM5250 with a larger array of function units that can keep as many as 29 pending instructions in flight.

Figure 3 is a diagram of the new pipeline. At its deepest, the pipeline extends to 16 stages, compared with a maximum of seven stages in the PNX1300. An oddity of this pipeline is that it takes nine stages just to fetch and decode the instructions, due to cache way-prediction and the compressed format of the VLIW instructions. Dynamic branch prediction helps avoid the penalty of taken branches in such a deep pipeline.

According to early benchmarks comparing the TM5250 with the PNX1300, the new core's media-processing performance roughly scales with its increase in clock frequency. Before questioning the value of all the improvements to the microarchitecture, keep in mind that scaling performance with clock speed is a challenge for an architecture as mature as TriMedia. In reality, the higher clock rate would be impossible without the enhancements, because the shorter pipeline of the PNX1300 is a bottleneck. In addition, Philips hasn't yet rewritten its media codecs to take advantage of the TM5250's new features, so the benchmark scores can only improve.

Indeed, the benchmarks indicate that TriMedia processors are already highly optimized for media processing, and that new designs like the TM5250 are doing a good job of keeping the TriMedia architecture competitive against newer and more-extreme architectures.

Silicon Hive Pursues Parallelism

Like the Philips TriMedia TM5250, Silicon Hive's **Avispa+** is a synthesizable processor core, not an off-the-shelf chip. However, while Philips has decided not to license the TM5250 to outside companies, the Avispa+ is licensable IP, so anyone can design a chip around it. Silicon Hive's goal is

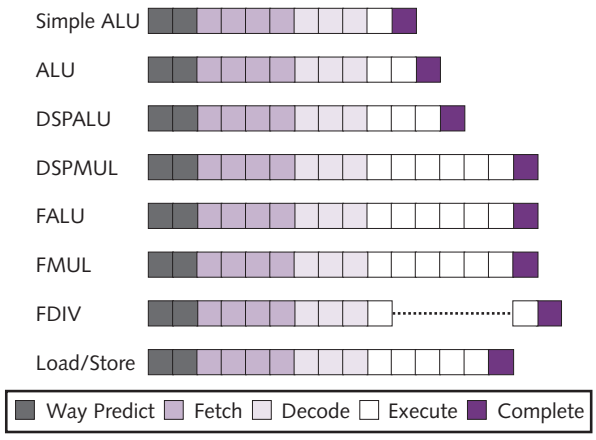

Figure 3. The first two stages in the TM5250 pipeline are required for way prediction when fetching instructions from the eight-way set-associative instruction cache. It takes four stages to fetch and decompress the VLIW instructions, then three more stages to decode them. A nonpipelined function unit carries out floating-point divides and square roots.

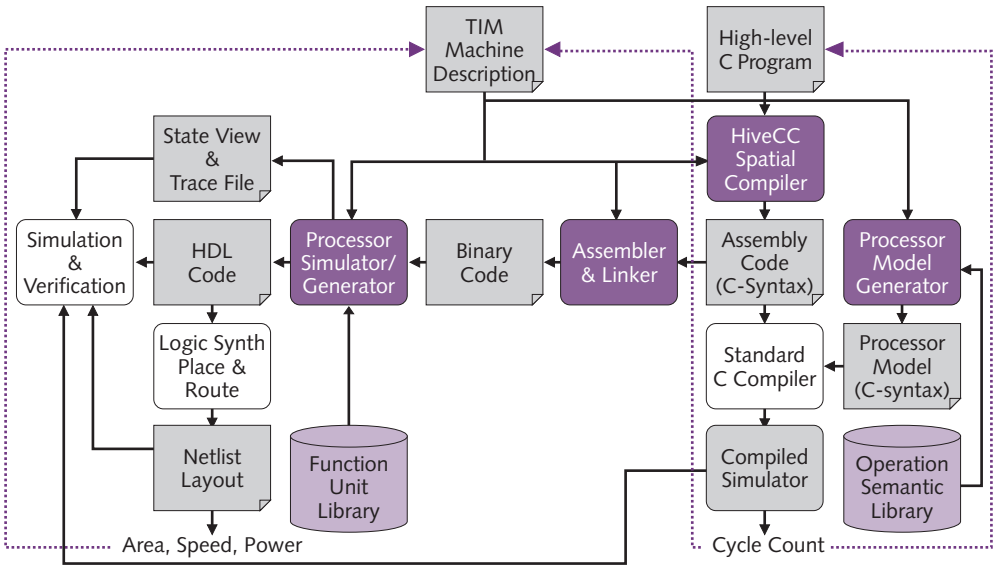

Figure 4. Feedback from an integrated tool chain helps the architect customize a ULIW-based design for a particular application by modifying the microarchitecture and instruction set. Avispa+ is one example of a processor core designed with this system; Silicon Hive can generate additional implementations on demand.

to build a profitable business by licensing media-processor cores to SoC developers, something Philips recently failed to do with TriMedia. This strategy is interesting because Silicon Hive is not only bucking the bleak history of media-processor licensing, but is also a Netherlands-based startup funded and owned by Philips Electronics. (See *MPR 12/1/03-02*, "Silicon Hive Breaks Out.")

Although both Avispa+ and the TriMedia TM5250 are synthesizable media-processor cores, the similarity ends there. TriMedia processors are based on a VLIW architecture at least 10 years old, while Avispa+ has a radical new ULIW (ultra-long instruction word) architecture. The "ultra" label isn't just marketing gibberish. Avispa+ instruction words are 768 bits long, and they may contain scores of operations for parallel execution. When this ULIW processor achieves its full potential for parallel issue, the peak performance is astounding: nine billion operations per second at a clock frequency of only 150MHz. It's also a highly efficient core, occupying only 4mm^2 of silicon and consuming only about 150mW (worst case) when fabricated in a 0.13-micron CMOS process.

Avispa+ is designed for signal processing in orthogonal frequency-division multiplexing (OFDM) radio applications, but it's suitable for other compute- and data-intensive tasks. Silicon Hive wants to replace some of the general-purpose processors, ASICs, and DSPs in high-performance embedded systems with a programmable ULIW SoC. However, the system may still require a general-purpose processor to run the operating system and handle other control tasks.

Particularly intriguing is the tool chain Silicon Hive has developed for the ULIW architecture. As Figure 4 shows, the architecture is configurable and uses compiler feedback from a cycle-accurate simulator to help generate an optimized design for the target application. This aspect of the architecture resembles the configurable-IP processors licensed by ARC International, MIPS Technologies, and Tensilica, except that Silicon Hive's configurable architecture is intended for compute-intensive, parallel-execution signal processing. Actually, Silicon Hive would be equally competitive in the IP-core or extreme-processor award categories, as well as in the media-processor category.

Silicon Hive has created an impressive processor architecture and configuration system. However, despite some helpful data supplied by the company, *MPR* remains skeptical that such an extreme architecture will fulfill its potential in actual applications. One drawback of VLIW architectures is their inability to extract as much instruction-level parallelism from real-world program code as the processor can support, forcing the compiler to fill unusable instruction slots with placeholder NOP instructions. A ULIW architecture with 60 issue slots per instruction word would seem even more susceptible to this problem. Silicon Hive claims its proprietary compilers have achieved a breakthrough in instruction-level parallelism. Although genuine breakthroughs are rare, perhaps Silicon Hive has indeed found the key—at least for some narrow applications.