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ClearSpeed Hits Design Targets

Early Samples of Floating-Point Coprocessors Are Fast, Power-Efficient

By Tom R. Halfhill {1/12/04-02}

ClearSpeed Technology has successfully tested early production samples of its CS301 floating-point coprocessor and is delivering small quantities to prospective customers. The massively parallel chip is hitting all its design targets for clock frequency (200MHz), power consumption (less than 2W), and peak floating-point performance (25.6 GFLOPS).

In addition to offering the CS301 as a standard part, U.K.-based ClearSpeed has decided to license the processor's synthesizable Verilog model for customers wishing to design their own chips. The model is configurable, so customers can determine the number of parallel-processing elements, the number and type of function units, and the amount of on-chip memory.

MPR visited ClearSpeed's small U.S. office in Los Gatos, California, shortly before Christmas to observe some math-intensive software running on the CS301, which was unveiled at Microprocessor Forum 2003. (See *MPR 11/17/03-01*, "Floating Point Buoys ClearSpeed.") The company has produced a small number of evaluation boards, with two CS301 chips per PCI board.

Using three of those boards and special drivers, ClearSpeed demonstrated an ordinary PC executing up to 30 GFLOPS. Although that performance is considerably less than the peak capability of 153.6 GFLOPS for six CS301 chips, it is respectable performance when all six coprocessors must share the same 133MB/s PCI bus. Production boards will allow more coprocessors per board and will have a PCI-X interface; larger systems can use any number of boards.

Testing Drugs Without a Test Tube

One of ClearSpeed's demos is a drug-screening simulator based on software from the University of Bristol, England. This "drug-docking" program tests the interactions of a candidate

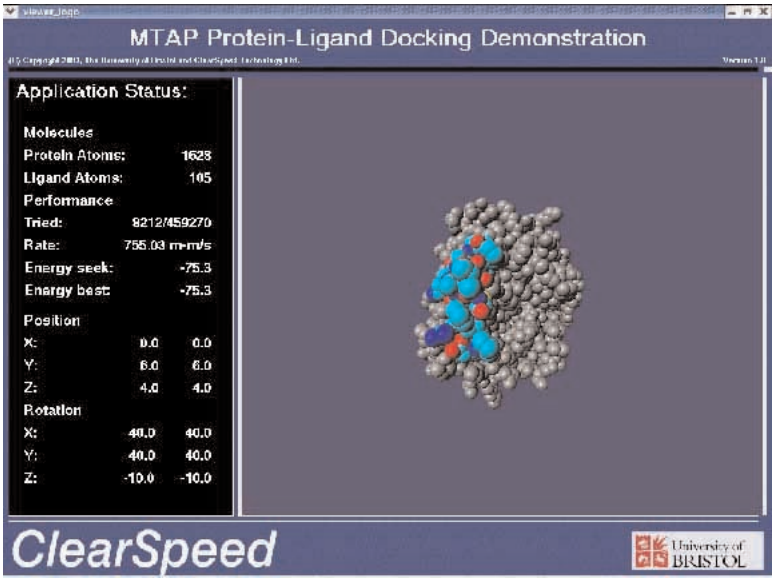

Figure 1. ClearSpeed created this demo by porting a drug-simulation program from the University of Bristol. The dark mass in the background of the image is a target protein; the lighter mass in the foreground is the ligand of a candidate drug.

drug against a target protein by trying to fit the atoms of the drug's ligand into the receptor atoms of the protein molecule. Simulating the interaction *in silico* allows much faster testing than does *in vitro* screening with test tubes or petri dishes.

When the drug-docking program runs on a 2.8GHz Intel Xeon without a CS301 coprocessor, it can test about eight million protein-ligand interactions per second. With six CS301 coprocessors on three PCI boards, the same system can test about 124 million interactions per second. Figure 1 shows a screen photo of this program in action.

Another ClearSpeed demo shows a single CS301 applying a fast Fourier transform (FFT) algorithm to about 100,000 datasets per second, sustaining about 5 GFLOPS. (The algorithm uses a 1,024-point complex, 32-bit floating-point Radix-2 FFT.) When running on six CS301 coprocessors on three PCI boards, the same demo executes about 586,000 FFTs per second, sustaining about 30 GFLOPS. Although that performance is well below the theoretical peak of 153.6 GFLOPS for six chips, it shows good consistency when scaling from one coprocessor to six coprocessors. Even more impressive is that power consumption peaks at less than 2W per chip.

Formal Benchmarking Will Be Difficult

Unfortunately, there are no industry-standard benchmark results for the CS301 yet, mainly because ClearSpeed has been testing customer applications. Furthermore, the most popular industry-standard benchmarks are unsuitable for the CS301.

For example, SPEC's floating-point benchmarks are ruled out because SPEC forbids source-code modifications. Unmodified ANSI C code will run on the CS301, but ordinary code won't take advantage of the chip's massively parallel array of processing elements. Programmers must modify variable declarations and functions so ClearSpeed's proprietary C compiler can emit executable parallel code.

Another obstacle to running SPEC benchmarks on the CS301 is that some tests require a Fortran compiler, which is not yet available for the CS301. The University of Bristol's drug-docking program is written in Fortran, so ClearSpeed had to port about 100 lines of the most math-intensive code to C.

EEMBC benchmarks aren't very useful with the CS301, either. Although EEMBC does allow vendors to modify source code for its optimized "full-fury" benchmarks, the EEMBC suites contain relatively little floating-point math and don't focus on scientific computing. A better candidate, perhaps, would be the NASA Advanced Supercomputing (NAS) parallel benchmarks. NASA's Ames Research Center in Silicon Valley developed the NAS benchmarks for scientific computing, and vendors are allowed to modify the source code.

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