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ARM Expands ARM11 Family

Significant New Features to Debut in ARM1156 and ARM1176 Cores

By Tom R. Halfhill {1/5/04-01}

ARM's latest synthesizable processor cores will introduce several eagerly anticipated features when they ship to licensees in the second quarter of the new year. Enhancements cover the gamut from security and power management to code compression and on-chip I/O.

It's a significant growth spurt for the youthful ARM11 family, which will celebrate only its second birthday in 2004.

Two new series of cores will join the ARM11 family in 2Q04: the ARM1156 and the ARM1176. Each series has two cores: the ARM1156T2F-S and ARM1156T2-S, and the ARM1176JZF-S and ARM1176JZ-S, respectively. All four are 32-bit synthesizable embedded-processor cores based on the progenitors of the ARM11 family, the ARM1136JF-S and ARM1136J-S, which first appeared in 2002.

The parentage is significant, because *MPR* considers the ARM1136JF-S to be among the best in its class—which is the reason it won the *MPR* Analysts' Choice Award for 2002 in the category of soft intellectual-property (IP) processor cores. In fact, we have renominated the ARM1136JF-S in the same category for the 2003 awards, because it's still very competitive. (See *MPR 12/15/03-02*, "Awards Nominees Announced.") The new ARM11 cores are ineligible for a 2003 award because they didn't sample or ship before the end of the year.

Decoding ARM Nomenclature

ARM watchers can divine some features of the new ARM11 cores by decoding their product names—which, despite the rumors, are not randomly assigned by the Department of Motor Vehicles.

The "ARM11" prefix, of course, identifies all four new cores as members of the ARM11 family, the most advanced generation of the ARM architecture. All ARM11 processors share several characteristics: the ARMv6 instruction-set architecture (ISA); an eight- or nine-stage instruction pipeline (the longest ARM); a load/store unit that allows out-of-order completion; an integral DMA controller; DSP extensions; and a combination of static and dynamic branch prediction. In addition, all ARM11 cores announced to date have the "-S" suffix, which indicates they are synthesizable. (See *MPR 6/3/02-01*, "ARM Family Expands at EPF.")

At this point, the new cores part ways with one another. Both ARM1156 cores have the "T2" designation, which means they support the Thumb-2 instruction extensions. Thumb-2 is an enhanced version of the Thumb instruction subset, which allows programmers and compilers to save memory by substituting 16-bit instructions for some 32-bit instructions. However, neither of the new ARM1176 cores supports Thumb-2; they continue to use Thumb-1. Because Thumb-2's variable-length instructions require extra decoding, the ARM1156 has a nine-stage pipeline, one stage longer than the ARM1136 and ARM1176. (See *MPR 6/17/03-02*, "ARM Grows More Thumbs.")

One core in each new series—the ARM1156T2F-S and the ARM1176JZF-S—boasts the "F" designation, which means they have an integral FPU for floating-point and vector arithmetic. The integral FPU is more efficient than an auxiliary FPU attached to the coprocessor interface. ARM introduced the integrated FPU with the ARM1136FJ-S in 2002. (See *MPR 10/21/02-02*, "MPF Hosts Premiere of ARM1136.")

The ARM1136 and ARM1176 series also carry the "J" designation, which stands for Jazelle, ARM's Java extensions.

(See *MPR 2/12/01-01*, "Java to Go: Part 1.") The ARM1156 cores, which lack the "J," don't support Jazelle. ARM says the deeply embedded applications for which the ARM1156 cores are designed—such as hard-disk-drive controllers—don't need Java. That's true in many cases, but Java is rapidly gaining popularity in all kinds of embedded applications, so the omission of Jazelle in the ARM1156 will steer some customers toward the other ARM11 cores.

Finally, both ARM1176 cores have the brand-new "Z" moniker, which could indicate a power-saving sleep mode (as in "catching Zs") but instead announces their support for the new TrustZone security extensions. (See *MPR 8/25/03-01*, "ARM Dons Armor.") Indeed, the ARM1176 cores are the first processors to support TrustZone, which upgrades the ARMv6 ISA to ARMv6Z. Table 1 sorts everything out by comparing features of the four new ARM11 cores with the two existing ARM1136 cores.

New AMBA Bus and Power Management

Three important features not encoded in the product names are the AMBA 3.0 system-bus interface, also known as the Advanced eXtensible Interface (AXI); the Intelligent Energy Manager (IEM); and the memory-management unit (MMU). All four new cores have AXI, leaving the ARM1136 series as the only ARM11 processors with the older AMBA 2.0 interface. (See *MPR 6/17/03-03*, "ARM Makes Bus Announcement.") In addition, both new ARM1176 cores support IEM, the dynamically variable voltage-and-frequency technology developed by ARM and National Semiconductor. (See *MPR 1/21/03-01*, "Analog and CPU Wizards Reduce Digital Power.") However, only the ARM1136 and ARM1176 have a full-fledged MMU. The ARM1156 has a stripped-down MMU that provides memory protection but not address translation. Like Jazelle, the full-featured MMU was omitted from the ARM1156 to save gates in deeply embedded applications.

ARM's estimated clock speeds for the ARM11 family are impressive, especially for fully synthesized designs. Simulations and early test chips indicate that the ARM1176 should reach the upper end of its range—550MHz—when fabricated in the fastest available TSMC 0.13-micron CMOS process (CL013LV OD FSK) with low-*k* dielectrics and Artisan HS (high-speed) libraries. Without the low-*k* dielectrics (TSMC CL013LV OD), ARM expects the ARM1176 to hit 500MHz. In TSMC's less-aggressive CL013LV process, the ARM1176 should still attain 450MHz. In TSMC's generic 0.13-micron process (CL013G), test chips are running at 333MHz, using Sage-X libraries, and at 370MHz, using Sage-HS libraries. The performance of other ARM11 cores should be close to these ARM1176 results, because their microarchitectures are very similar.

Power consumption is equally impressive for such high-performance cores. ARM originally estimated the ARM1136 would consume about 1.0mW per megahertz when fabricated in a generic 0.13-micron process. After using the Synopsys Power Compiler to help optimize the design, ARM now believes the ARM1136 will consume about 20% less power than the original estimate, or 0.8mW per megahertz. This revised estimate is based on experience with an early ARM1136 test chip.

Simulations of the ARM1176 indicate its power consumption will be about the same as that of the ARM1136, or slightly lower. Although ARM hasn't publicly estimated the power consumption of the ARM1156 cores, they should consume a little less than the ARM1136 and ARM1176, because they lack an MMU and Jazelle extensions. Note that power estimates for the ARM1176 don't consider the savings made possible by dynamically reducing the core frequency and voltage using IEM.

ARM hasn't yet released any certified EEMBC benchmark scores for the ARM11 family but plans to do so for the ARM1176 in 2004. Until then, a rough indicator of actual performance is the hoary Dhrystone 2.1 benchmark. In simulation, the ARM11 processors deliver about 649–743 Dhrystone mips at 550MHz.

Feature	ARM 1156T2F-S	ARM 1156T2-S	ARM 1176JZF-S	ARM 1176JZ-S	ARM 1136JF-S	ARM 1136J-S
Architecture	ARMv6	ARMv6	ARMv6Z	ARMv6Z	ARMv6	ARMv6
Arch Size	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
Pipeline Depth	9 stages	9 stages	8 stages	8 stages	8 stages	8 stages
DMA Controller	Yes	Yes	Yes	Yes	Yes	Yes
Integral MMU	No	No	Yes	Yes	Yes	Yes
DSP Extensions	Yes	Yes	Yes	Yes	Yes	Yes
Branch Prediction	Static/ Dynamic	Static/ Dynamic	Static/ Dynamic	Static/ Dynamic	Static/ Dynamic	Static/ Dynamic
Thumb (16b instr)	Thumb-2	Thumb-2	Thumb-1	Thumb-1	Thumb-1	Thumb-1
Integral FPU	Yes	No	Yes	No	Yes	No
AMBA 3.0 AXI	Yes	Yes	Yes	Yes	No	No
TrustZone	No	No	Yes	Yes	No	No
IEM Extension [1]	No	No	Yes	Yes	No	No
Jazelle (Java)	No	No	Yes	Yes	Yes	Yes
Synthesizable	Yes	Yes	Yes	Yes	Yes	Yes
Core Freq [2]	333–550MHz	333–550MHz	333–550MHz	333–550MHz	333–550MHz	333–550MHz
Dhrystone 2.1	450–743 mips	450–743 mips	400–660 mips	400–660 mips	393–649 mips	393–649 mips
Power (mW/MHz)[3]	<0.8	<0.8	0.8	0.8	0.8	0.8
Availability	2Q04	2Q04	2Q04	2Q04	2002	2002

Table 1. ARM's new processor cores triple the size of the ARM11 family. The ARM1156 and ARM1176 cores offer significant improvements over the award-winning ARM1136, which isn't even two years old. [1]IEM: Intelligent Energy Management for dynamic voltage/frequency scaling. [2]Based on simulations and early test chips in various 0.13-micron digital CMOS fabrication processes. [3]Includes miscellaneous memories, such as the main cache RAMs and translation lookaside buffer (TLB).

ARM Family Needs Birth Control

As the numerous back-issue references in this article indicate, *MPR* has thoroughly covered all the new technologies in the latest ARM11 cores, which are the first to implement AXI, IEM, Thumb-2, and TrustZone. It's remarkable that ARM has introduced so many architectural innovations less than two years after the ARM11 made its debut in 2002. We have no doubt customers will welcome the new processor cores and features.

Our only concern is the rapid proliferation of ARM cores and the compromises they impose. Gone are the days when ARM offered a basic 32-bit embedded RISC processor in any color the customer wanted, as long as it was black. Today, ARM has so many different processor cores, and so many architectural extensions and enhancements, the company must churn out an increasing number of very similar cores in an attempt to offer the optimum combinations of features customers desire. Inevitably, some customers will have to settle for a suboptimal combination.

For example, it's easy to imagine a low-power, small-memory embedded application that can benefit from the power efficiency of dynamic voltage/frequency scaling and the code efficiency of enhanced 16-bit instructions. So far, however, ARM doesn't offer a processor core with both IEM for lower power consumption and Thumb-2 for greater code density. To get Thumb-2, the customer must choose an ARM1156 core; to get IEM, the customer must choose an ARM1176. Likewise, a customer wishing to implement security features with the TrustZone extensions must license an ARM1176 core, which rules out Thumb-2. For hardware-accelerated Java performance, customers must choose the ARM1136 or ARM1176, because the ARM1156 doesn't support Jazelle.

ARM will probably address the dilemma by introducing more new ARM11 cores that roll up all the latest features. This raises the specter of a core named the ARM-1196IEMT2AXIJZF-S, which will also need a checksum so customers can be sure they're ordering the right SKU.

There's a better solution: configurability. One basic ARM11 core with modular extensions would allow each customer to design its own ARM11 processor, cafeteria style. ARC International, MIPS Technologies, and Tensilica already offer this degree of configurability and much more. ARM needn't go as far as those companies by letting customers tinker with low-level architectural details, such as instructions, registers, buses, and the like—although EEMBC benchmarks show it's a way of achieving superlative performance. Merely by providing a configuration tool that allows each SoC developer to assemble its own ARM core out of modular synthesizable building blocks, ARM could slim down its product line and give customers greater flexibility.

Even without configurability, the ARM1156- and ARM1176-series processor cores are worthy additions to the elite ARM11 family. By bringing advanced power management, TrustZone security extensions, Thumb-2 instructions, and the AMBA 3.0 AXI bus to market, they will strengthen ARM's position as the leading provider of 32-bit embedded-processor cores.

Price & Availability

Licenses for the ARM1156- and ARM1176-series processor cores are available now, but the synthesizable models won't ship until 2Q04. ARM1136-series cores have been shipping since late 2002. ARM does not publicly disclose licensing fees, royalty rates, or terms. For more information, see *www.arm.com*.