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Sonics Gains Acceptance

On-Chip Interconnect Wins Customers, Promotes Standards

By Tom R. Halfhill {12/22/03-01}

Since its founding in 1997, Sonics has been gradually establishing its on-chip interconnect technology among important customers like Broadcom, Flextronics, Fujitsu, Hitachi, Hughes, Intel, NASA, NEC, Nokia, Samsung, Texas Instruments, and Toshiba. Last fall, TI licensed additional Sonics technology for its OMAP wireless-communication processors, and an industry-standards body adopted the core-interface protocol backed by Sonics.

Sonics is gaining acceptance by attacking several problems that face today's chip designers. One is the growing complexity of SoCs and ASICs: higher integration usually confers a competitive advantage, but integrating dozens of processor cores, peripherals, and memories on a single chip is a difficult job. Meanwhile, engineers are under more pressure to reduce time-to-market delays by finishing their complex chip designs sooner. Soaring engineering costs and expensive mask sets are encouraging more design reuse and synthesis, but on-chip interconnects tend to be less efficient in synthesized designs than in full-custom layouts.

Software designers faced similar problems years ago. To make their growing projects more manageable, they have adopted object-oriented programming languages with class libraries and standardized APIs that can integrate many different software components—whether those components are written from scratch, licensed from a third party, reused from a previous project, or invoked over a network. Hardware design is following the same general path. Numerous companies now license ready-to-use intellectual property (IP) in the forms of hard macros or synthesizable processors and peripheral cores. Integrating IP from different vendors isn't a straightforward task, however, because the on-chip interfaces are so variable.

Sonics stands at the intersections between those IP components. Its own licensable IP consists of switched-fabric interconnects, sockets, and design tools for integrating other vendors' core IP on SoCs. Sonics' latest product is SiliconBackplane III, a new version of its interconnect fabric. SiliconBackplane III isn't just another bus that competes with ARM's AMBA, IBM's CoreConnect, and similar buses for core IP. Instead, it's a micronetwork with some native intelligence that can work with any core-IP interface. Companion products include Synapse 3220 Peripheral Interconnect IP (introduced in 2002), MemMax Memory Scheduler IP (introduced at Microprocessor Forum 2001), and Sonics Studio, an SoC design-integration tool.

The company received a major boost in October when the core-interface protocol it supports was adopted by an important industry-standards body, the Virtual Socket Interface Alliance (VSIA). VSIA endorsed the Open Core Protocol (OCP)—which is controlled by the OCP International Partnership, an independent trade organization—as a standard socket for connecting on-chip components. Sonics is a long-time supporter of OCP and uses the socket to connect IP cores to its SiliconBackplane III, Synapse 3220, and MemMax products. VSIA's adoption of OCP will expand the amount and variety of licensable IP that plugs into the Sonics interconnects without any special design effort.

Optimizing Multimedia Chips

SiliconBackplane III introduces new features for multimedia SoCs. Sonics sees an expanding market for multimedia chips in digital TVs, set-top boxes, personal video recorders, and

other consumer products that must handle streaming video and 2D graphics. Video processing complicates the design of on-chip interconnects because it increases the demand for bandwidth and requires the chip to process larger data-streams in real time. To meet the quality-of-service requirements of video, the chip may have to process multiple video frames in parallel, moving more data between various parts of the chip and the memory subsystem.

Previous versions of the Sonics micronetwork supported burst data transfers, but SiliconBackplane III has improved "burst agents"—the interfaces between the fabric and the OCP sockets. These agents can manage data transfers more efficiently by combining multiple data requests from an initiator (such as a processor core or MPEG decoder) into a single extended-burst transfer across the fabric. At the receiving end, the memory-interface agent converts the burst transfer into the appropriate memory requests. The memory agent then returns the data to the initiator as another extended burst across the fabric. Although the burst agents and interconnect fabric inevitably add some gate delays to the datapath, Sonics says the overhead is less than 10% and is less significant than the arbitration latencies between the initiators and the memory.

The new burst agents also support block transfers of 2D graphics data. The agents can access noncontiguous blocks of memory—common in video frame buffers—by automatically translating the target memory address according to the width, height, and stride that defines the block. The burst agents can group related requests together so the MemMax scheduler, which optionally connects to the DRAM controller, can schedule the requests more efficiently. MemMax strives to keep memory pages and banks open while accessing the blocks, thereby reducing the latency of opening and closing the memory.

Because SoC developers can configure the burst agents for different purposes, the number of gates an agent adds to a design varies. Sonics says the average size of a burst agent is about 2,500 gates. One agent is required for each node on the SiliconBackplane III micronetwork that needs high bandwidth. (A node might be a processor core, a high-speed peripheral core, or a custom function block.) Sonics says the SiliconBackplane III fabric and burst agents can sustain data throughput of 4GB/s in any direction.

Flexible Bandwidth Allocation

Using the Sonics Studio design tools, SoC developers can specify the amount of bandwidth a core or function block needs. When the design is synthesized, the fabric has the necessary intelligence to guarantee the amount of bandwidth required for each initiator, using a time-division multiple-access (TDMA) protocol. The protocol can also be programmable at run time, allowing the bandwidth allocation to change on the fly.

To meet the demands of hard real-time applications, any initiator can become the highest-priority node at any time. The fabric distributes any unused time slots among the other initiators in a round-robin fashion.

Peripheral cores or function blocks that don't need the high-bandwidth features of the burst agents can hook into the SiliconBackplane III micronetwork, using ordinary OCP agents. The lowest-bandwidth peripheral nodes—UARTs, keyboard ports, USB controllers, smartcard slots, wireless transceivers, and the like—can attach to the Synapse 3220 micronetwork. This lower-power, lighter-weight interconnect is designed for large numbers of low-bandwidth peripherals scattered around a chip. It can bridge to an AMBA Advanced Peripheral Bus (APB) and manage nonblocking, multi-threaded data transfers with some built-in access security. A typical Synapse 3220 node requires an OCP agent of about 500 gates. Figure 1 shows a hypothetical SoC with a SiliconBackplane III fabric and a Synapse 3220 peripheral network.

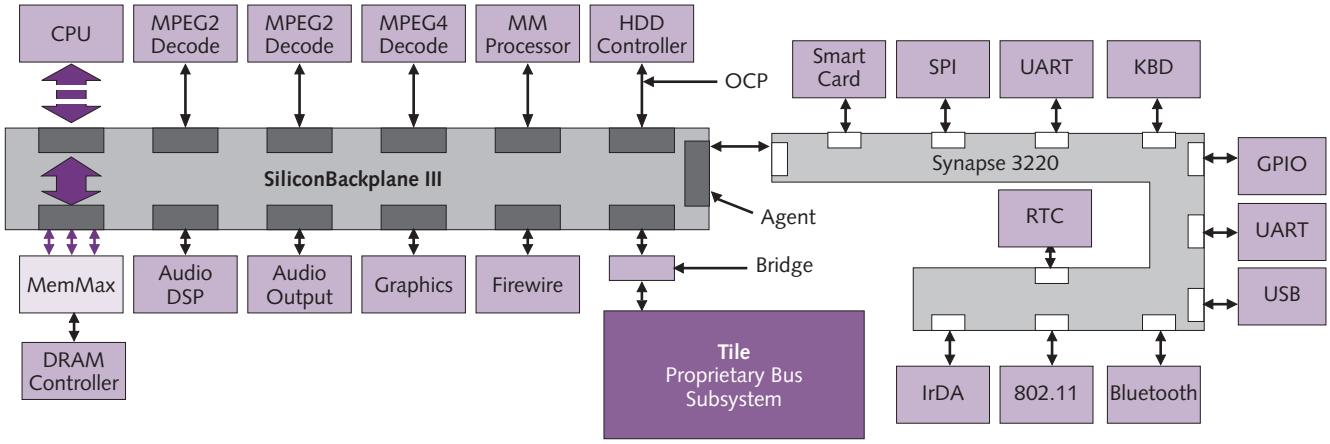

Figure 1. In this block diagram of a typical SoC design, the high-bandwidth SiliconBackplane III fabric bridges to a lower-bandwidth Synapse 3220 peripheral network and a Sonics MemMax memory scheduler. The large arrow at the left represents multiple data transfers between the microprocessor core and external memory, which SiliconBackplane III bundles into a single burst transfer across the fabric. Another bridge connects the fabric to a "tile"—a preverified subsystem of IP with its own internal bus.

An important feature of the Sonics interconnect technology is that SoC developers can group IP cores and custom function blocks into reusable "tiles" with defined interfaces. Internally, a tile can have its own buses and even an independent SiliconBackplane III fabric. For subsequent projects, developers can simply drop the tile into the design and connect it to the global SiliconBackplane III micronetwork with little effort.

Tiles are the hardware counterpart of a class file or package of classes in an object-oriented programming language—a reusable collection of functions that needs no reverification. Customers like Broadcom are using tiles to reduce the time required for some SoC projects from the usual 12–18 months to 2–8 months.

Making the Build-or-Buy Decision

The Sonics technology is impressive but doesn't come cheaply: single-use design licenses cost $240,000 for SiliconBackplane III, $120,000 for Synapse 3220, and $95,000 for MemMax. SiliconBackplane III and Synapse 3220 also incur chip royalties. Although on-chip buses like AMBA and CoreConnect are much less sophisticated, their licenses are free, and there are no royalties to pay later. SoC developers that have already produced AMBA- or CoreConnect-based designs—and their numbers are legion—may be reluctant to license an expensive proprietary technology that adds another learning curve and will probably require OCP wrappers for their core IP.

Of course, the $455,000 question is whether the Sonics technology will save enough design time and effort to recover the licensing fees and royalties. If the Sonics IP can help finish a project in half the time, it could easily save a million dollars or more in nonrecurring engineering costs and capture the revenue that would be sacrificed by a later entry into the marketplace.

Much depends on the complexity of the design and on whether any elements are reusable in future projects. A simple SoC with a single microprocessor core, a few peripherals, a small amount of memory, and average performance requirements is a relatively easy project for an experienced design team. An ordinary on-chip bus can provide enough performance, and the timing closure isn't too tricky. As the number of on-chip processors and peripherals increases, and as the performance bar rises, an intelligent switched fabric begins to look more attractive than a passive multidrop bus. Creating a switched fabric from scratch, instead of licensing one from Sonics, isn't out of the question, but an SoC design team shouldn't expect to duplicate a family of IP that represents six years of focused development.

Reusability is another critical factor. The ability to encapsulate a functional block of IP as a reusable tile with stable I/O interfaces is a powerful feature of the Sonics design tools. Entire tiles—such as MPEG decoders and baseband processors—can be moved from one design to another, amortizing their development costs over multiple projects. A one-off design that can't leverage this feature makes the Sonics licensing fees more difficult to justify.

The build-or-buy decision is similar to the quandary that SoC developers face when choosing a microprocessor core. Some market research indicates that roughly half of all SoC developers that need a programmable RISC core prefer to create their own simple processor instead of licensing an off-the-shelf core from an IP vendor. The vendors are always perturbed by this finding. For some projects, however, the roll-your-own approach is more economical. For more-complex projects that envision future modifications of the design, a sophisticated processor that's flexible enough to handle new tasks will often justify the licensing costs.

The same reasoning applies to the Sonics IP. Relatively small, low-performance designs that present little opportunity for future improvement probably don't need an elaborate on-chip micronetwork or reusable tiles of logic. Larger, high-performance designs that are expected to undergo future revisions can certainly benefit from what Sonics has to offer—as the company's star-studded lineup of licensees attests. ◇

Price & Availability

SiliconBackplane III is available now; a single-use design license is $240,000. Synapse 3220 and MemMax have been available for more than a year; single-use design licenses are $120,000 and $95,000, respectively. Chip royalties are undisclosed. For more information, visit *www.sonicsinc.com*.