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ARC Alters Trajectory

Faster CPU Core Has New Tools, Audio Extensions, Licensing Options

By Tom R. Halfhill {12/15/03-01}

ARC International was the first to license a customizable microprocessor core, but financial success has been elusive, and new competitors keep emerging. In a bid to regain the initiative, ARC has extensively revamped its product line and is pursuing a wider range of customers by offering preconfigured cores. The most significant announcement is a successor to the ARCtangent-A5 microprocessor core, the company's two-year-old flagship product.

The new ARC 600 core adds static branch prediction, more power-saving features, and a deeper pipeline that boosts the clock frequency by as much as 45%—to 290MHz in a 0.13-micron fabrication process. Like the ARCtangent-A5, the ARC 600 is a synthesizable 32-bit RISC processor that customers can configure and extend for specific applications and then implement in an SoC, ASIC, or FPGA. The ARC 600 has the same 16/32-bit ARCompact instruction-set architecture (ISA) as the ARCtangent-A5 and is binary-compatible with A5 software, although recompilation will improve performance.

New or improved hardware-development tools make it easier for customers to optimize the ARC 600 for their applications. ARC's graphical processor-configuration tool, ARChitect, has received a major facelift and is now called ARChitect 2. A new "wizard" tool streamlines the task of merging custom extensions with the synthesizable model of the ARC 600. A new hardware/software cosimulation tool allows developers to run the ARC 600 instruction-set simulator alongside the software debugger and register-transfer-level (RTL) simulations of external logic. Software programmers get some goodies, too: ARC has revised the entire MetaWare software-development tool chain for the ARC 600, including the addition of compiler optimizations that exploit the deeper pipeline and branch prediction.

Providing a user-customizable processor is still central to ARC's business strategy, but the company has decided to also offer preconfigured CPU cores for vertical applications. Previously, the only preconfigured processor cores from ARC were minor variations of the older ARCtangent-A4 that were preverified for implementation in FPGAs instead of in ASICs. Now, ARC sees more customers asking for a complete "platform" of licensable intellectual property (IP): a soft microprocessor core already customized for a popular application domain, peripheral soft-IP, supporting middleware, development tools, and perhaps some system software. To capture that lucrative business, ARC will offer new platforms of preintegrated IP as an additional licensing option. The first example is an ARC 600 processor with new hardware extensions and software codecs designed for portable digital-audio products, mainly MP3 players.

All these announcements strengthen ARC's competitive position against its chief rivals—ARM, MIPS Technologies, and Tensilica—as well as against some newcomers to soft-IP licensing, such as Octera and Silicon Hive. Although ARC can rightfully boast of an increasingly comprehensive product line, none of the new products will give ARC a decisive advantage. Therefore, ARC's fortunes remain tied to its struggle toward profitability and the general health of the industry. (See sidebar, "New Leadership Tries to Revitalize ARC.")

ARC 600 Gets a Speed Boost

Since Tensilica introduced the Xtensa V microprocessor core more than a year ago, the ARCtangent-A5 has been lagging behind in clock frequency. (See *MPR 9/16/02-01*, "Xtensa V Hits 350MHz.") In a typical 0.13-micron process, the ARCtangent-A5 hits the wall at about 200MHz. However, with a customizable processor, raw clock speed isn't the prime factor in performance. With the help of a few custom extensions, performance can often improve by an order or magnitude or more, as proved by certified EEMBC benchmarks. Indeed, a customized Xtensa V posted the highest-ever EEMBC ConsumerMark score last year at a clock speed of only 260MHz. The 150MHz ARCtangent-A4 finished a distant second in that benchmark suite but still outscored every other benchmarked processor, including a 1GHz PowerPC.

Still, it's poor marketing to lag too far behind the pack in clock frequency, so ARC took steps to boost the ARC 600's raw speed. The most significant change was to deepen the basic pipeline from four stages in the ARCtangent-A5 to five stages in the ARC 600. This seemingly minor tweak fixes a pipeline problem that surfaced in 2001, when ARC introduced the ARCtangent-A5, the first processor to use the 16/32-bit ARCompact ISA.

ARCompact cleverly improves code density by allowing programs to freely mix the usual 32-bit RISC instructions with a new subset of 16-bit instructions. (See the sidebar, "ARCompact: An Elegant 16/32-Bit ISA" in *MPR 2/18/03-06*, "Soft Cores Gain Ground.") Unlike some other 16/32-bit ISAs, ARCompact doesn't require mode switching—both types of instructions can coexist in any sequence in memory. However, this flexibility disrupts the classic RISC model of fetching fixed-length instructions in 32-bit gulps. With ARCompact, the processor must scan the instruction stream, find the instruction boundaries, and realign the instructions before decoding, much like a CISC processor. The additional gate delays in the fetch and decode stages of the ARCtangent-A5 unbalanced the pipeline and hampered the processor's ability to hit higher clock speeds.

As Figure 1 shows, ARC rebalanced the pipeline by inserting a new stage dedicated to accessing operands in the register file, which previously happened in the decode stage. Relocating the register-fetch logic to stage 3 allowed ARC to distribute the instruction-fetch and decode logic more evenly in stages 1 and 2. ARC also took the opportunity to rebalance the whole pipeline, smoothing out other wrinkles. The result is a pipeline that remains short and simple while providing enough depth to reach higher clock rates.

ARC's estimate of 290MHz is for a minimal configuration of the ARC 600, when synthesized for maximum speed in a 0.13-micron process, under worst-case conditions. Note that the base-configuration core has no caches or multiplier and totals about 27,000 gates; the vast majority of customers will want a more realistic configuration. With caches and a 32- × 32-bit multiplier, the ARC 600 grows to about 75,000 gates (excluding the cache arrays), and the maximum clock frequency drops to 205MHz. Add DSP extensions, and the core grows to 88,000 gates, and the clock frequency falls to 191MHz. The ARC 600 is definitely an improvement over the ARCtangent-A4, but the biggest performance gains will continue to accrue from custom extensions, not raw clock speed.

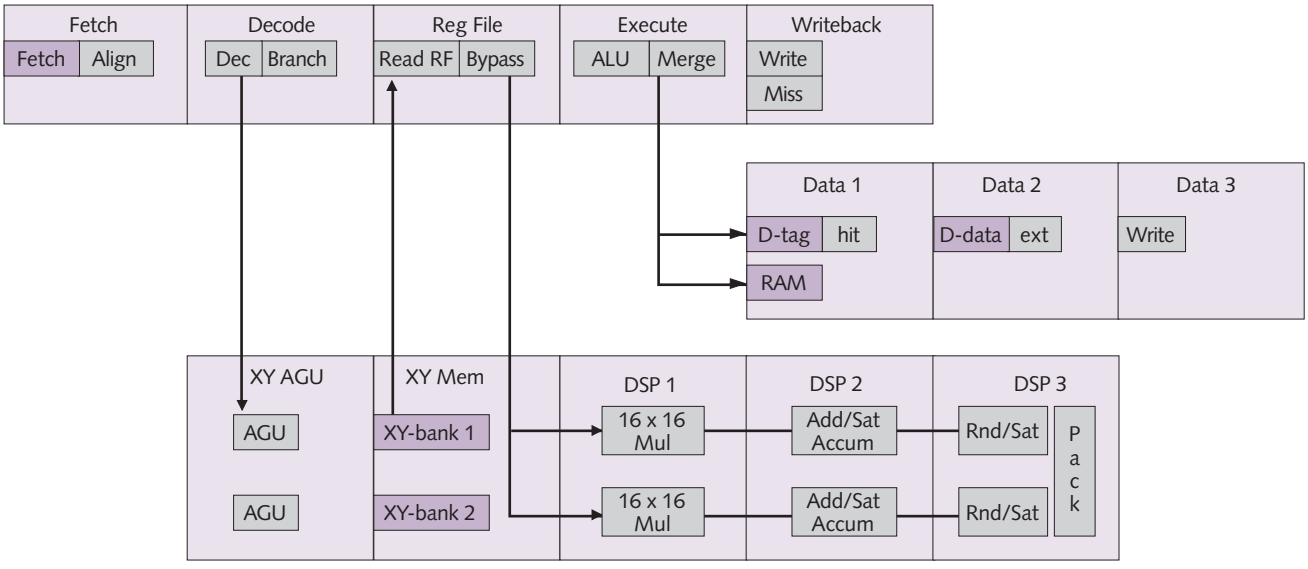

Figure 1. The ARC 600's five-stage pipeline is a classic RISC design, except for the extra logic required to align the 16- and 32-bit ARCompact instructions in stage 1. For load and store instructions, the pipeline is six and seven stages long, respectively. Adding the optional 16-bit DSP extensions to the ARC 600 creates a separately pipelined function unit in which DSP instructions can execute in parallel with nondependent ALU instructions, although the uniscalar ARC 600 can retire only one result per clock cycle.

Saving Power With Predictions

One drawback of a deeper pipeline is a larger penalty when the processor takes a conditional branch and must flush and reprime the pipe. That's why the ARC 600 is the first ARC processor that has branch prediction. A new optimization flag directs the MetaWare C/C++ compiler to use profile-guided static prediction, and the processor handles the predicted compare-and-branch instructions in stage 2 (decode).

As a result, the ARC 600 holds the cycles-per-instruction (CPI) count to about the same level as the ARCtangent-A5's CPI. This was done without sacrificing two desirable features of the older processor: conditional instructions (which eliminate some explicit compare-and-branch instructions altogether) and zero-overhead DSP loops (which the processor handles in stage 1).

ARC also added cache-way prediction to the optional two- or four-way set-associative instruction cache. Although way prediction can improve cache performance, ARC's motivation was to save power. The processor probes only one predicted way in the instruction region of the cache instead of probing all the ways in parallel while looking up the cache tags. If the prediction is accurate, the processor can begin fetching instructions from the correct way without wasting power to probe the incorrect ways or the tags. (For the seminal paper on this technique, see "Reducing Set-Associative Cache Energy Via Way-Prediction and Selective Direct-Mapping" in the *Proceedings of the 34th International Symposium on Microarchitecture: www.ece.purdue.edu/~vijay/papers/2001/waypred.pdf.*)

To save additional energy, the ARC 600 has more clock-gated power domains than the ARCtangent-A5. (Clock gating is a configuration option.) And, like its predecessor, the ARC 600 has a sleep mode that shuts down most of the processor while preserving its state. In sleep mode, power consumption drops to about 0.012mW per megahertz.

Active power consumption is also very low. ARC estimates that a base-configuration ARC 600 core (27,000 gates, no caches or extensions) will consume 0.04mW per megahertz under typical conditions when power-optimized for a 0.13-micron process. That estimate compares favorably with the active power consumption of a base-configuration Xtensa V core (25,000 gates, no caches or extensions): 0.07mW per megahertz under similar conditions.

Of course, both processors will consume more energy in an extended configuration or when synthesized for speed instead of low power. Gate counts rise quickly when customizable processors are configured and extended for typical embedded applications. An ARC 600 configured as a general-purpose embedded processor (four-way set-associative caches and a 32-bit multiplier) will have about 75,000 gates, excluding the SRAM arrays. When configured with DSP extensions (dual MAC multipliers and data memories), the ARC 600 will have about 88,000 gates, again excluding the SRAM. In comparison, the Xtensa V cores that Tensilica customized for the EEMBC benchmarks ranged from 48,000 gates (office-automation configuration) to 263,000 gates (consumer configuration).

The great advantage of customizable processors is their ability to serve in either low-power or high-performance embedded applications, depending on the way they're configured and extended. ARC's 81 licensees range from SanDisk, which uses a minimal configuration of the processor as a disk controller on flash-memory cards, to Internet Machines, which integrated 64 ARC cores on a network processor. To preserve that flexibility, companies like ARC and Tensilica avoid complicating their processors with superscalar pipelines and other features that would inflate their base configurations. Custom extensions almost always deliver more performance than gate-hungry general-purpose expansions of the core microarchitecture.

Audio Extensions Challenge Tensilica

ARC's new digital-audio extensions are a welcome, if tardy, option. The ARC 600 Digital Audio Platform is designed for portable MP3 players, digicams, DVD players/recorders, set-top personal video recorders, and multimedia mobile phones. The fast-growing MP3 market alone justifies the platform. In-Stat/MDR research analyst Cindy McCurley expects sales of MP3-capable digital-audio players to hit 18.6 million units in 2004, up from 850,000 units in 1999. The vast majority of MP3 players are battery powered, and every unit needs at least one microprocessor, so the market is attracting more attention from vendors of low-power processors. Tensilica, ARC's direct competitor, recently introduced its HiFi Audio Engine extensions for the Xtensa V. (See *MPR 9/29/03-01*, "Tensilica Makes Music.")

Although ARC's digital-audio extensions are less comprehensive and lack the 24-bit precision of Tensilica's audio extensions, they are more compact and deliver sufficient fidelity for portable players. The Digital Audio Platform includes the ARC 600 microprocessor core, 16 new instructions, and five software codecs. That compares with 54 new instructions, 23 new registers, and 10 software codecs in Tensilica's HiFi Audio Engine. However, ARC's audio platform requires only about 50,000 gates, including the ARC 600 processor and DSP extensions. (This gate count assumes the DSP extensions omit the control logic for XY data memory, which the audio extensions don't need.) Tensilica's extensions add about 50,000 gates to the Xtensa V base configuration of 50,000–70,000 gates.

To undercut Tensilica's gate count by more than 50%, ARC settled for 16-bit audio precision instead of 24-bit precision and designed a less lavish instruction set, shown in Table 1. Neither trade-off compromises the value of ARC's extensions, because almost all MP3 audio processors use 16-bit precision, and the instruction set is adequate for this application. ARC's extensions do not preclude 24-bit precision, because the 32- × 16-bit multiply and multiply-accumulate (MAC) instructions can perform 32- × 32-bit operations (and hence, their 24-bit subsets) in two steps. Although that's less efficient than using

New Leadership Tries to Revitalize ARC

As *MPR* was preparing this article, ARC removed CEO Mike Gulett and began searching for a replacement. Board chairman Peter van Cuylenberg is the interim CEO. Mike Morrissey—former CEO of ZSP—has been hired as chief operating officer until a new CEO is found. The company is also looking for a new chief architect for future microprocessor development.

Gulett came to ARC from Virata/GlobeSpan and was CEO for two years. The company continued to lose money at a rapid pace during his tenure, despite repeated cutbacks and layoffs, including 20 more job cuts last fall. In the quarter ending September 30, ARC reported revenue of $4.3 million and a net loss of $10 million. Since the company went public on the London Stock Exchange in September 2000, its stock has declined from a high of £3.46 per share (about $6) to 15.25 pence (about 26 cents) in early December 2003.

"As stated in our third-quarter results, the company has continued to reduce its operating expenses," said van Cuylenburg after becoming interim CEO. "We intend to introduce further operational improvements and reduce corporate overhead expenses in a continuing drive towards profitability and revenue growth."

a full 32-bit multiplier, it significantly reduces the processor's gate count and power consumption. ARC estimates that the complete audio platform, including processor, will consume only 0.1–0.2mW per megahertz in a 0.13-micron process—an impressively low figure that will prolong the battery life of a portable player.

To accelerate software development, ARC's platform includes optimized C and assembly-language source code for five software codecs: AAC encode/decode, MP3 encode/decode, and Windows Media Audio (WMA) decode. The AAC codecs support temporal noise spatialization (TNS), a noise-reduction technique that some AAC codecs don't support. The codecs were developed for ARC by Ittiam Systems (*www.ittiam.com*), a DSP software company in Bangalore, India. (Interestingly, Tensilica's HiFi Audio Engine was developed by Cute Solutions in Hyderabad, India.)

Instruction	Description
ASLDW	Multiple arithmetic shift left dual word
ASLSDW	Arithmetic +/- shift left w/ saturate
ASRDW	Multiple arithmetic shift right dual word
ASRSDW	Arithmetic +/- shift right w/ saturate
LSRDW	Multiple logical shift right dual word
MACFLW	MAC 32x16 fraction low word
MACHFLW	MAC 32x16 fraction high word
MACHLW	MAC 32x16 signed high word
MACHULW	MAC 32x16 unsigned high word
MACLW	MAC 32x16 signed integer low word
MAXABSSDW	Maximum absolute dual word
MULFLW	Multiply 32x16 fraction low word
MULHFLW	Multiply 32x16 fraction high word
MULHLW	Multiply 32x16 high word
MULLW	Multiply 32x16 signed integer low word
MULULW	Multiply 32x16 unsigned integer low word

Table 1. Note that barrel-shifter instructions can manipulate two 16-bit values at a time, as can some other instructions. The various 32- × 16-bit multiply and MAC instructions can perform two-step 32- × 32-bit multiplies and MACs at a much lower gate count than a full 32-bit multiplier would require.

The ARC 600 can run the audio codecs at clock speeds well below its maximum frequency. ARC's estimates are 28MHz for MP3 decoding, 51MHz for MP3 encoding, 35MHz for AAC decoding (with TNS), 53MHz for AAC encoding (with TNS), and 37MHz for WMA decoding. (These estimates assume a bit rate of 128Kb/s and a sampling frequency of 48KHz.) Power consumption at those clock frequencies would range from a low of 2.8–5.6mW to a high of 5.3–10.6mW (at 0.13 micron). Clocking the processor at a higher frequency would provide head room for additional tasks. ARC intends to add video codecs in a future release of the platform and will port the voice codecs already available for the ARCtangent-A5.

Improved Tools Ease Development

Despite the relative simplicity of ARC's processors, internal revisions to the microarchitecture usually take about two years. One reason is that the hardware/software tool chain for a customizable processor is so dependent on the microarchitecture. Every revision requires rewrites or updates to four representations of the processor: the synthesizable VHDL and Verilog models plus the C-based instruction-set simulator and the cycle-accurate simulator.

In addition, ARC must revise its graphical processor-configuration tool (which almost amounts to another model of the microarchitecture), the assembler, linker, C/C++ compiler, and debugger. More adjustments may be required to the code profiler, in-house peripheral IP, Precise/MQX real-time operating system (RTOS), and miscellaneous other system software and middleware. Those are a great many code bases to synchronize and support.

For the ARC 600, the company has not merely updated the tools, it has significantly overhauled some of them and created new tools. The improved processor-configuration tool, ARChitect 2, adopts the property-sheet user interface seen in many object-oriented software-development environments. When the developer selects a component—for example, the optional instruction cache—ARChitect 2's

new property box displays all the configurable parameters for that component, such as the cache's size, set-associativity, and bus width. Developers can configure the component by clicking on check boxes and selecting menu options. Figure 2 is a screen shot of ARChitect 2.

Two new development aids are the Extension Integration Automation (EIA) Wizard and MetaSim, a hardware/software cosimulation tool. The EIA Wizard is a fancy VHDL/Verilog editor that makes it easier for developers to integrate custom extensions with the ARC 600 core. In the past, developers had to manually merge their HDL with the synthesizable model of the processor and ensure that all the signals were properly connected. Entry points in the processor's HDL were marked and documented, but it was possible to make mistakes. The EIA Wizard guides the developer through a four-step process that should eliminate any guesswork.

The new MetaSim tool runs the ARC 600 instruction-set simulator alongside the MetaWare SeeCode debugger and the developer's HDL simulator. It allows developers to test software on separate simulations of their own RTL logic and the processor, using a shared memory model. Simulation speeds are 1–2 mips. For critical performance testing, ARC's 100% cycle-accurate simulator runs at a simulated clock speed of 415kHz on a 2.8GHz desktop PC. (Faster simulation is possible with ARCangel, an FPGA-based development system.) ARC's tools run on Windows, Solaris, and Linux.

ARC Needs a Crystal Ball

Although the ARC 600 Digital Audio Platform is new, ARC has been gravitating toward a hardware/software platform strategy for a few years. ARC believes more customers want easy solutions, with hardware and software IP in a preintegrated package. By obtaining as much IP as possible from a single source, customers can spend less time integrating and verifying individual components and more time developing proprietary IP that gives them a competitive edge in the marketplace. ARC intends to be the supplier of the preintegrated IP for popular embedded applications.

It's a sound strategy from the standpoint of demand, especially if synthesizable IP follows the evolution of software development. For many years now, programmers have been able to buy or license prewritten software components and class libraries that save them months of redundant work. Why write another TCP/IP stack or rich-text editor if these components are available off the shelf? Likewise, why design a custom microprocessor from scratch or create digital-audio extensions for an existing processor if equivalent IP is readily available for licensing? The differentiation that makes or breaks a product is probably at the higher level of industrial and user-interface design.

ARC's challenge is to execute the platform strategy. One problem is resources: ARC strives to be a one-stop shop with a broad shelf of soft-IP and system software, but it's a relatively small company (about 180 employees) hard-hit by layoffs during the tech recession. Just maintaining the code bases for all its existing products and enhancing the centerpiece of its product line—the customizable processor and related tools—is a strain on ARC's shrinking engineering resources. Competitors that are about the same size as ARC (MIPS, Tensilica) focus almost exclusively on their processors.

To stretch its resources, ARC is relying more heavily on business partners and outsourced engineering. Of course, this is consistent with industry trends, but it can complicate project management and product support. To keep things coherent, ARC seems to be more territorial when dealing with its partners. For example, although both ARC and Tensilica outsourced the development of their digital-audio extensions, ARC owns the finished IP, whereas Tensilica merely acts as the marketing agent for its Indian partner, which owns the IP.

Another obstacle ARC must overcome while pursuing a platform strategy is identifying popular embedded

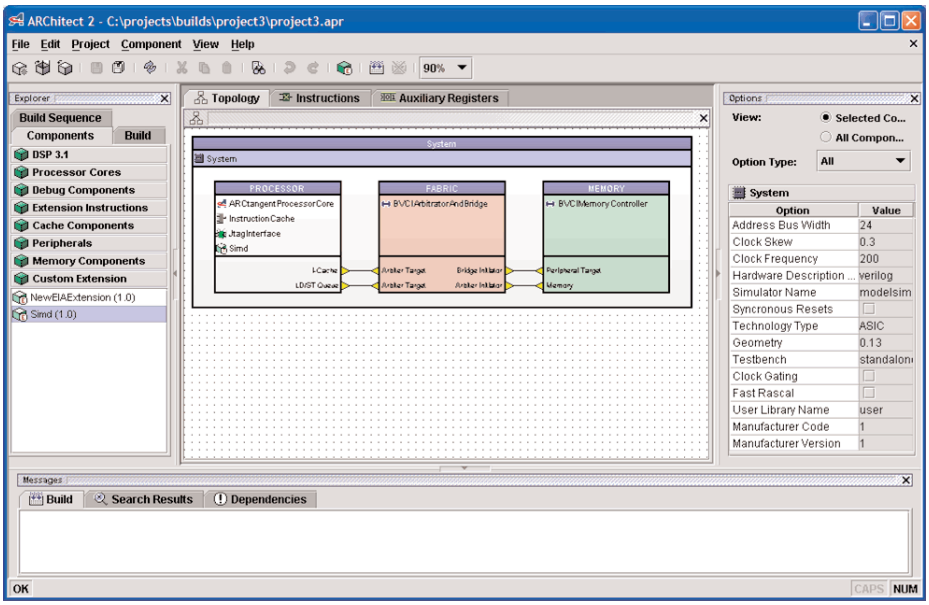

Figure 2. After its facelift, the ARChitect 2 processor-configuration tool resembles the GUI designer of a software-development tool. Notice the property box at right, which displays all the configurable options for the selected component. At left is the drag-and-drop component library. After configuring the components, the developer issues the "build" command by clicking a tool-bar icon, which assembles the prewritten VHDL or Verilog modules required to synthesize the processor. ARChitect 2 also generates the appropriate synthesis scripts and test-bench routines for the target fabrication process.

Price & Availability

Synthesizable models of the ARC 600 customizable processor and the Digital Audio Platform are available for licensing now, in VHDL and Verilog formats. The Digital Audio Platform requires a separate license for the ARC 600 DSP extensions. ARC does not publicly disclose licensing fees or terms for synthesizable IP. Licensing fees for the digital-audio software codecs are $30,000 per encoder and $50,000 per decoder. The new and improved development tools are available now; some are included with the ARC 600 license. For more information, visit *www.arc.com*.

applications—and identifying them early enough to develop the necessary platform IP while the market is still hot. This won't be easy, because it will take ARC at least a year to develop a useful package of IP for an emerging application, and then customers will have to spend a year or two using the IP to spin a chip and design their product. Starting from the point when ARC identifies a potentially lucrative market, that's a total time-to-market window of two or three years—and much can happen in two or three years.

Consider how ARC was bitten by Bluetooth. In 2000, ARC introduced a platform of Bluetooth-related hardware/software IP called BlueForm. The goal was to make it easier for developers to integrate Bluetooth wireless communications into their SoCs. When ARC had begun developing BlueForm about a year earlier, the industry was expecting rapid adoption of Bluetooth. For reasons beyond ARC's control, Bluetooth didn't catch on as fast as predicted, and BlueForm sank in the marketplace. ARC withdrew it last year. Ironically, Bluetooth is only now starting to fulfill its early promise, but ARC has moved on to new frontiers.

ARC's digital-audio platform seems to be a safer bet, now that the record companies are growing more comfortable with the idea of downloaded music. But it's been almost six years since Eiger Labs introduced the first portable dedicated MP3 player in March 1998, and two more years may elapse before ARC's new audio extensions appear in a finished chip in a finished product. ARC is a latecomer to a hot market that's already becoming crowded.

To successfully execute its platform strategy and generate the royalties it needs, ARC will have to improve its foresight, avoid delays when outsourcing projects to development partners, introduce good products like the ARC 600 and Digital Audio Platform much sooner, and pray for better luck from the fickle winds of the marketplace. ◇