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PicoChip Makes a Big MAC

Massively Parallel Chip Has 260 Multiply-Accumulate Processors

By Tom R. Halfhill {10/14/03-03}

If you want a Big Mac, go to McDonald's. If you want a big MAC, see PicoChip Design. The U.K.-based company is introducing the PC102, a massively parallel communications chip that contains 344 processors, including 260 with multiply-accumulate (MAC) units.

PicoChip COO and chief architect Peter Claydon announced the PC102 on October 14 at **Microprocessor Forum 2003**. It's surprising that a relatively small startup could design such a complex chip so closely on the heels of its first product, the PC101, which Claydon unveiled only four months earlier at Embedded Processor Forum. (See *MPR 7/28/2003-02*, "PicoChip Preaches Parallelism.") However, both the PC102 and PC101 are based on the same picoArray architecture, so they have more similarities than differences. Both are communications chips for cellular-telephony and wireless-network infrastructures, although they would excel at other signal-processing tasks.

Despite several enhancements, the PC102 does not supersede the PC101 in the same way that an Intel Pentium 4 replaces a Pentium III. Although the PC102 has twice as many on-chip processors with MAC units as the PC101, the earlier chip has more processors in total. They are siblings, not quite twins, designed for customers having different computational requirements.

PicoChip says the PC102 will ship in 1Q04 and run at 160MHz at its nominal core voltage of 1.2V. Like the PC101, it will be fabricated in TSMC's eight-layer-metal 0.13-micron digital CMOS process. Volume pricing will be announced soon.

Massive Parallelism for Communications

PicoChip's basic design philosophy remains the same: cram hundreds of small, local processors on a single chip; equip

Feature	PicoChip PC102	PicoChip PC101
Architecture	picoArray	picoArray
Frequency	160MHz	160MHz
Instruction Format	3-slot LIW	3-slot LIW
On-Chip Processors	344 total	430 total
STANdard	260 [1]	240
MAC	260 [1]	120
MEMory	65	68
CTRL	4	2
Function Accel Units [2]	15	0
Native GIPS [3]	158	206
16-Bit MACs	1 cycle	1 cycle
32-Bit MACs	4 cycles	—
Sustained MMACS [4]	41,600	19,200
Bootstrapping	Self-boot	Host CPU
External I/O	4 x 5.12Gb/s	4 x 2.56Gb/s
Process	0.13µm 8LM	0.13µm 8LM
Voltage (core, I/O)	1.2V, 2.5V	1.2V, 3.3V
Foundry	TSMC	TSMC
Power (typ, peak)	4W, 6W	3W–4W, 7W
Package	FCBGA-704	BGA-528
Package Size (mm)	29 x 29	37.5 x 37.5
Availability	1Q04	1Q04
Price	TBA	TBA

Table 1. The new PC102 is generally more sophisticated than the PC101, but it is smaller in the same fabrication process. TBA: to be announced in 4Q03. [1]STANdard and MAC processors are combined in the PC102. [2]Function accelerator units are application-specific local processors. [3]Giga-instructions (1,000 million) per second. [4]Million multiply-accumulates per second (16-bit).

each processor with its own instruction memory, data memory, and register file; program the processors with three-slot long instruction words (LIW); knit the processors together with a complex fabric of internal 32-bit datapaths; provide enough I/O bandwidth to keep the processors busy; and allow embedded-system designers to link together multiple chips to assemble even larger arrays of processors.

By carrying out tasks with their own local registers and memory, the individual processors in the PC101 and PC102 can reduce off-chip memory accesses and conserve their I/O bandwidth for data. They are well suited for data-intensive applications, such as processing the multiple channels of datastreams in cellular and wireless base stations.

The basic building block of the picoArray architecture is a 16-bit integer processor, roughly comparable to an ARM9 for control tasks or a TMS320C55x DSP for signal-processing tasks. The new PC102 has 344 of these local processors on chip, compared with 430 on the PC101. However, the PC102's 344 processors include 260 with MAC units, whereas the PC101 has only 120 MAC processors. Table 1 summarizes the important differences between the chips.

Each MAC-type local processor can execute a 16- × 16-bit MAC in one clock cycle and store the result in a local 40-bit accumulator. By more than doubling the number of MAC processors in the PC102, PicoChip has increased the number of sustainable MAC operations by a like amount: 41,600 million MACs per second (MMACS) at 160MHz, compared with 19,200 MMACS for the PC101 at 160MHz. In addition, the PC102's MAC processors have new instructions, not found in the PC101, that can perform a double-pumped 32- × 32-bit MAC in four cycles.

The improved MAC resources will make the PC102 more broadly useful for communications and other data-intensive applications. Two examples cited by PicoChip are adaptive antenna algorithms—such as those used for multi-input multi-output (MIMO) antennas—and a function known as joint detection or multiuser detection (MUD). To perform the latter function, the processor demodulates the signals for all users in a CDMA (code division multiple access) system in parallel to determine their mutual interference.

```
entity Modifier is                                  ┐
  port (myOutPort: out integer32@16;                │
        myInPort: in  interger32@16);               │
  end entity Modifier:                              │ VHDL interface
                                                    │
architecture C of Modifier is                       │
begin MEM                                           │
  CODE                                              ┘
  int main()  {                                     ┐
   while (1) {                                      │
    integer32 value = getmyInPort();                │
    value += 10;                                    │
    putmyOutPort (value);                           │ ANSI C body
   }                                                │
   return 0;                                        │
  }                                                 │
  ENDCODE;                                          ┘
end Modifier;
```

Figure 1. Programmers can specify the VHDL interface by using a structural subset of VHDL. The ANSI C bodies can use all features of C.

MAC processors aren't the only type of local processors in a picoArray. PicoChip describes the other processor types as STAN (standard processors: 16-bit integer); MEM (memory processors: 16-bit integer processors with a multiplier and 8.5K of local memory); and CTRL (control processors: similar to MEM processors but having 64K of local memory). In many applications, CTRL processors handle protocol termination and supervise groups of other processors. In the PC102, the MAC and STAN processors are combined, not distinct types. Therefore, the 260 MAC processors also execute standard integer operations, sometimes in parallel with MAC operations.

Of the 84 non-MAC processors in the PC102, 65 are MEM processors and four are CTRL processors. In addition, the PC102 has 15 new processors not found in the PC101. These "function accelerator units," as PicoChip calls them, provide application-specific hardware acceleration for widely used communications functions, such as correlation and forward error correction.

Enhanced Internal and External I/O

By using the switched-fabric datapaths of the picoArray architecture—described in more depth in the previously cited PC101 article—every local processor in the PC102 can communicate directly with every other local processor. One improvement in the PC102 is the addition of two new horizontal buses that bypass the local processors and directly connect the switches between the horizontal and vertical buses in the fabric. These "bypass" or "expressway" buses are useful in applications that must globally distribute large amounts of data to dozens or hundreds of local processors. An example is the data coming from multiple antennas in the RF stages of a wireless base station.

Four interfaces handle off-chip I/O and let embedded-system designers stitch multiple picoArrays together to create larger fabrics. The PC102 improves on the PC101's design by doubling the I/O bandwidth per interface to 5.12Gb/s, or 20.48Gb/s of aggregate bandwidth per chip, compared with 10.24Gb/s of aggregate bandwidth for the PC101. The new chip's I/O interfaces are also more flexible, allowing direct connections to standard serializer/deserializer (serdes) devices, with support for both fixed- and variable-size packets.

The PC102's instruction set has a few improvements over the PC101's but is largely the same. In addition to the new 32-bit MAC instructions, the PC102 has some conditional copy/move instructions, for more-efficient compilation, and a halt instruction that lets programmers insert breakpoints more easily. Software written for the PC101 will run on the PC102 when recompiled or reassembled. The reverse is true only sometimes: software that uses the PC102's new instructions or functions obviously won't run on the PC101.

Software development on both chips remains the same—unorthodox but not insurmountable. Programmers can write applications with PicoChip's ANSI C compiler and assembler, but they must specify the signal flows among the local processors by using structural VHDL, normally a hardware-design language. It's less difficult than writing behavioral VHDL, because there's no need for logic synthesis. The structural VHDL is necessary only because plain-vanilla C lacks the semantics to define interprocessor signal flows. Figure 1 shows a simple example. To help automate this task, PicoChip plans to support a schematic editor later this year.

Math Muscle for 3G Networks

PicoChip hopes to win sockets by absorbing some or all functions of multiple chips in base stations: the control/protocol processor (usually a RISC processor), the channel codec (usually a DSP), the modem (usually an ASIC or FPGA), and even a piece of the analog RF section. (The PC102 can replace some analog filters with digital filters, and it implements power-amplifier linearization, normally considered an RF function.) The PC102's ability to boot directly from ROM or flash memory gives it more autonomy than the PC101, which depends on an external host processor for bootstrapping.

The PC101 and PC102 are intended primarily for next-generation cellular and wireless networks, not for today's narrowband voice/data networks. PicoChip estimates that a 64-user baseband processor for a Universal Mobile Telecommunications System (UMTS)—a 3G mobile broadband technology for voice, data, audio, and video—must execute at least 2,000 GIPS (giga-instructions per second). That level of performance is within reach of a picoArray consisting of 10–15 PC101 chips. PicoChip's design team has already made PC101-based development boards with as many as 16 chips that can execute a total of 4.4 trillion instructions per second. The PC102 does even better: with its additional MAC processors, new function accelerator units, and other improvements, it can deliver comparable performance with only four to six chips, according to PicoChip.

It will be easier to evaluate PicoChip's unusual design philosophy when the company announces volume pricing, firm delivery dates, and design wins. The massively parallel PC101 and PC102 are fairly large, complex devices, limited to a relatively slow clock frequency (160MHz), even when fabricated in a leading 0.13-micron process. However, their power consumption seems reasonable: about 4W typical, 6W peak for the PC102, and about 7W peak for the PC101. That's not much power for a muscular communications chip that can potentially replace multiple RISC processors, DSPs, ASICs, and FPGAs. Furthermore, the PicoChip devices are standard parts, obviating the need for an ASIC development project. If PicoChip can deliver on its promises and catch the attention of major base-station vendors, it may have a pair of winners. ◇

Price & Availability

PicoChip says it will announce volume pricing for the new PC102 and previously announced PC101 shortly. Both chips are scheduled for production in 1Q04. For more information, see *www.picochip.com*.